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NIST TIP White Paper:
TIP Critical National Needs Ideas:

Next Generation Lithography

"As we push down to 11 nm lines and spaces"

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Semiconductor Industry Review

The semiconductor industry is an enabling industry to the U.S. economy. Semiconductor chips are used in virtually all industrial, automotive, telecommunications, computing, military, medical, and consumer products. In 2010, world wide semiconductor sales were an estimated $300 billion[1]. For the past 45 years the semiconductor industry has been growing at an annual rate of ~25 percent per year. This amazing growth rate is typically explained by the general form of Moore's Law[2], namely, the semiconductor industry doubles the number of transistors on integrated circuits every two (or three) years. The dramatic increase in the number of transistors on integrated circuits has continuously improved computer performance and reduced costs to U.S. consumers. While reduced costs and improved functionality drive the entire semiconductor industry, the ability of the semiconductor industry to follow Moore's curve (at least through 2020) depends heavily on continuing to increase the productivity of semiconductor equipment and to extend the capability of existing tool sets for next generation technology and product cycles. Recently, the ITRS (2010)[3] has introduced the concept of Functional Diversification ("More than Moore", MtM). This new definition (MtM), addresses the emerging category of circuits that incorporate functionalities that do not necessarily scale according to "Moore's Law," but provides additional value to the end customer in different ways.

As the cost of computer functionality to the consumer falls, the cost for manufacturers to follow Moore's law follows an opposite trend. Each year, R&D and manufacturing costs have increased steadily with each new generation of chips. In fact, "Moore's second law" implies that the capital costs associated with a new semiconductor manufacturing facility increase exponentially over time[4]. Largely responsible for these increased costs is the single most expensive module in the fabrication process, namely, the lithographic patterning process. Pattern processing and metrology equipment accounts for ~50% of the equipment capital cost in U.S. and foreign facilities[5]. The surge in the number of foreign foundries and the reduction of U.S. based foundries from 1995 through 2010 is a clear sign that semiconductor industry is constantly searching for ways to reduce chip production costs through labor, construction, and infrastructure reductions.

Over the past decade (2000-2010), the number and diversity of new semiconductor products has grown to such an extent that semiconductor companies continue to reduce product cycle times to stay competitive – this *world-wide* consumer driven push places huge time constraints on corporate R&D, which must deliver new tools to industry. The growth in the semiconductor industry has moved from the PC to powerful handheld devices that are now routinely equipped with GPS, advanced sensors, and interfaces that monitor the health of the user. The semiconductor patterning process is the single most critical and capital intensive part of the semiconductor manufacturing process, and the one needing the most co-operative attention now and in the future. Semiconductor technology can make winners and losers out of countries – those in the front and those behind in the technology race.

Current Trends and Technologies

The growth in the mobile phone and handheld device market has been steadily improving throughout the past decade (2000-2010). This trend is expected to accelerate, with the expectation that handheld device will become computationally as powerful as the laptop while using less energy to operate. As semiconductor transistors have gotten smaller and faster, circuit manufacturing has become technically more challenging. To increase CPU speed and functionality, designers and manufacturing engineers are now using multi-core, microprocessor designs and advanced materials to compensate for fundamental limitations in the physical characteristics of CMOS transistors. As the ITRS lithography roadmap[6] describes, sub-16 nm (half pitch) processing will require novel solutions to complex manufacturing and design problems – limited by several critical technological barriers.

The nano technology field has exploded over the past 10 years (2000-2010). By far, the most prolific example of nanotechnology is the semiconductor industry. Currently devices at dimensions of 32 nm are routinely being fabricated and EUV lithography provides a path to single digit nm devices. The great power of top down optical techniques in the production of nanodevices is the complete flexibility it affords enabling the creation of extremely complex devices without any requirements on short or long range order. Moreover, the intrinsically parallel nature of projection lithography techniques allows these complex nanostructures to be fabricated at incredible speeds. For example, at the 8-nm node, a single high volume nanolithography tool might be expected to be able to fabricate $4.5x10^{17}$ bits of information every hour. Attaining the single digit nanoscale will thus bring to fruition incredible computing and sensing power in very small footprints and at very low cost. This in turn will finally enable truly smart environments bringing the benefits of nanotechnology to the macro environment we all live in. Such proliferation of computing and sensing power will lead to a host of benefits in a wide variety of areas including crucial sectors such as biomedical and energy efficiency. First however, we need to develop the semiconductor manufacturing processes and tools to get us there. Most importantly, we must strengthen the joint collaboration between U.S. industry, research labs, university, and U.S. government agencies to develop the tools that will enable next generation lithography and the future products that help make the U.S. a leader in technology.

Challenges for Next Generation Lithography (Technical)

According to Dan Armbrust, president and CEO of SEMATECH, “Lithography is the linchpin of success in the semiconductor industry,” “It has enabled productivity in the information technology industry for the past 45 years, and has sustained the semiconductor industry’s underlying business model. Now, for the semiconductor industry to continue to grow, lithography must remain profitable in the face of current technical and economic challenges.”

According to the ITRS[7], it is becoming increasingly more difficult to extend optical lithography as we know it today. In 2010, Flash devices were being manufactured using 32 nm half-pitch double patterning (DP) as a way of extending the half-pitch while keeping the Numerical Aperture (NA) and wavelength constant. This approach will probably continue as DRAM (and MPU) move towards a 32 nm half pitch and Flash memory products near the limit of optical solutions for the 22 nm half-pitch node in ~2014. But it is near this technology node that an alternative Next Generation Lithography (NGL) must be introduced into manufacturing for a transition into sub 22 nm semiconductor manufacturing.

EUV lithography is the lead candidate for NGL because of its potential for lower cost of ownership. Second, is extending 193 immersion double patterning down to a k1 of 0.15 for 22 nm half-pitch, followed by maskless lithography (e-beam technologies) and imprint lithography[7]. In many cases, the technology is not limited by the lithography tool, but rather by the supporting technologies. There are many difficult challenges as we move into the NGL regime. For EUV lithography (≤16 nm), ***masks, radiation sources, metrology, and resist systems*** are critical components that require further development.

Proposed Areas of Study

- **EUV Source and Collector**
- **Metrology and Resist Development**
- **Mask**

EUV Source:

EUV source development started over 20 years ago[8]. The challenges for EUV lithography were initially so difficult that the technology was often considered not practical for high volume manufacturing. To some extent, this view still holds for many involved with the manufacturing and development of EUV lithography systems and subsystems. To keep pace with the ITRS lithography roadmap (for sub 16 nm lithography), EUV power scaling, double patterning, higher NA optics, and the possibly of developing new EUV sources (13.5 nm) with smaller wavelengths (~6 nm) has already been discussed. Given that the first prototype lithography tools with high power EUV sources were delivered to industry just 4 years ago (2006), the EUV research track needs to be accelerated to meet future production needs. This is a very expensive and complex undertaking for the very few U.S. companies and research centers who are experts in this critical and gating area.

For EUV lithography, the availability of high power 13.5 nm sources has been categorized as high risk and ranked as critical with other technologies requiring significant developments to enable the realization of EUV lithography[7]. High sensitivity photoresists with good line-edge-roughness (LER) are needed to keep the required source power within reasonable limits. Photoresist sensitivity and other light absorbing elements are the basis to derive EUV source power requirements within the usable radiation bandwidth of 2 %. According to the joint requirements from scanner manufacturers[9], an

EUV power of >115 W with 2 % bandwidth at the intermediate focus (IF) is required for 5 mJ/cm^2 photoresist speed to enable >100 wafers per hour (WPH) scanner throughput, and 180 W with 2 % bandwidth at IF is needed for 10 mJ/cm^2. Photoresist sensitivities above 20 mJ/cm^2 could drive power requirements well above the 200 W level, and the need for a Spectral Purity Filter (SPF) could increase the requirements even higher. *A scalable EUV source architecture* is needed to enable the evolution of EUV lithography during the life cycle of the technology. A comprehensive review of EUV source developments for lithography was given in the book edited by Bakshi.[10] Following the early development of discharge produced plasma (DPP) sources, laser-produced-plasma (LPP) sources are expected to deliver the necessary high power for critical-dimension high volume manufacturing scanners for the production of integrated circuits in the post-193 nm immersion era.

EUV LPP power roadmap:

Technology (DRAM half pitch)	25 nm	20 nm	16 nm	11 nm	8 nm
Year	2014-2016	2016-2018	2018-2020	2020-2022	2022 - 2024
Source Power (W) / λ	250 W λ= 13.5 nm	350 W λ= 13.5 nm	350 W λ=13.5 nm	500 W λ= 13.5	>500 W λ=6 nm open

Collector damage and nanolayer development:

For the 20 nm technology node (2017), high-power EUV source operation is required to support high wafer throughput at the exposure tool. During LPP EUV source generation, a stream of high speed, tin droplets are injected into a vacuum system and are evaporated and ionized by a powerful carbon dioxide laser pulse. This ablation results in a flash of radiation that is reflected off the surface of a large collector optic (coated with a complex nano-layer stack, typically 60+ alternating layers of Mo/Si to achieve >70% reflection efficiency) and focused at a position called intermediate focus (IF). The EUV light from this plasma event is sent into the optical system and is used for exposing resist coated wafers. A key challenge facing development of LPP EUV sources is to maintain the high collection efficiency and stable power output over long periods of time in order to meet the critical Cost of Ownership (COO) targets. The proximity of the collector optic to the high temperature plasma exposes it to high energy ions, neutral atoms and other debris which can potentially damage the coating and reduce reflectivity. The three main degradation mechanisms are deposition of tin particle debris from the droplets, erosion of the mirror by high energy ions and neutral atoms, and deposition of tin vapor. The decrease of the droplet size has arguably the most important beneficial impact on the effectiveness of debris mitigation techniques. It is necessary to reduce the load on the individual debris mitigation subsystems responsible for eliminating each degradation mechanism. Droplet sizes with diameters as small as 30 μm have been demonstrated for extended run times and are now routinely used in LPP systems for integrated testing. Such small droplets provide the added advantage of reducing the annual tin consumption, which also reduces tin material costs.

The development of very high power (> 500 W) EUV sources (possibly at a wavelength of 6 nm) will require the development of new source materials (for example, Gd or Tb), source injection systems, and methods to control particle debris. The development of these complex EUV source systems will require modeling the plasma and emission field of the source material, understanding the fluid and gas dynamics of the source injection process, investigating new highly efficient source materials, and developing complex, nanolayer systems (possibly including, C, B, W, La Ru, Mo, Co, Ni, Cr) for robust collector optics.

The research activities for creating a new and robust collector for high power EUV applications (with reduced COO) should include: investigations of new collector substrate materials for good thermal management, new optical metrology for characterizing the surface roughness for atomically flat surfaces, and the development of robust nanolayer coatings. Nanolayer development activities should include the development of: self-healing atomic layers (possibly using Atomic Layer Deposition (ALD) methods, developing nanolayers with improved diffusion resistance, new surface protection layers, diffusion barriers, new absorber and spacer material layers.

The development of new robust EUV mirror surfaces will also require investigating the following complex surface interactions: surface oxidation, surface photo chemistry, radiation and plasma damage, interface roughness at the atomic level, and diffusive mixing - for each coating design.

Benefits from these research and development activities will lead to improved life-time and reduced COO for high power EUV sources and materials.

Other critical areas for NIST consideration:

Since the drive laser for the LPP EUV source is a large, carbon dioxide laser (~100 kW), the development of high power fiber lasers[11] with small footprints is an interesting research area - especially if the fiber drive system(s) can operate at high power and reduced costs. Advantages of fiber lasers include good power scaling, high efficiency, and high repetition rates.

Metrology and Resist Development:

Early in the development of EUV lithography, the general belief, arguably by necessity, was that non-actinic metrology of EUV systems, mirrors, and masks would be sufficient. As the complexity of EUV systems has increased and evidence mounts of crucial wavelength dependent effects, the need for EUV (actinic) metrology in all areas of EUV technology is now widely accepted. The delay in this realization has led to significant differences in maturity of EUV lithography systems compared to metrology systems and arguably poses a threat to the successful commercialization of lithography as a whole.

Areas of EUV metrology where no commercial solutions exist include high-NA wavefront interferometry, high accuracy reflectometer/scatterometer for very large optics,

and mask inspection systems including mask blank, patterned mask, and aerial image systems. Various challenges remain in the development of such systems with the largest being the availability of sources with suitable brightness. The requirements for metrology sources are intrinsically different than those for lithography sources making the use of lithography sources for metrology applications unsuitable. Separate and parallel development of metrology specific sources is required.

Other significant metrology challenges also remain and must be addressed in parallel with source development if timely progress is to be made. For example, lithographic systems require extremely high wavefront accuracy. Typical lithographic optics are two to three times better than what is typically referred to as a diffraction limited optic. This places extreme demands on wavefront metrology systems which increase dramatically with increasing numerical aperture. Research should be directed towards the development of EUV-compatible wavefront metrology systems for numerical apertures of 0.4-NA and above. Moreover, although the research is arguably best be carried out at synchrotron facilities, the research should focus on the development of metrology techniques compatible with the laboratory-scale sources of the future.

Mask inspection is another crucial area for metrology. Significant questions remain in the design of systems that can simultaneously capture the full range of EUV defects which includes a complicated mixture of defects underneath, within, and on top of the multilayer. To make immediate progress in this area, synchrotron sources could also be used, but again development would ideally be focused on systems compatible with future commercial sources. That being said, much can be learned even from synchrotron-specific systems from the perspective of defect classification and setting specifications for future tools.

The development of ultra-high resolution EUV resists is another area of significant concern. Progress in this area is in large part limited by the lack of availability of ultra-high resolution exposure systems. Just as we cannot wait for high brightness source development to be completed before addressing metrology issues, we cannot wait for ultra-high resolution commercial lithography tools to become available before addressing resist issues. Arguably, the resist should be ready by the time the lithography tool is ready. Given lack of market for advanced lithography tools meant solely for resist development, the only viable approach to developing such complex systems which are two to three nodes in advance of commercial tools, is through government/industry partnerships. Also, such tools are ideally located at synchrotron facilities where source costs can be mitigated and resist progress can be decoupled from source progress. This is especially true as EUV lithography research moves towards 6 nm wavelength.

Mask:

As mentioned earlier, after a long run, optical lithography is unlikely to be able to pattern chips beyond the 22 nm technology generation and extreme ultraviolet lithography (EUVL)—with a wavelength of only 13.5 nm—is now widely considered the best replacement for optical lithography. Since 2003, however, the semiconductor industry has ranked defect-free EUV masks among its top three technical issues. EUV masks used for sub-22 nm patterning must be free of printing defects and current metrology tools are generally ineffective at finding defects below 32 nm.

Defects from EUV lithography can derive not only from the traditional opaque defect in the patterning layer but also from small phase defects on the EUV substrate or a phase defect generated in the multilayer of the reflective blank. These defects are created either during the substrate polishing and cleaning or while depositing the many silicon and molybdenum layers that comprise the multilayer reflector of the mask blank. Neither the hardware to polish and clean the substrate nor the equipment that deposits the multilayer can operate without adding defects today. Creating the polishing, cleaning, and deposition tools that can operate defect-free will require invention, investment, and significant development time.

Mask defects of 16 nm and below are beyond the resolution limits of today's existing metrologies. Substrate inspection will require the use of novel strategies to enhance contrast at optical wavelengths. As mentioned above, blank inspection will require an actinic, or EUV, inspection wavelength to detect phase defects. Once the mask blank is patterned, actinic wavelengths will be required for pattern inspection and aerial image review. The inspection equipment infrastructure (substrate, blank, patterned mask, and AIMs) needed for EUV mask manufacturing at the 16 nm node does not exist.

Finally, once defects have been located they must be characterized. The most common commercially available characterization technique is Energy Dispersive Spectroscopy (EDS), but EDS only provides reliable chemical composition capability down to 80 nm. Defects being detected today are 30 nm in size, and those that must be found and eliminated to enable manufacturing with EUV are 16 nm and smaller. New characterization techniques such as Auger spectroscopy and photo-thermal infrared resonance (PTIR) are somewhat available in laboratory settings. These and other methods must be identified and developed in the form of clean commercial products that can be used by the mask blank manufacturers. As with many of the other challenges described earlier in this paper, each of these development projects requires innovation, sometimes disruptive in nature, coupled with significant investment capital and years for product development.

Producing the tools required to address the gaps in mask infrastructure is far too costly for any single company or industry sector to develop independently, and will require collaborative innovations that address both technology and business needs across multiple industry segments.

Challenges for Next Generation Lithography (Economic Barriers)

U.S. R&D Funding Trends (The critical need for NIST TIP funding):

Intel, the leading U.S. manufacturer of complex microprocessors, has reported recently[12] (2010), that semiconductor research and development spending has continued to rise in both dollars spent and as a percentage of corporate revenues (approaching 20%). This trend is expected only to continue as the industry looks to manufacture semiconductor circuits to stay on track with Moore's Laws. The semiconductor industry spends more money on hardware and process development as compared with software. The dollars for state and local governments for corporate research is extremely small. For several years, many state budgets have been running at large deficits and money for semiconductor corporate research is virtually non existent. Typically, state and local budgets depend on universities to partner with corporations to supply critical R&D funding. These forces put tight restrictions on how U.S. corporations spend R&D dollars - which are critical for developing new and diverse tools for the semiconductor industry and U.S. competitiveness.

National Funding:

2010's election results and increased attention on government spending clearly signals future pressure on R&D funding for all branches of the government. The high level of defense R&D spending (~66% of the federal total) may be among the first to be reduced. It is unclear if the NSF, NIH, NIST, and the DOE's Office of Science will be fully funded moving forward in the years 2011-2015. The R&D funded by government science and energy agencies directly affects U.S. competitiveness and economic growth.

Foreign Funding and Competition:

EU:

Foreign competition for semiconductor market share is fierce. Foreign governments realize that to be competitive in the global marketplace they must fund semiconductor corporate research and development. Recently[13] (2010), the European Commission has authorized the Netherlands to grant $15.6 million of soft loans and a direct grant of $5.7 million to Mapper Lithography B.V, for the development of E-beam lithography. The Commission found the aid to be compatible with the EU Framework for State aid for research, development and innovation because the research and development would not have been able to carry out this risky R&D-project without the aid. In particular, the aid addresses a specific failure of the private venture capital market and is limited to the necessary minimum. The Commission found that the private venture-capital market failed to provide sufficient financing for this risky, yet promising project.

The Commission further established that this lithography project is in line with European priorities, such as those defined by the European Union's R&D Framework Programs (FP), in particular the ICT-theme as well with the ENIAC Joint Technology, and the

EUREKA programs (CATRENE). The Commission therefore concluded that the positive effects of the aid outweigh any potential distortion of competition.

Asia:

Besides the EU, the U.S. faces an incredible uphill battle when competing with Asia for semiconductor manufacturing market share and government R&D sponsorship. The world is already well aware of the huge number of foreign semiconductor manufacturing facilities (now funded by many U.S. and EU companies).

Leading Asian nations recognize that their economic expansion can be sustained by continued commitment to R&D investment across a wide range of science and technologies. The scale and significance of research and development in Asia continues to grow, with implications for the rest of the world. Experienced researchers are becoming harder to find in the U.S. and Europe, as Asian emigrant scientists return to attractive opportunities at home. To take advantage of lower labor costs and larger pools of skilled scientists and engineers most countries are supporting substantial R&D facilities throughout Asia and they are directing increasing shares of R&D budgets overseas. Finally, funding and geographic dynamics in the R&D landscape are likely amplified by macroeconomic factors, such as the rate of innovation and balances of trade, with corresponding shifts in liquidity, affluence and advanced manufacturing. These factors will make it more difficult for the U.S. to maintain its historic lead in the development and economic leverage of innovation.

During the 2007-2010 recession, the Asian R&D communities and China specifically, increased their R&D investments[14]. As a Reuters headline noted, “While the world slashed R&D in a crisis, China innovated”. China entered the recession with a decade of strong economic growth. During that time, it increased R&D spending roughly 10% each year—a pace the country maintained during the 2008-2009 recession. This sustained commitment set China apart from many other nations.

R&D Importance to Industry and Nation

Semiconductor Diversity:

Competition between companies in the U.S. and the rest of the world has produced diverse solutions to difficult problems facing the semiconductor industry. This diversity in problem solving represents the backbone of the semiconductor industry. When an industry has a wide range of solutions for difficult problems, no single company can gain a monopoly on profit[15]. However, since corporate R&D spending is driven by the motivation to capture markets and gain maximum profits, R&D budgets are often reduced when solutions are thought to already exist. As R&D budgets tighten, corporations and universities seek partnerships with both consortia and government agencies to pool resources and tackle difficult problems. It is vital that NIST (through TIP) continues to help fund critical semiconductor R&D programs. The partners for this paper have suggested several critical areas for continued funding. These funds will help keep the U.S. a leader in global technologies.

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