Advanced Components for High Speed, High-MW Drives

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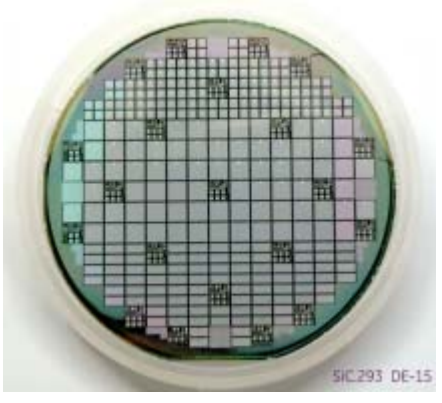

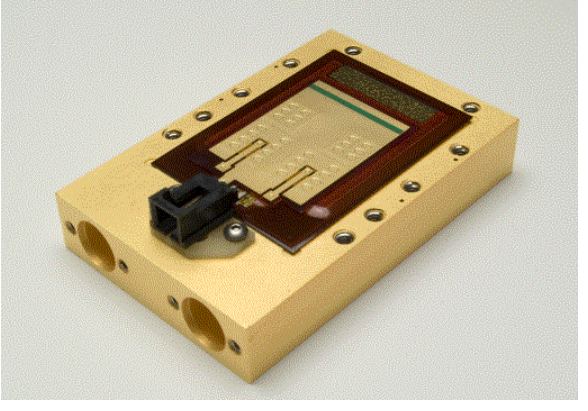

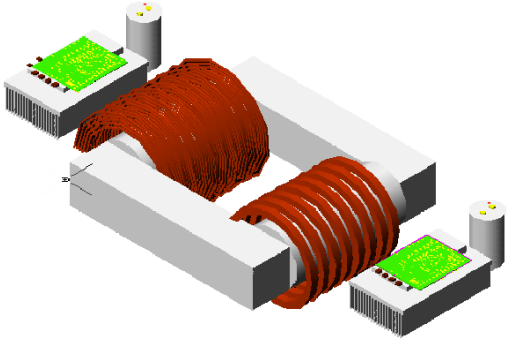

Presentation Outline

- SiC Power Devices
- SiC Power Packaging
- Magnetics
- Conclusions

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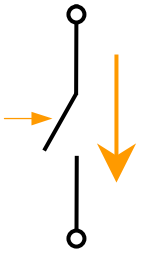
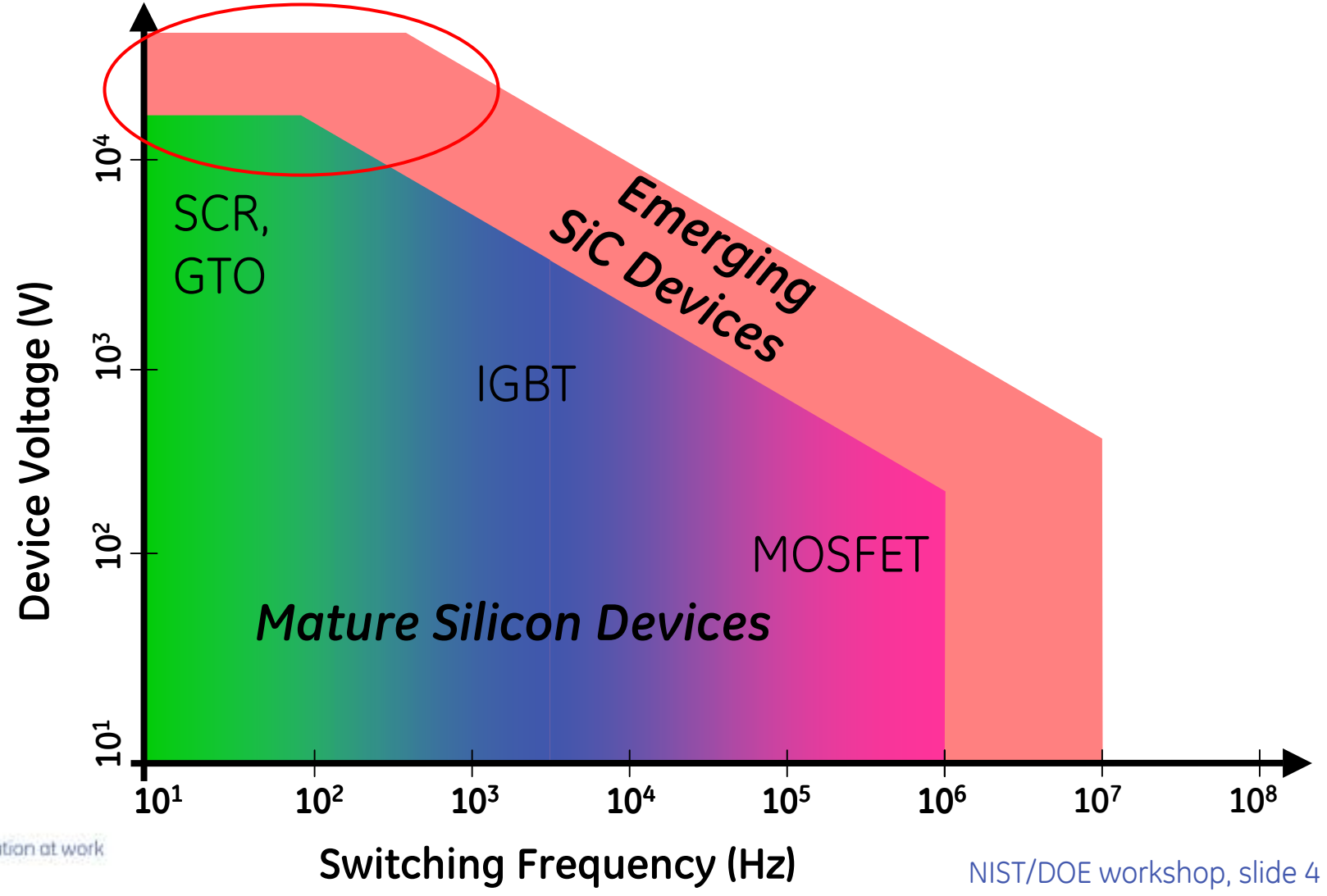
Semiconductor Power Devices

- SiC: fast high voltage devices that can operate at temperatures well above 200°C





DARPA HPE Phase III Program

DARPA/ONR Contract#: N00014-07-C-0415

Objective:

A 2.7 MVA, 13.8 kVac/ 465 Vac, solid-state transformer switching at 20 kHz

Features:

- 10 kV SiC power devices
- High voltage, 20 kHz magnetics
- Modular power converter architecture

Benefits:

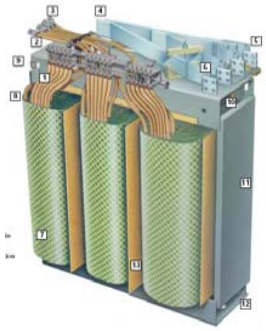
- Forty transformers on CVN-78 aircraft carrier; total estimated benefit: 172 tons, 292 m^3
- Fault-current limiting, improved power quality
- Flexibility, ability to supply both AC & DC loads

Partners:

- Cree, Inc.
- Powerex, Inc.
- General Dynamics Corp.
- Los Alamos National Lab.
- Virginia Tech, University of Wisconsin-Madison

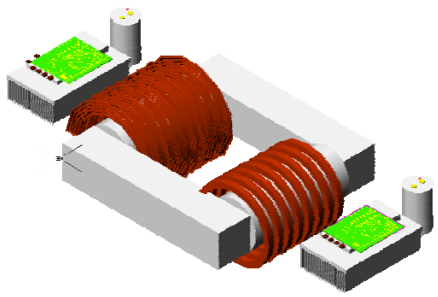
imagination at work

DARPA HPE Phase III Program



Low Frequency Conventional Transformer (analog)

- 2.7MVA
- 13.8kV/450V (Δ/Y) 60Hz
- **6 tons/each**
- **10 m³/each**
- **fixed, single output**



Estimated SiC-based Solid State Power Substation (digital)

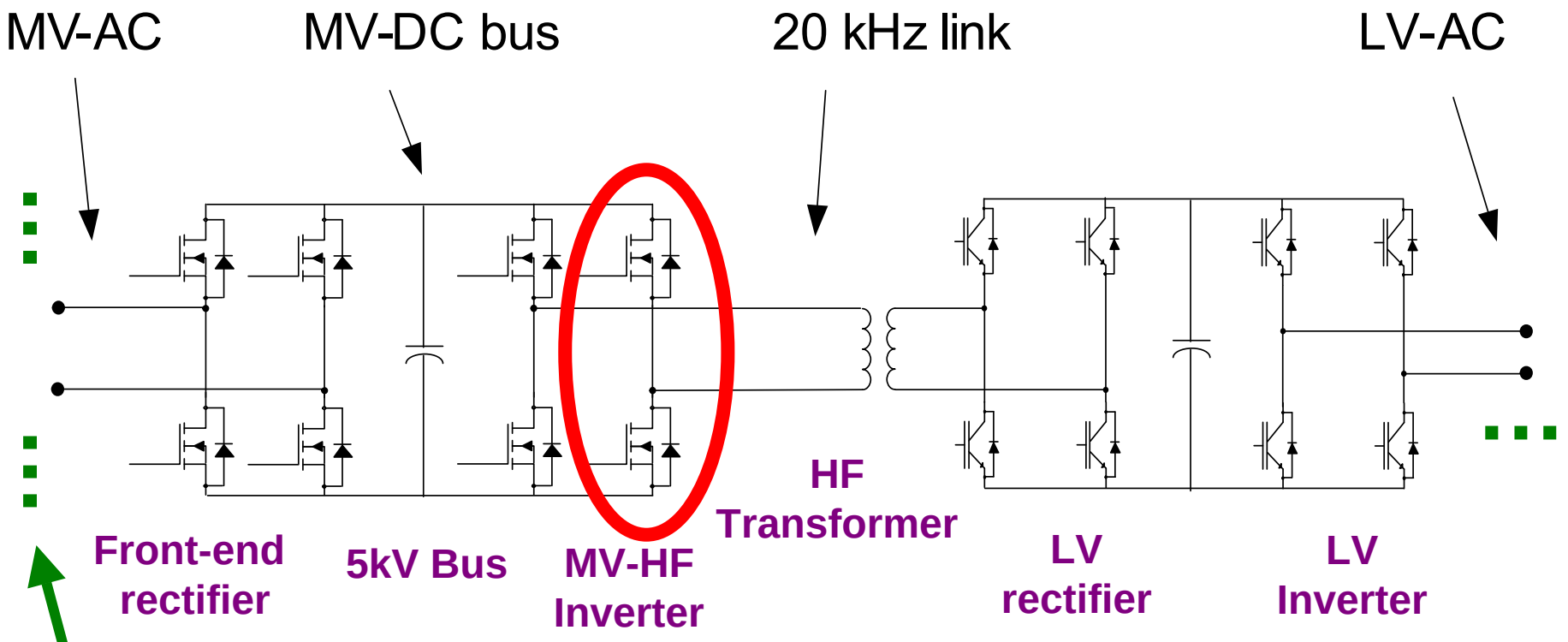
- 2.7 MVA
- 13.8kV/465V (Δ/Y) 20 kHz
- **1.7 tons/each**
- **2.7 m³/each**
- **multiple taps/outputs**

BENEFITS:

- **Reduction of weight and volume**
- **Precise voltage regulation to isolate voltage spikes, voltage dips**
- **Unity Power Factor (20% increase in power)**
- **Fast fault detection, protection, and potential removal of circuit breakers**

S. Beermann-Curtin, "Wide Bandgap Semiconductor Technology: High Power Electronics DARPA/PEO-Aircraft Carrier/ONR," HPE Phase3 industry-day, May 16, 2006, Washington, DC

System Integration for Representative SSPS Topology

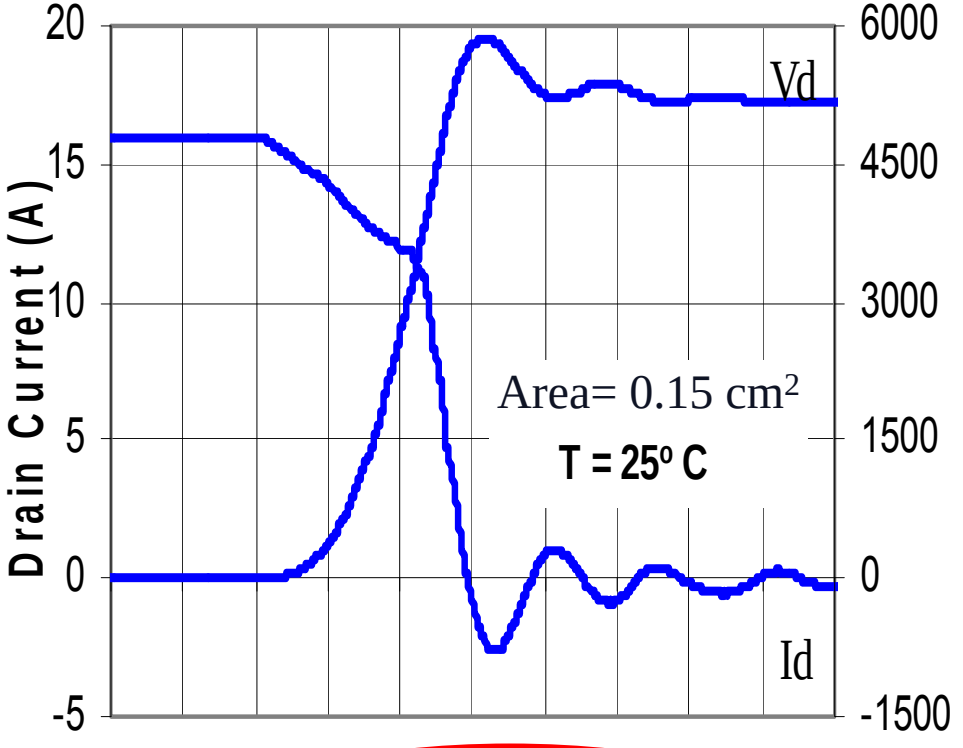


This configuration requires four series blocks for each phase of the 2.75 MVA, 13.8 kV to 465 V SSPS.

A. Hefner, "High-Voltage Isolated Gate Drive Circuit for 10 kV, 100 A SiC MOSFET/JBS Power Modules," presented at 2008 IAS Conference, Calgary, Canada.

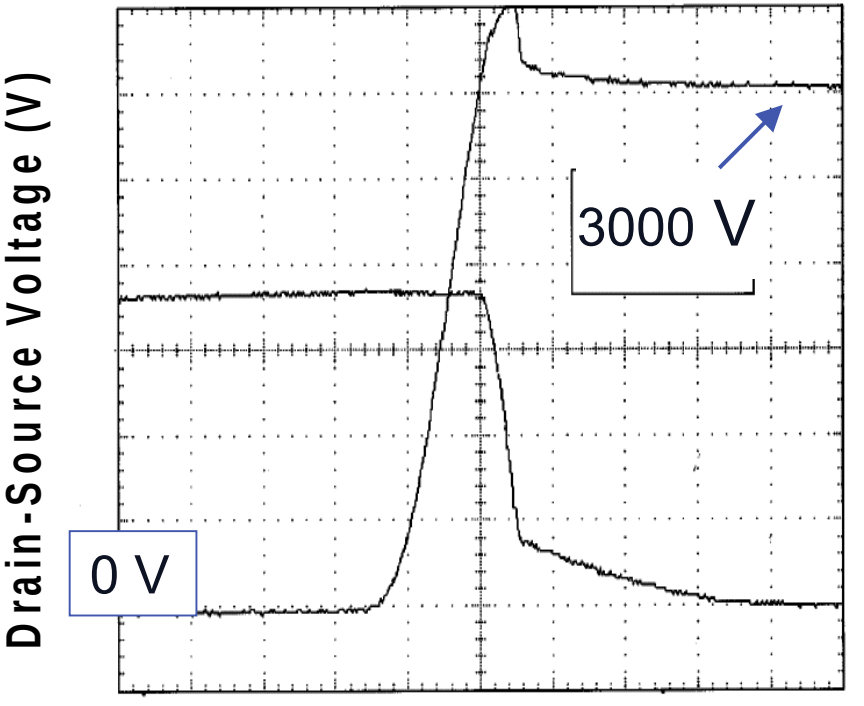
DARPA HPE MOSFET:
High Speed at High Voltage

SiC MOSFET: 10 kV, 30 ns



15 ns /div

Silicon IGBT: 4.5 kV, 2us



1us /div

A. Hefner, "Silicon-Carbide Power Devices for High-Voltage, High-Frequency Power Conversion Applications," HPE Phase3 industry-day, May 16, 2006, Washington, DC

SiC Device Requirements/Challenges

No commercially available 10 kV SiC devices

Requirements/challenges:

- Lowest losses at >10kV, ~1kHz

  V_{ON}(T) for majority carrier devices

- High current chips/modules

  Yield of large MOS-gated (MOSFET, IGBT) devices

- High reliability and stability over temperature, time

  Gate oxide reliability, stability

  Bipolar degradation

Need robust and reliable devices scaleable to >1 kA

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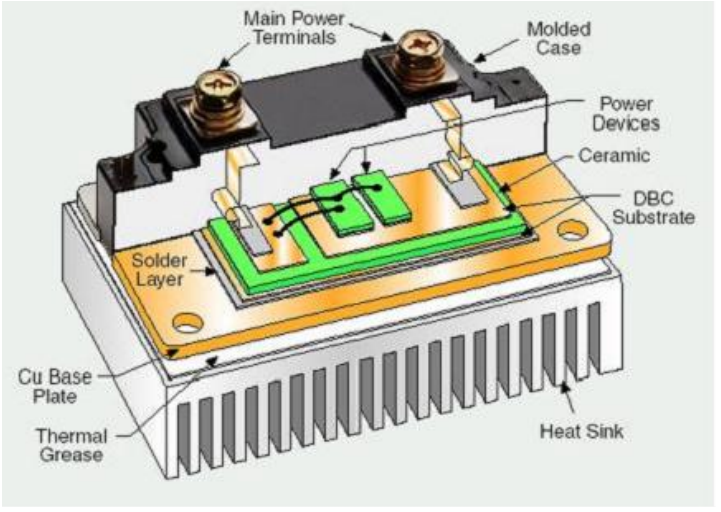
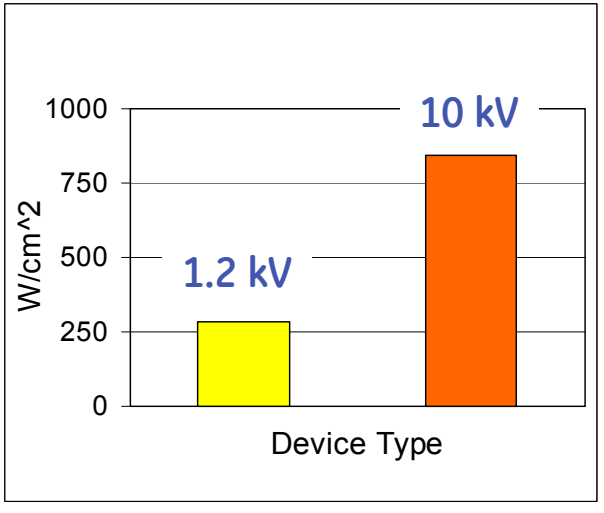
Power Module Challenges

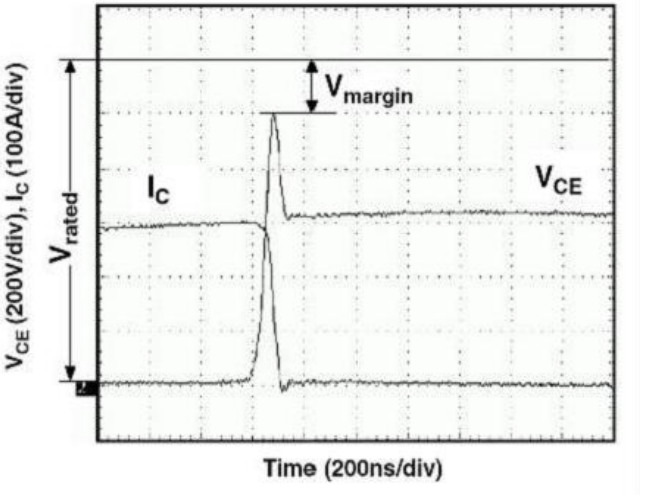


- Thermal limitations
- Electrical de-rating
- Wirebond reliability

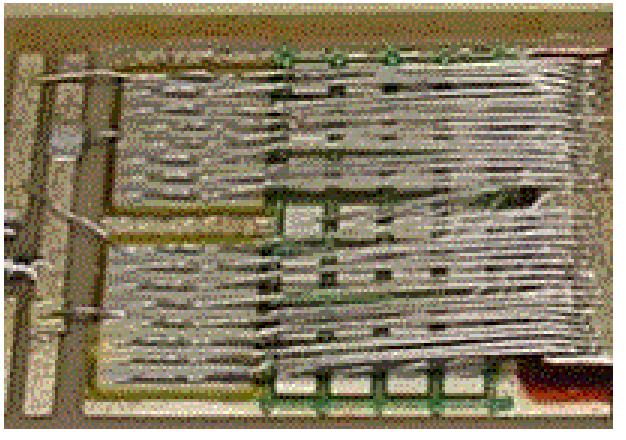
Power Loss Density



Parasitic Inductance



Wirebond Reliability



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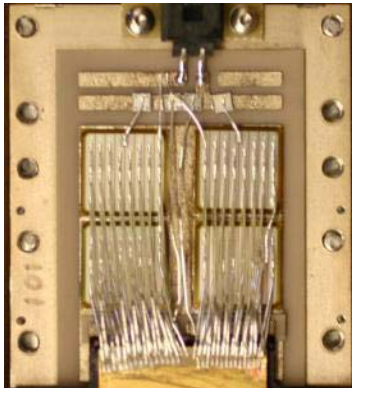
Module Thermal Study

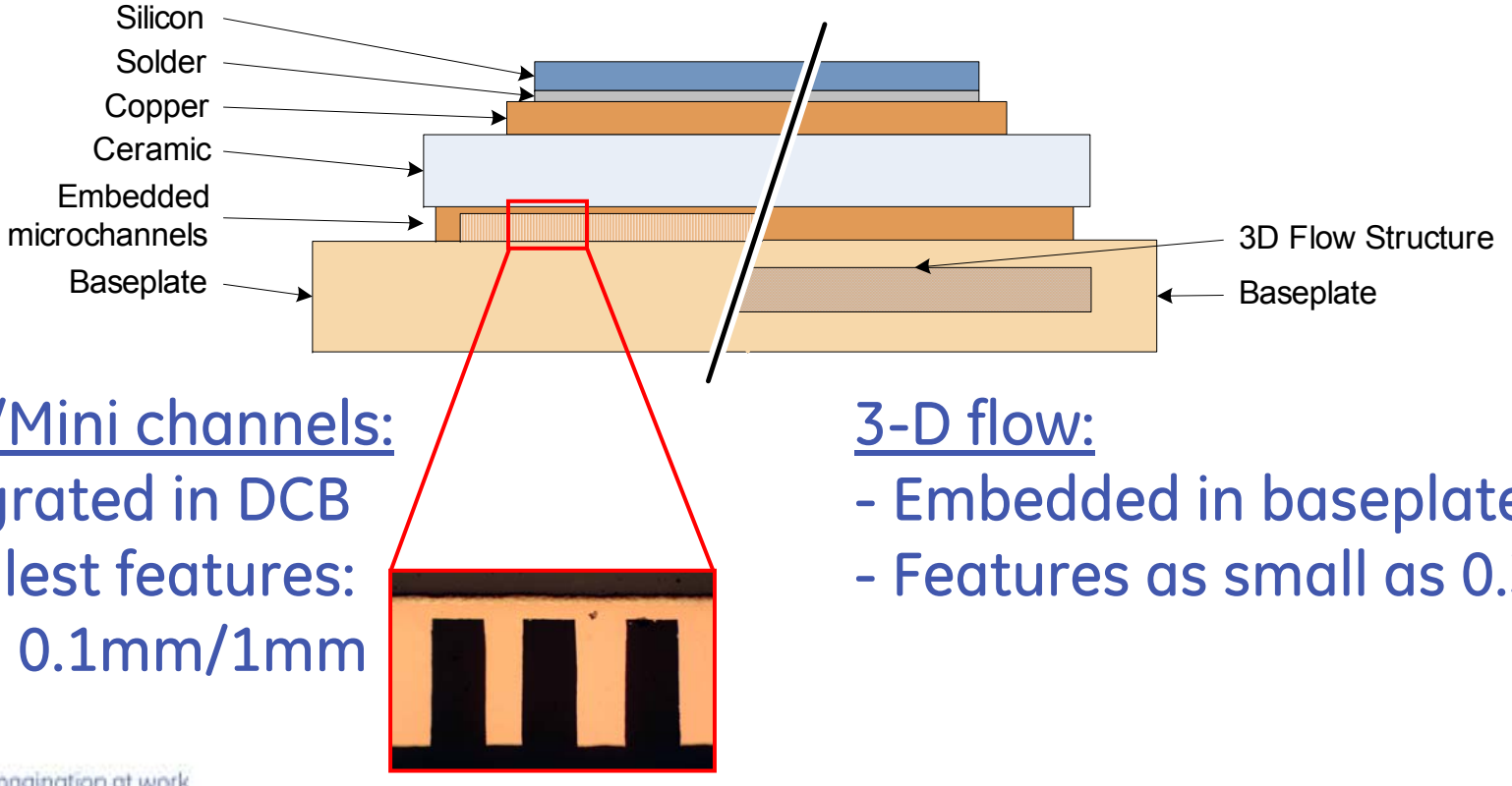
Test heatsinks:

4x150A IGBTs

Same layout, same DCB (AlN)

Three heatsinks: 3-D flow, Micro-/Mini-channels





Micro/Mini channels:

- Integrated in DCB
- Smallest features: 0.1mm/1mm

3-D flow:

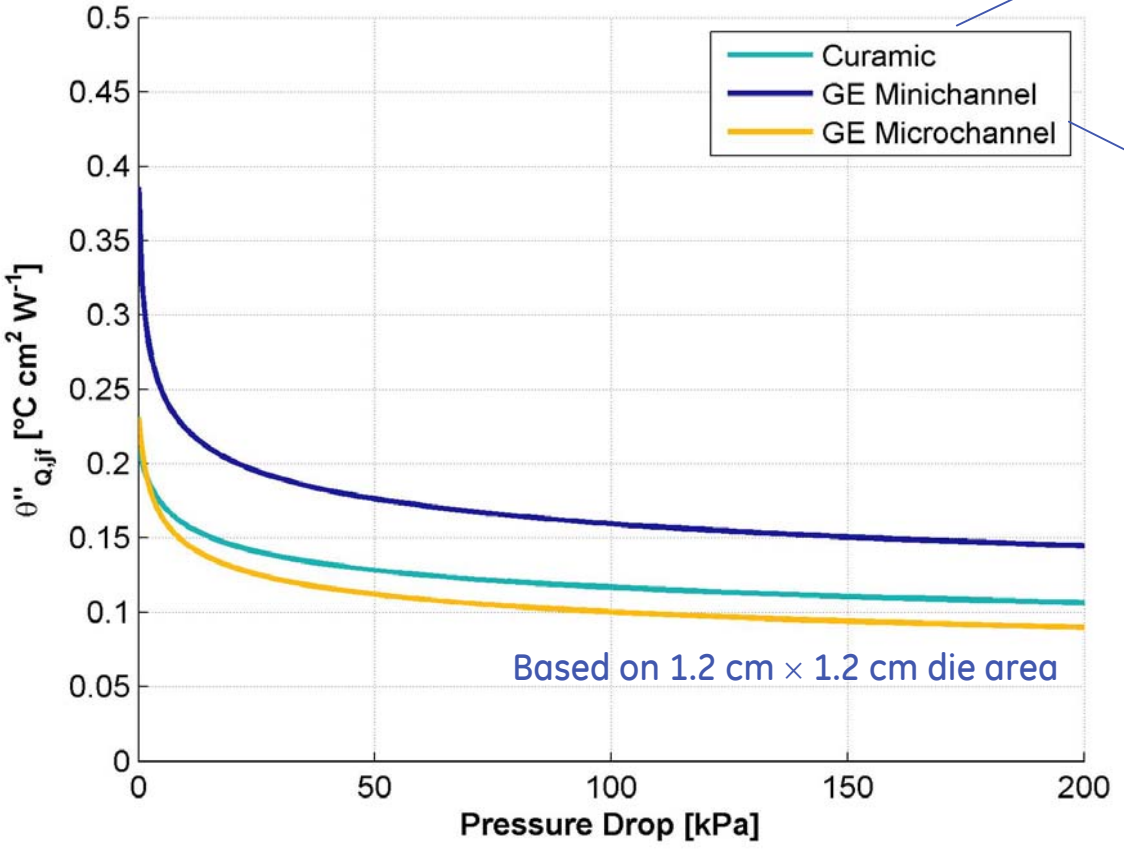
- Embedded in baseplate
- Features as small as 0.3mm

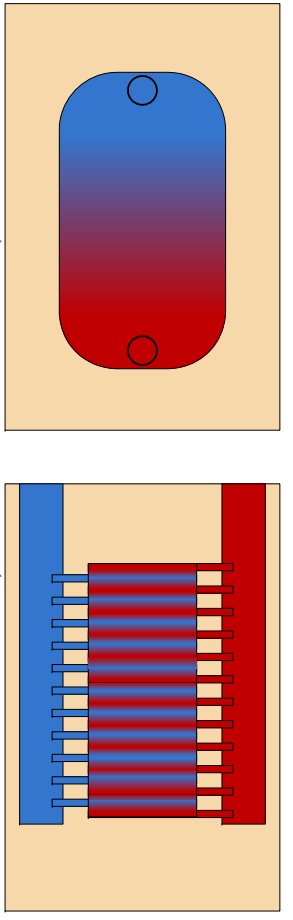
ARL Contract#: W911NF-04-2-0045

Module Thermal Study

Micro-channel offers best performance:

- High ratio of surface area to fluid volume
- Short channel length → lower ΔP





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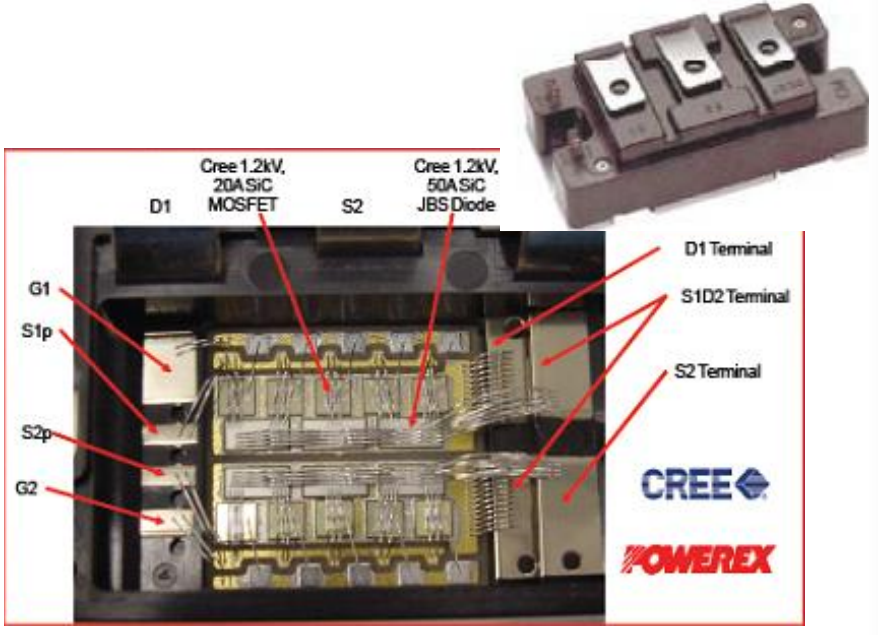
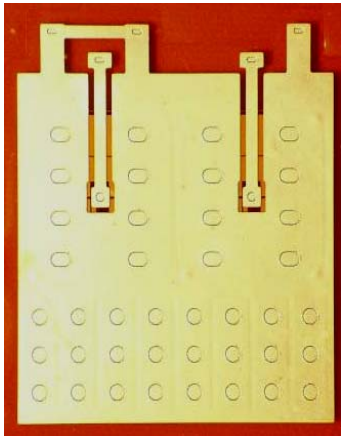
Power Module Roadmap

Conventional Wirebonded



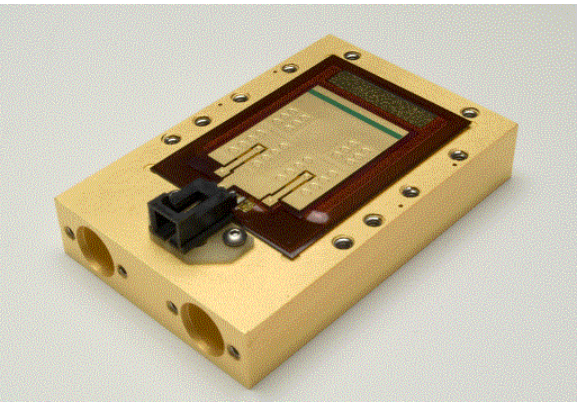
Advanced Wirebondless



Advantages of Wirebondless Module

- Higher power density
- Reduced package thickness and area
- Interconnect many devices using artwork
- Different via sizes as needed without change in process
- Less parasitic L (better current sharing, switching loss)
- Lower contact resistance (lower conduction loss)
- Planar interconnect enables top-side cooling
- Higher surge current capability

GE Power Overlay - POL



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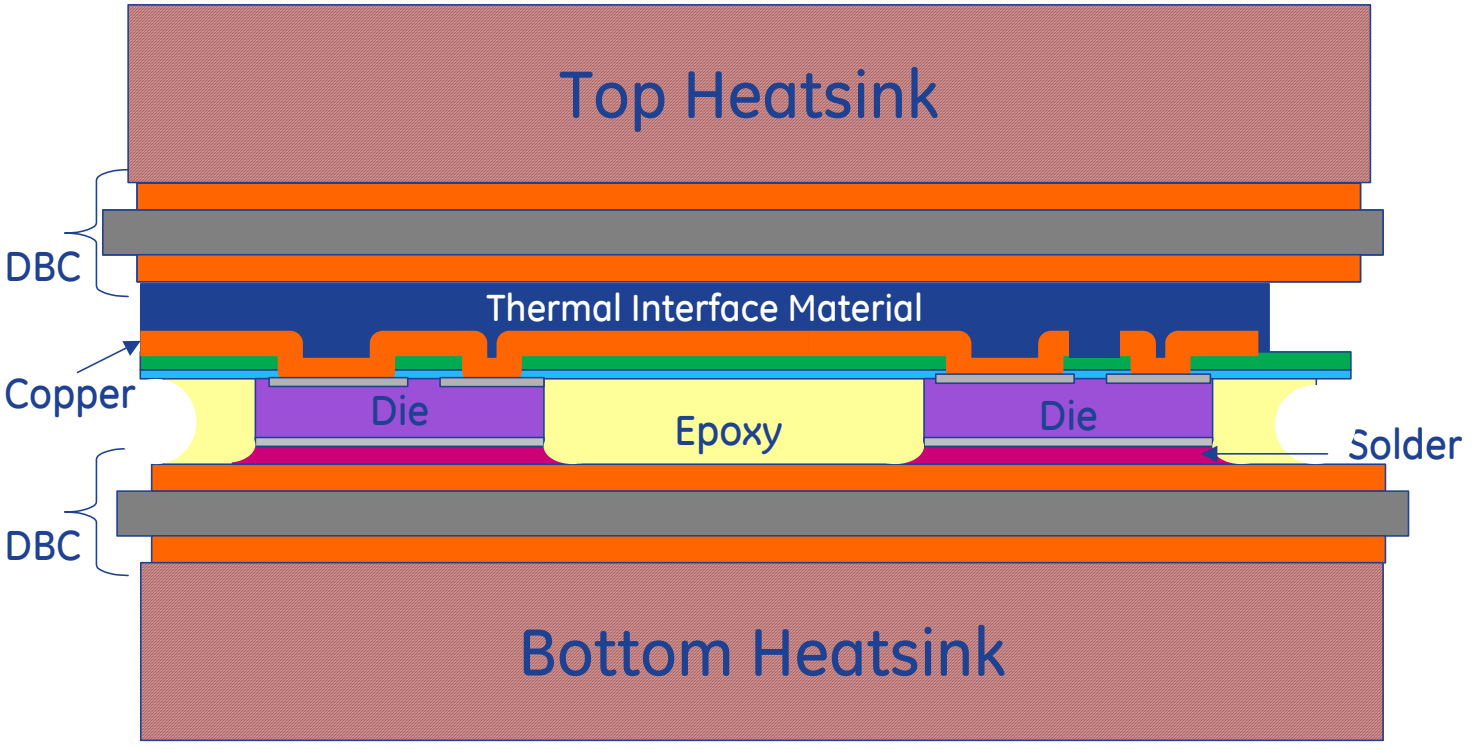
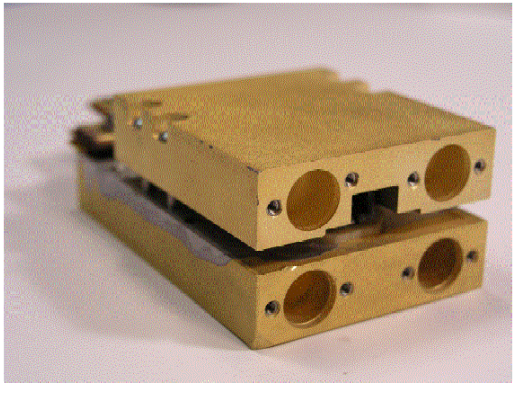
Double-sided Cooling



Not to Scale

Improvement from top-side heatsink:

15-30% with water-based microchannel, up to 40% with P.G.



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Power Module Requirements/Challenges

No commercially available >10 kV, >1 kA modules

Requirements/challenges:

- High reliability

  Device interconnect for high currents & temp's

  Materials CTE matching

- Topology requirements for module failure modes

  Fault tolerant to open/short failure

- Thermal performance

  High performance (top & bottom) device cooling

Need advanced packaging to maximize benefits of SiC

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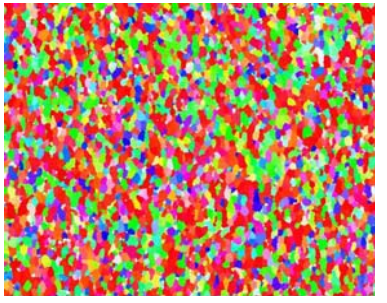
New Soft Magnetic Materials

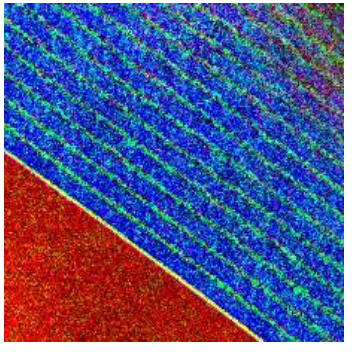
Minimize hysteretic losses

- New alloy compositions (amorphous & crystalline)
- Novel nanostructures to reduce coercivity



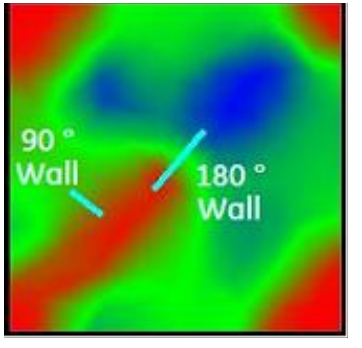
Minimize eddy current losses

- New material geometries enabled by advanced material processing techniques
- Enable wide range of operating frequencies



Maximize materials utilization

- Maintain balance of properties
  - High saturation magnetization (1.5 – 2.0 T)
  - Operating temperature (> 300 °C)



New Magnetic Materials R&D/Investment Needs

Alloy design

- Advance alloy theory and modeling to impact:
  - Saturation magnetization -> Increase power density
  - Anisotropy -> reduce power loss
  - Magnetostriction -> reduce power loss
- **Good opportunity for University partnerships**

Material Characterization

- Apply advanced magnetic and structural probes to magnetic materials
- **Leverage metrology facilities at NIST and National Labs**

Material processing

- Develop new process routes to achieve desired microstructures
- Validate material performance in pilot-scale processing
- **Utilize National Lab facilities (e.g. Oak Ridge, Ames)**
- **Good opportunity for public/private collaboration to mitigate risk**

Summary

No commercially available SiC devices for >10 kV,

Need robust and reliable devices scaleable to >1 kA

No commercially available >10 kV, >1 kA modules

Advanced packaging to maximize benefits of SiC

Need high efficiency, B_{SAT}, temp magnetic materials

Questions?