CHARACTERIZATION CHALLENGES IN THE 28 NM NODE

Prof. Dr. Hubert Lakner

2015 International Conference on Frontiers of Characterization and Metrology for Nanoelectronics

Fraunhofer
IPMS

CNT - CENTER NANOELECTRONIC TECHNOLOGIES

Joseph von Fraunhofer (1787 – 1826)

© Deutsches Museum

Researcher

➔ Discovery of the “Fraunhofer lines” in the solar spectrum

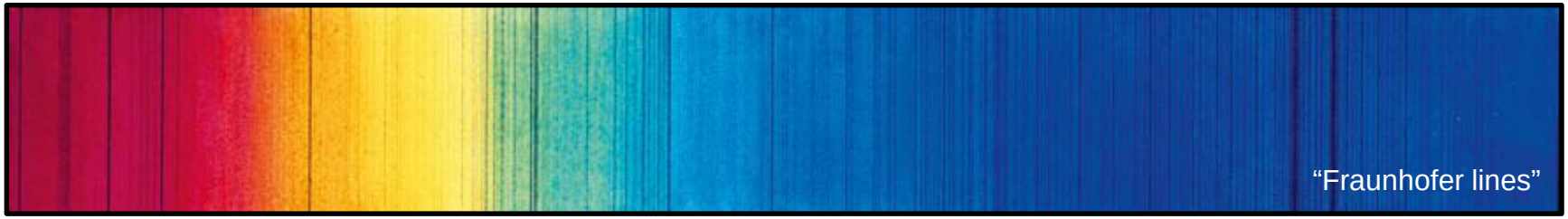
Inventor

➔ New methods for processing lenses

Entrepreneur

➔ Director and partner in a glassworks

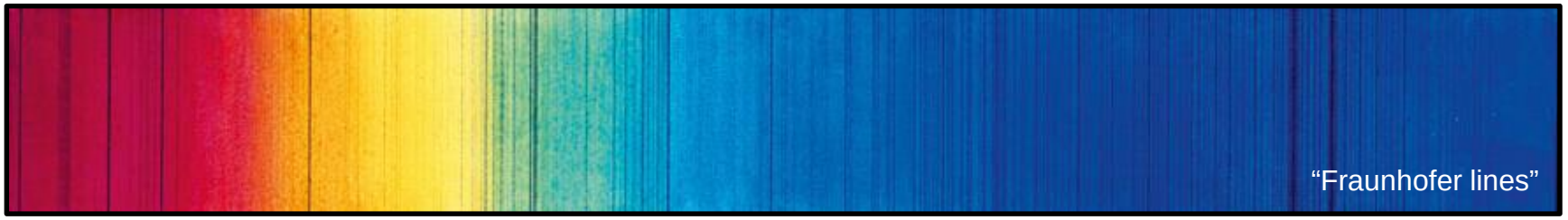
© Fraunhofer-Gesellschaft



Fraunhofer-Gesellschaft, the largest organization for applied research in Europe

- 67 institutes and research units
- More than 23,000 staff
- EURO 2 billion annual research budget.

  - 2/3 of this sum is generated through contract research on behalf of industry and publicly funded research projects.
  - 1/3 is contributed by the German federal and *Länder* governments in the form of base funding.

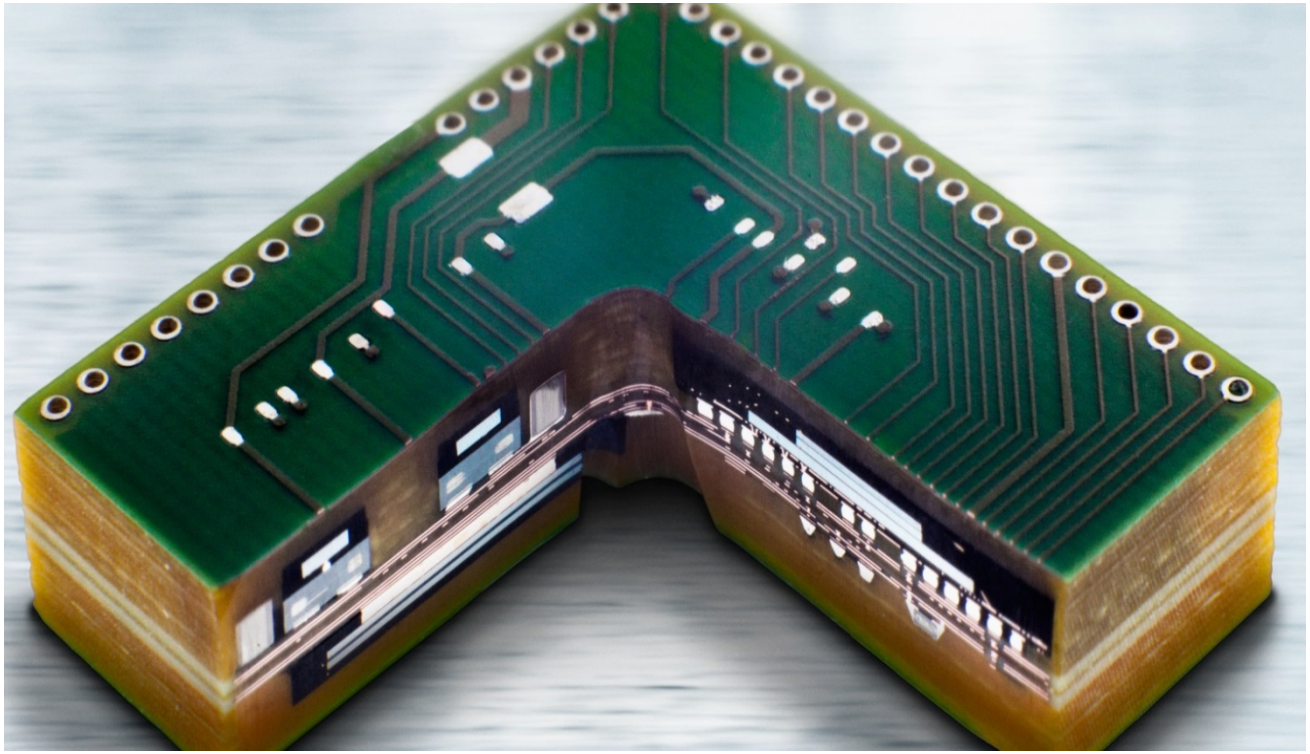


Fraunhofer Groups

- ICT Group
- Group for Life Sciences
- Group for Light & Surfaces
- **Group for Microelectronics**
- Group for Production
- Group for Materials and Components – MATERIALS
- Group for Defense and Security VVS

Fraunhofer Group for Microelectronics

- We make the Invisible



Fraunhofer MIKROELEKTRONIK

Fraunhofer Microelectronics – a leading European R&D service provider for smart systems

Facts and Figures

- 11 Member institutes:
  EMFT, ENAS, FHR, HHI, IAF, IIS, IISB, IMS, IPMS, ISIT, IZM
- 5 Guests from other Fraunhofer Groups (ICT Group and MATERIALS):
  ESK, FOKUS, IDMT, IKTS, IZFP
- Founded in 1996

- Chairman: Prof. Hubert Lakner
- Deputy chair: Prof. Anton Grabmaier
- Business office in Berlin

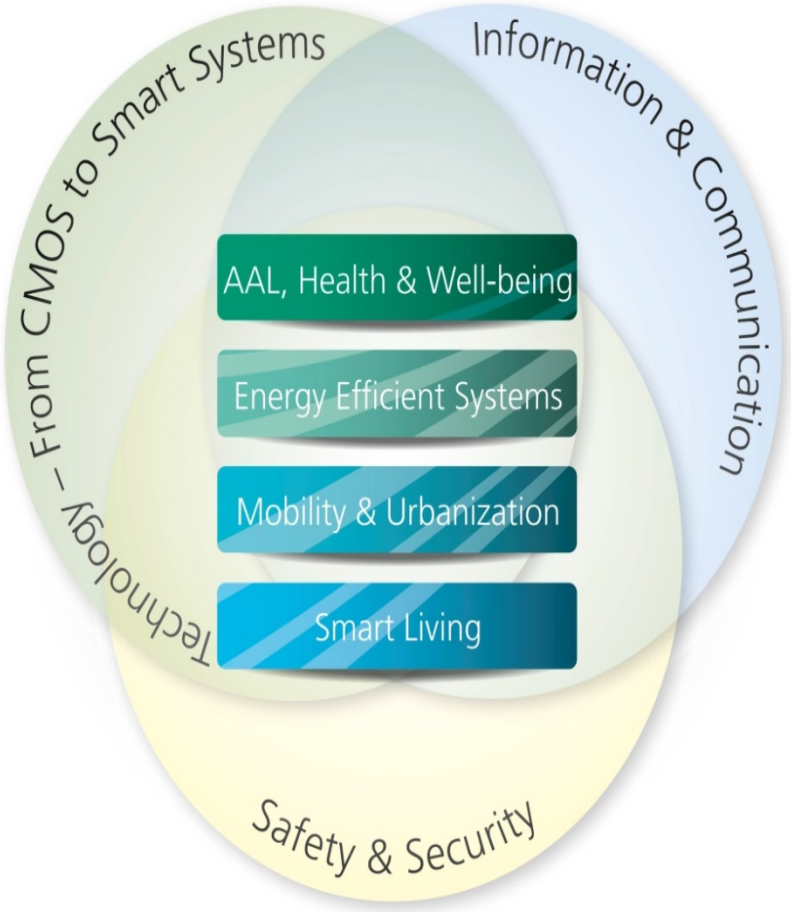
- Budget: 345 Mio € (2014)
- Revenue: 311 Mio €
  - Industry: 207 Mio € (61%)
- More than 3,000 employees
- Cleanrooms at 8 institutes

- R&D service provider for smart systems integration:
  microelectronics, nanoelectronics, power electronics and microsystem technologies

Technology-oriented cross-cutting areas provide the essential basics for our customers‘ applications

Technology-oriented Business Areas

- Technology: From CMOS to Smart Systems
- Information and Communication
- Safety and Security



Cross-institute technological core competences allow long-term coverage of the entire value chain

Strategic Alignment

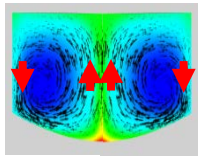
- Design for Smart Systems
- Semiconductor-based Technologies: Silicon, SiC, GaN
- Power Electronics and System Technologies for Energy Supply
- Sensors and Sensorsystems
- System Integration Technologies
- Quality and Reliability
- RF and Communication Technologies

We support specific needs of our customers in various forms of cooperation

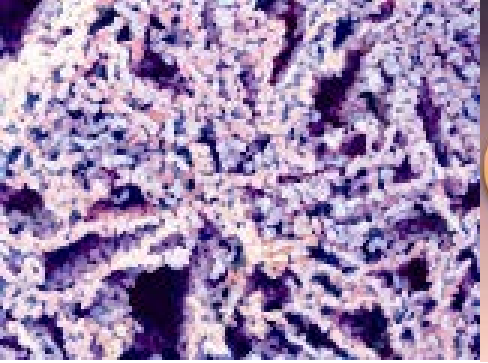
- Industrial Contract Research
  - R&D projects, feasibility studies, technology & process development
- Services for Industry
  - demonstrators, prototypes, technology service, equipment, personnel
- Technology Transfer
  - technologies and processes, licensing
- Strategic Alliances
  - public-private-partnerships, joint labs, manufacturing lines with industry
- Cooperative Projects
  - funded jointly by public & industrial sources e.g. Federal Ministry of Education & Research, Federal States, EU
- Applied Basic Research
  - with institutes and universities

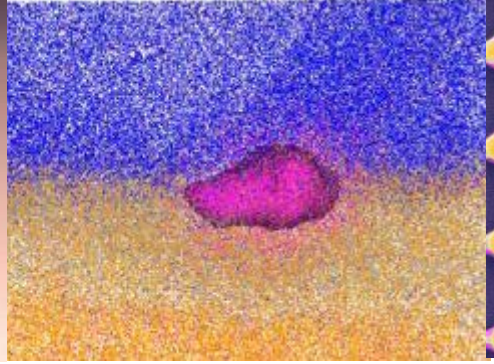
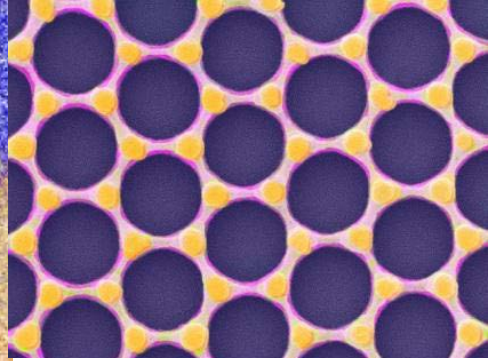
We offer a strong network for effective implementation of research objectives to our customers

Memberships (exemplary)



- Close cooperation at European level with Leti (FR), CSEM (CH) and VTT (FI) in the **HTA** (**H**eterogeneous **T**echnology **A**lliance)
- Member of the largest European microelectronics-organizations
  - **CATRENE** (**C**luster for **A**pplication and **T**echnology **R**esearch in **E**urope on **N**ano**E**lectronics)
  - **EURIPIDES²** Member (The Smart Electronics Systems Cluster)
  - **ECSEL** Member (**E**lectronic **C**omponents and **S**ystems for **E**uropean **L**eadership)
    - **AENEAS** (**A**ssociation for **E**uropean **N**ano**E**lectronics **A**ctivitie**S**)
    - **ARTEMIS-IA**(**A**dvanced **R**esearch & **T**echnology for **EM**bedded **I**ntelligence and **S**ystems **I**ndustry **A**ssociation)
    - **EPoSS** (**E**uropean Technology **P**latform **o**n **S**mart **S**ystems Integration)
- **ESIA** Member (**E**uropean **S**emiconductor **I**ndustries **A**ssociation)
- **ISA** Member (**I**nternational **S**olid State Lighting **A**lliance)
- **SEMI** Member (**S**emiconductor **E**quipment and **M**aterials **I**nternational)
- Participation in the **ITRS** (**I**nternational **T**echnology **R**oadmap for **S**emiconductors)



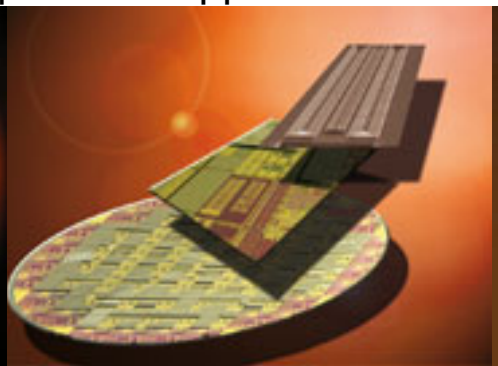
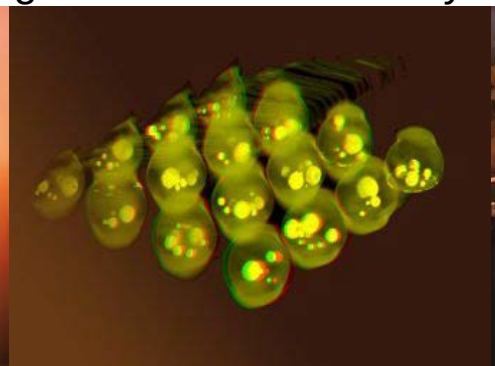



Dresden Fraunhofer Cluster Nanoanalysis – DFCNA

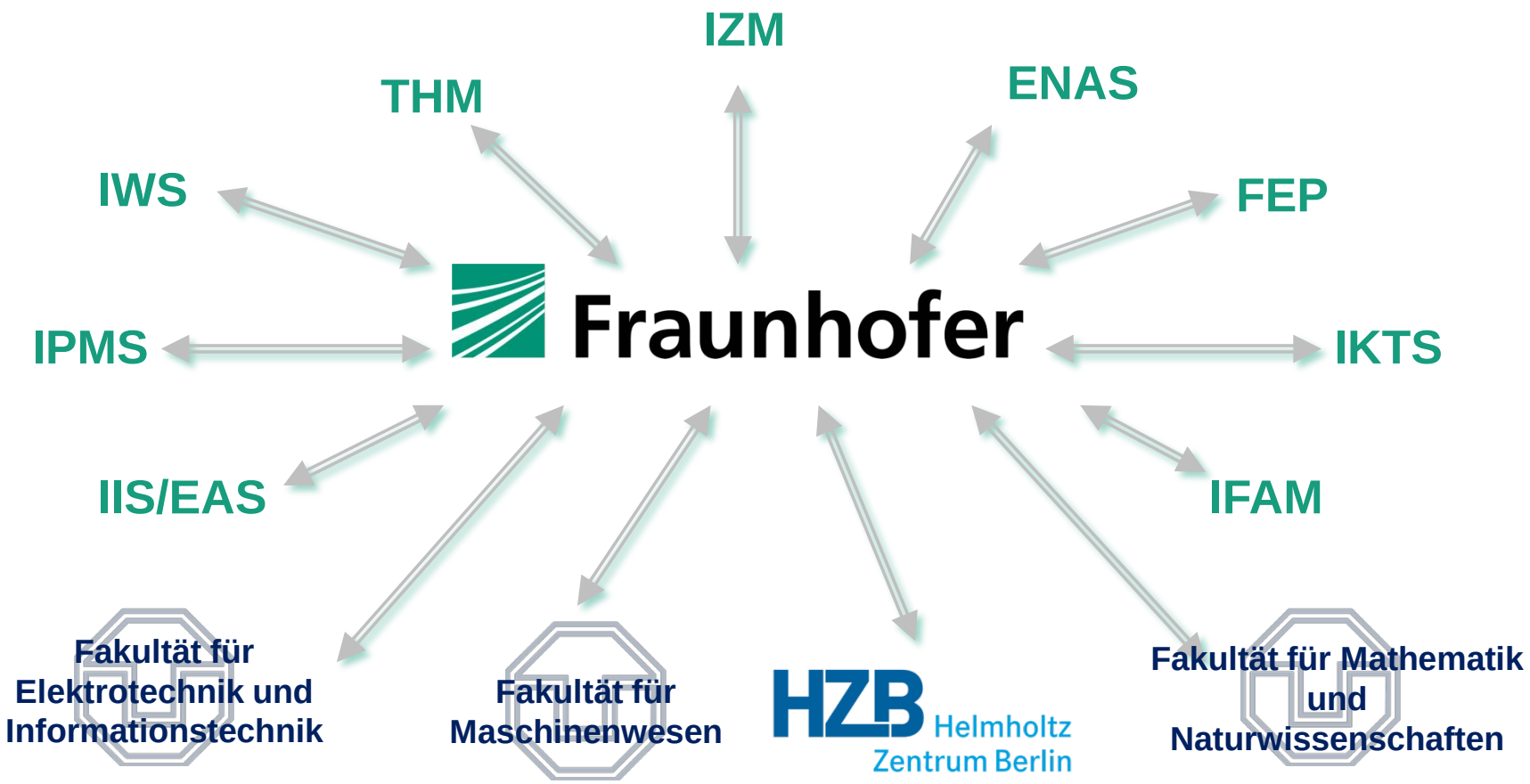
Vision Establish an internationally visible competence center for nanoanalysis as recognized partner for industry

Mission Applied research and development in the field of nanoanalysis for discovering suitable technical and conceptual solutions:

- Advancement of analysis methods
- Consultation and accomplishment of services in the field of analysis
- Development of components and systems for new analysis techniques
- Development of application strategies for advanced analysis methods


Dresdner Fraunhofer-Cluster Nanoanalytik



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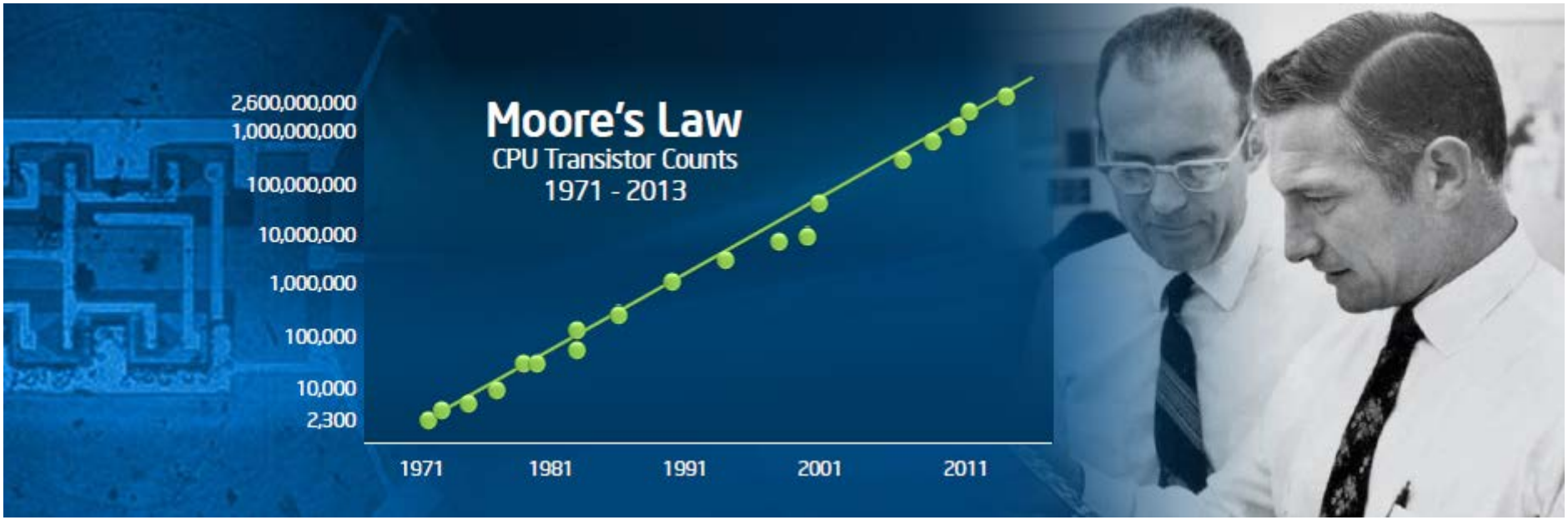
Outline

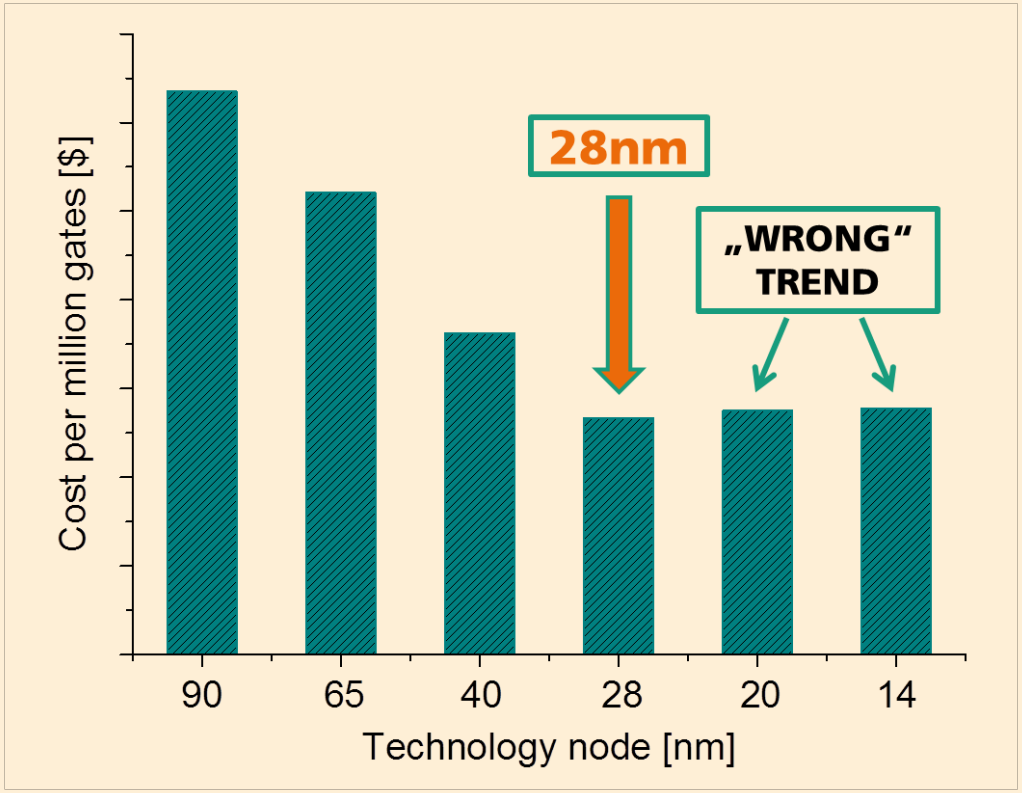
- The End of Moore‘s Law?
- 28nm as „golden node“
- Characterization challenges at 28nm
- Example – Defect passivation by fluorine interface treatments within the gate stack
- Summary

Gordon E. Moore: The number of transistors on a chip doubles roughly every two years.



Renee James IDF 2013 Keynote on New Era of Integrated Computing.

Challenges to Moore‘s law scaling



No cost /transistor crossover for the first time at the transition from 28nm → 20nm node

Due to:

Lithography (multi patterning, EUV)

high impact of minor process variations

- 28nm technology is now mainstream node for many applications
- Conversion from 28nm to 20/14nm may not be attractive for manufacturers

T. Werner, Industrial Partner Day CNT 2014

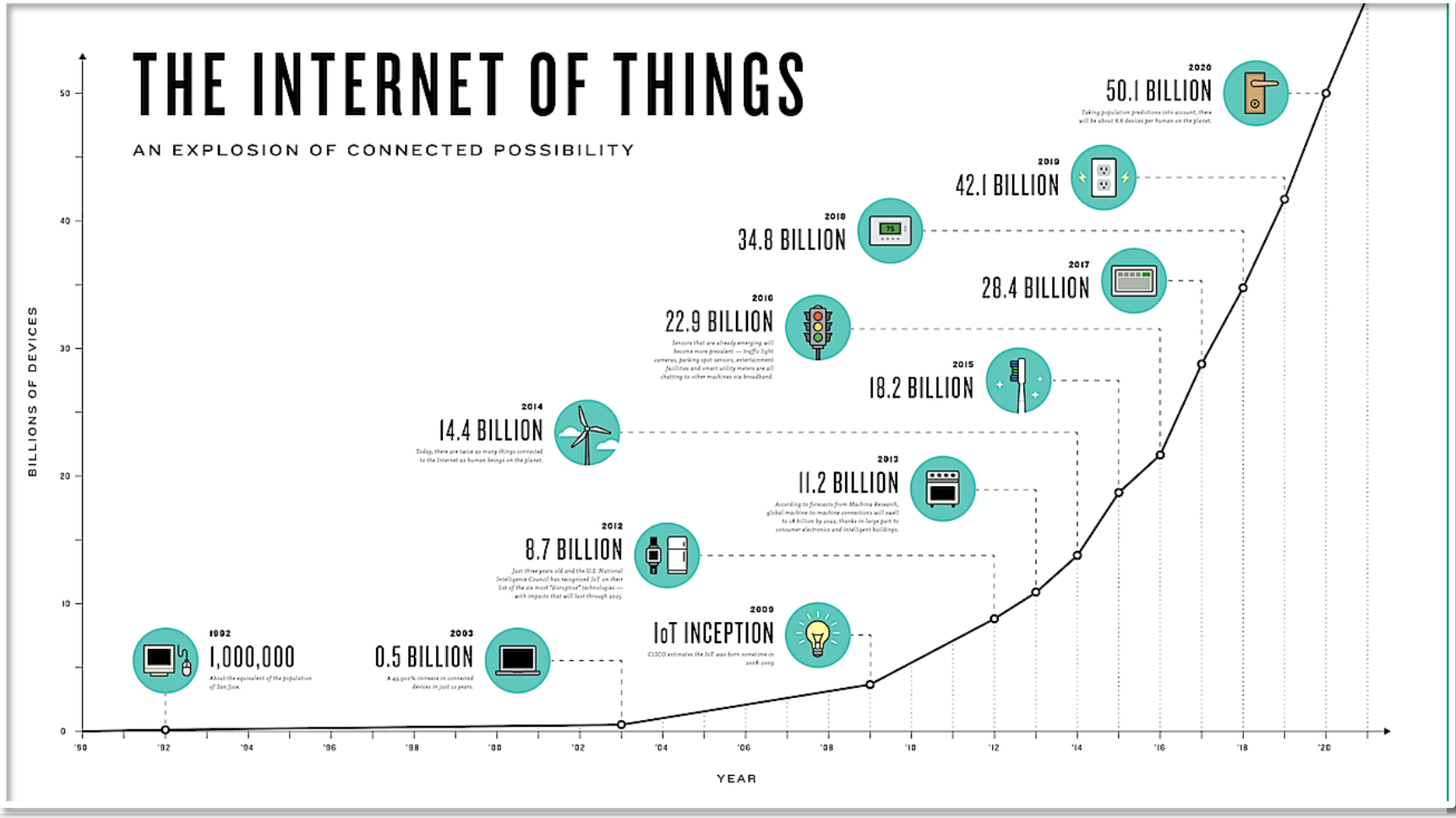
28nm as a „golden node“?

- Wally Rhines (CEO of Mentor Graphics):
  - „28nm is a golden node with respect to cost vs. die size / performance“

- High costs in further nodes e.g. due to extremely advanced litho (double patterning) and integration of FinFETs

Whally Rhines (CEO of Mentor Graphics) discusses the end of Moore‘s Law at the Future World Symposium 2014

Internet of Things (IoT) requires a high volume of cheap devices.

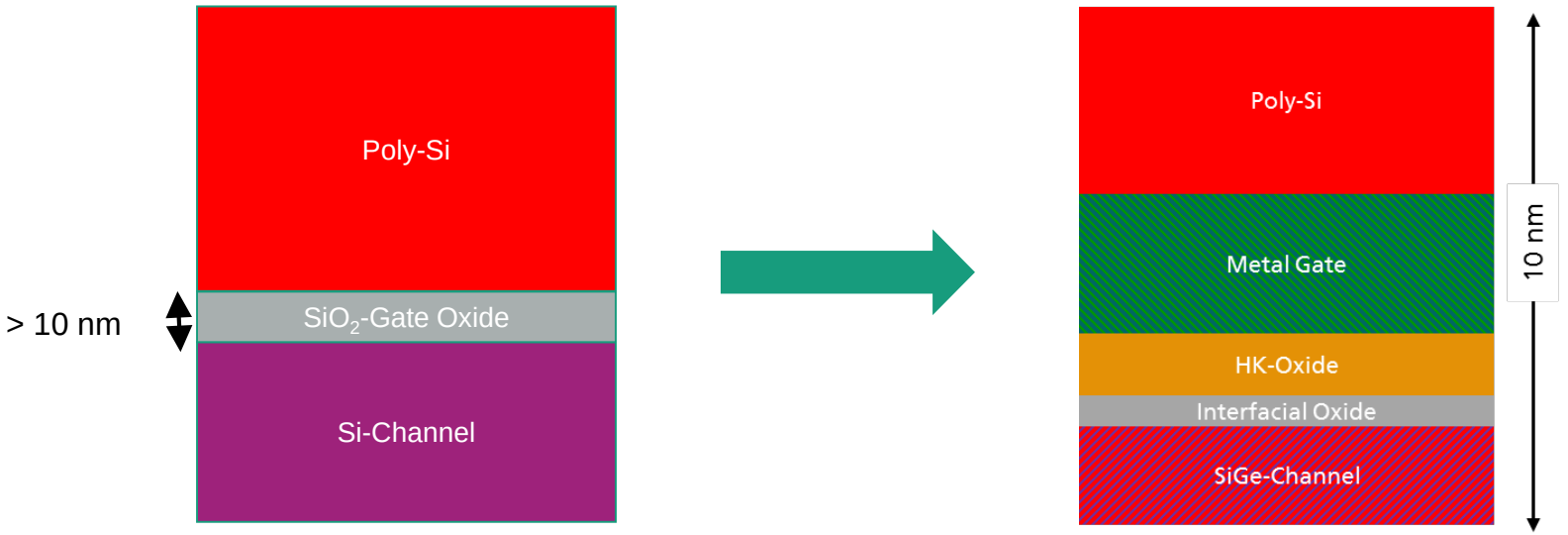


The Connectivist (Cisco)

What is special about the 28nm node?

Implementation of the high-κ / metal gate technology

- Replacement of the „conventional“ gate stack



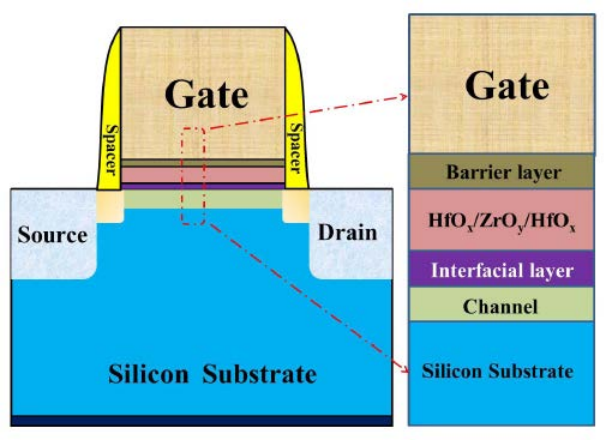
0.8µm node (90’s)

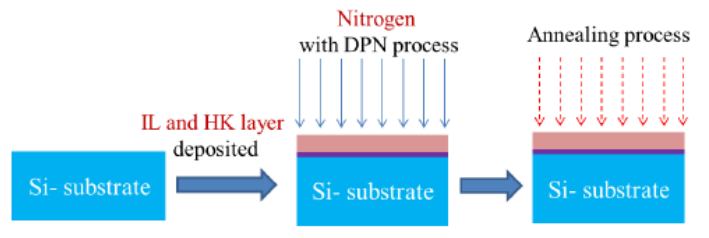
28nm node (today)

Metrology challenges concerning the high-**k** / metal gate technology *using Hf based oxides*

Metrology challenges concerning the high-**κ** / metal gate technology *using Hf based oxides*

- Nitrogen concentration in high-κ dielectrics

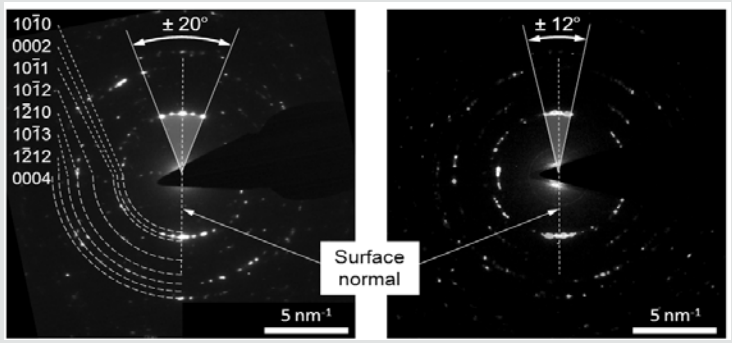


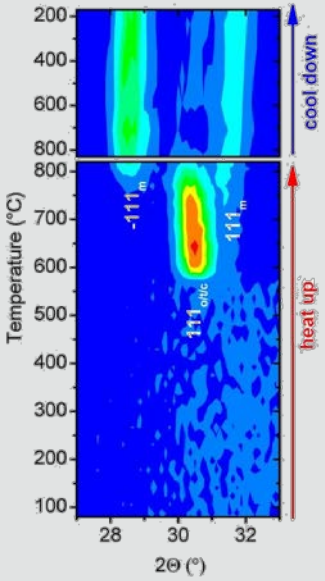


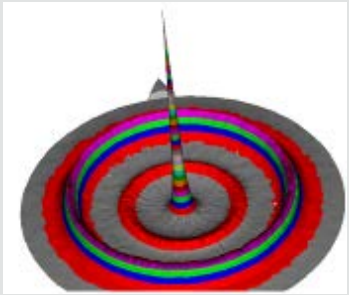
IEEE Trans. On Plasma Science, Vol. 42, No. 12, Dec. 2014

Metrology challenges concerning the high-**κ** / metal gate technology *using Hf based oxides*

- Nitrogen concentration in high-κ dielectrics
- Nano-crystalline film structure (phase and texture)







Metrology challenges concerning the high-**κ** / metal gate technology *using Hf based oxides*

- Nitrogen concentration in high-κ dielectrics
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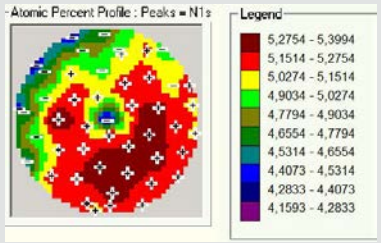
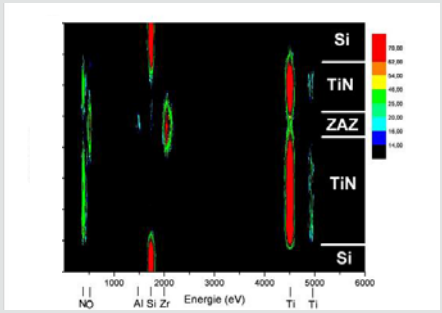
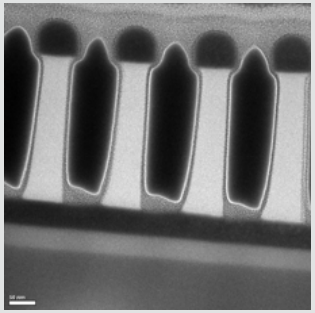
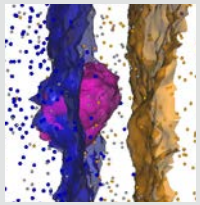
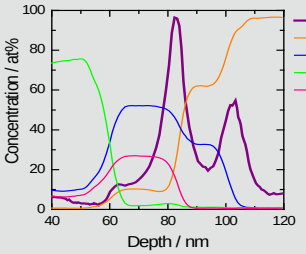
- Composition of work function adjusting films

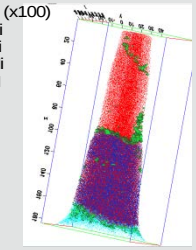












Metrology challenges concerning the high-**κ** / metal gate technology *using Hf based oxides*

- Nitrogen concentration in high-κ dielectrics
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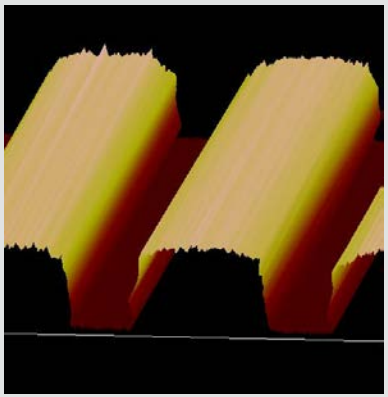
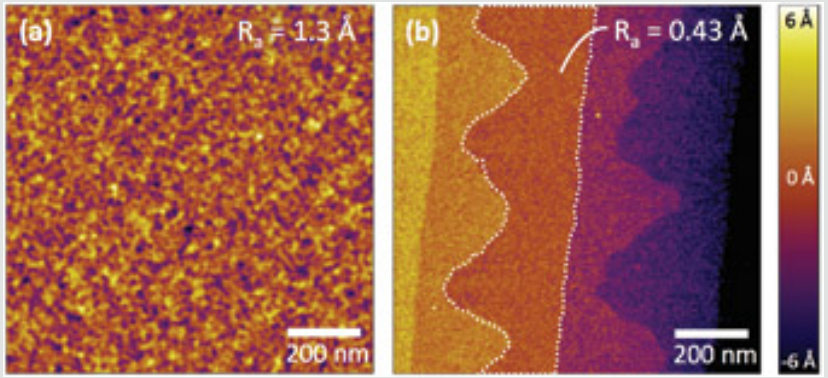
- Composition of work function adjusting films
- Nanoscale roughness in the same dimension as film thickness





Measuring Surface Roughness with Atomic Force Microscopy, Asylum Research

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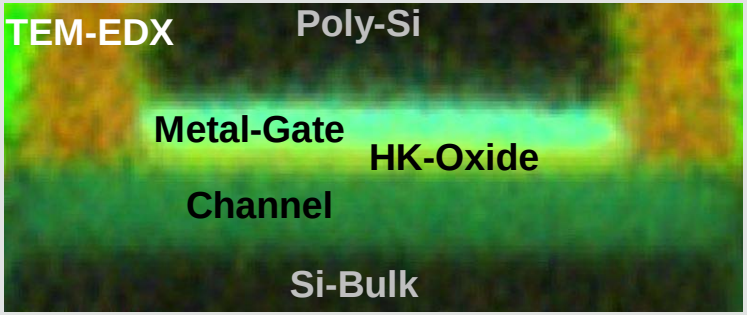

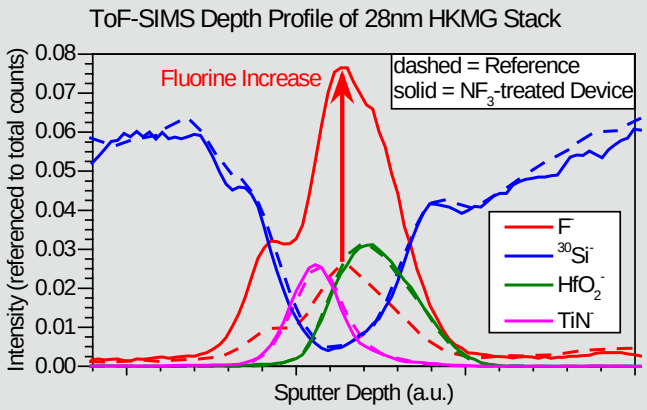

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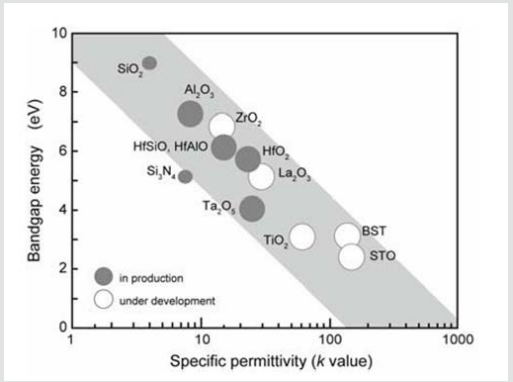
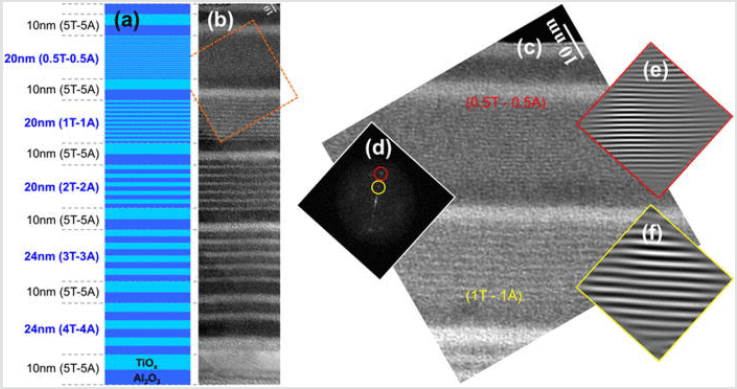
- Nitrogen concentration in high-κ dielectrics
- Nano-crystalline film structure (phase and texture)
- Composition of work function adjusting films
- Nanoscale roughness in the same dimension as film thickness
- Materials characterization of annealed gate stacks
- Mixed high-κ dielectric or even ultra-thin layers high-κ laminates



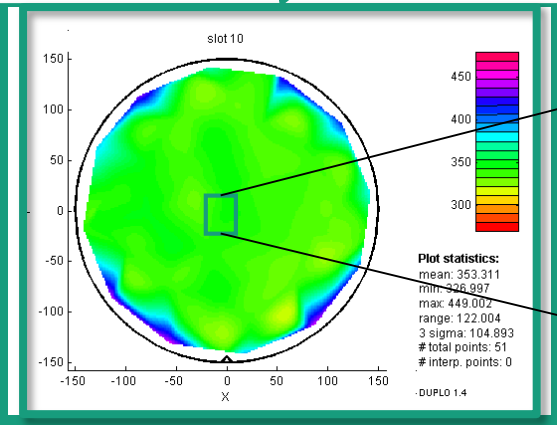
Dimension Increase in Metal-Oxide-Semiconductor Memories and Transistors, Hideo Sunami

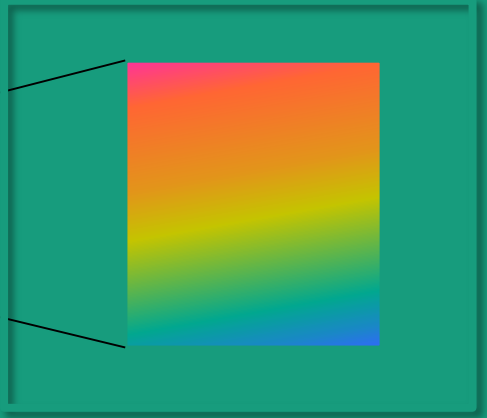


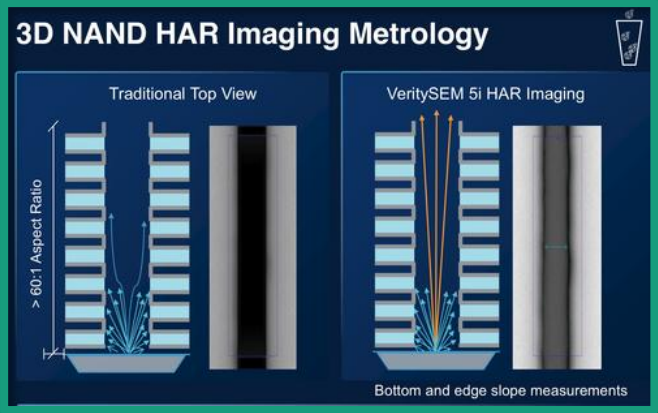
Tailoring dielectric relaxation in ultra-thin high-dielectric constant nanolaminates for nanoelectronics Appl. Phys. Lett. 102, 142901 (2013)

In-Lab vs. IN-FAB

- For in-fab metrology it‘s necessary to map nanometer-scale material properties and other critical functions:
  - over the wafer in-die and on complex 3D structures (e.g. FinFETs)







APPLIED MATERIALS

In-Lab vs. IN-FAB

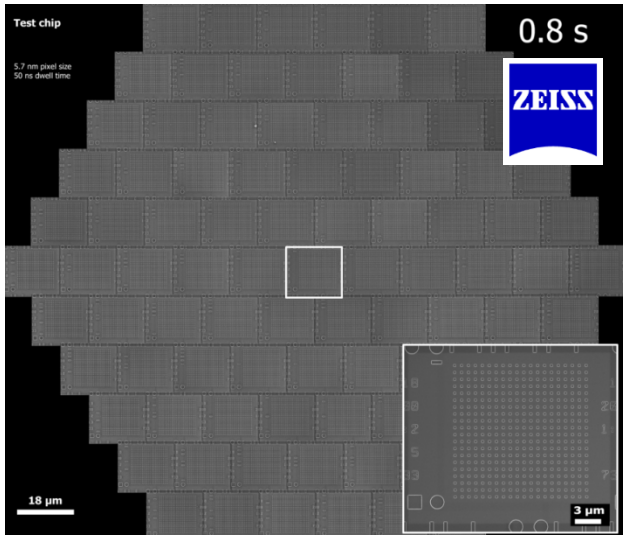
New tool development for cost-effectiveness in-fab characterization

Zeiss MultiSEM505

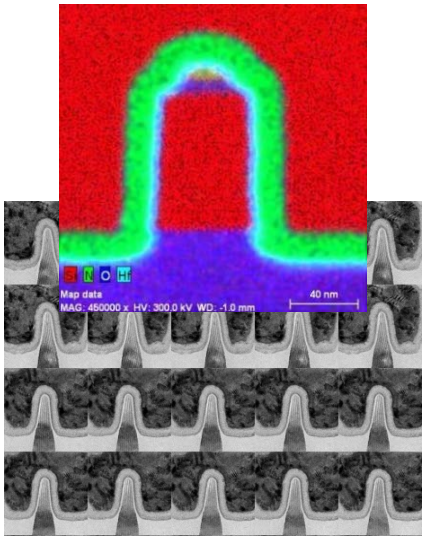
Non-destructive

Wafer scale to feature scale

Fast measurement



High volume TEM data



4 minutes: high-speed EDX elemental map taken on a SEMATECH FinFET sample

In-Lab vs. In-Fab

- Characterization of materials at nanoscale requires high resolution imaging and spectroscopy → time and cost consuming processes
- Need for speed of process optimization under industrial conditions
- BUT

The combination of speed and high resolution imaging and spectroscopy is one major frontier in the characterization of nanoelectronics.

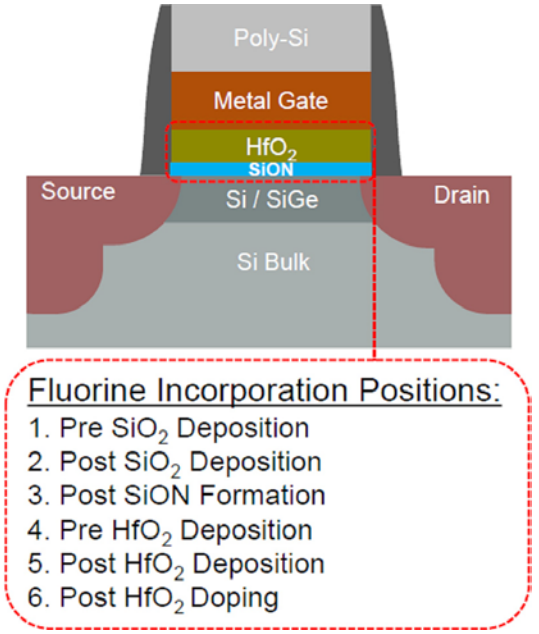
Example – Fluorine interface treatments within the gate stack for defect passivation in 28nm high-**κ** / metal gate technology

[1] M. Drescher et al., J. Vac. Sci. Technol. B **33**(2), 022204, Mar/Apr 2015

Example – Fluorine interface treatments within the gate stack for defect passivation in 28nm high-κ / metal gate technology

- High-κ gate dielectrics enable device scaling, but introduce device reliability challenges due to interface and bulk defects
- Fluorine is known to passivate defect states and to improve device reliability
- Complexity of high high-κ metal gate stack demands comprehensive characterization of fluorine-treatment to understand interaction with device parameters

HKMG stack schematic depicting individual fluorine treatment positions during the CMOS process flow.

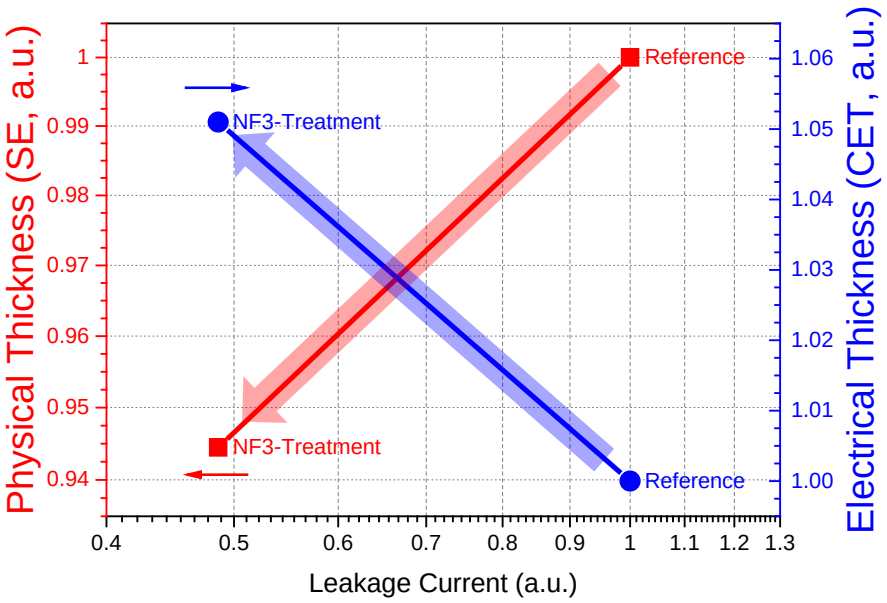


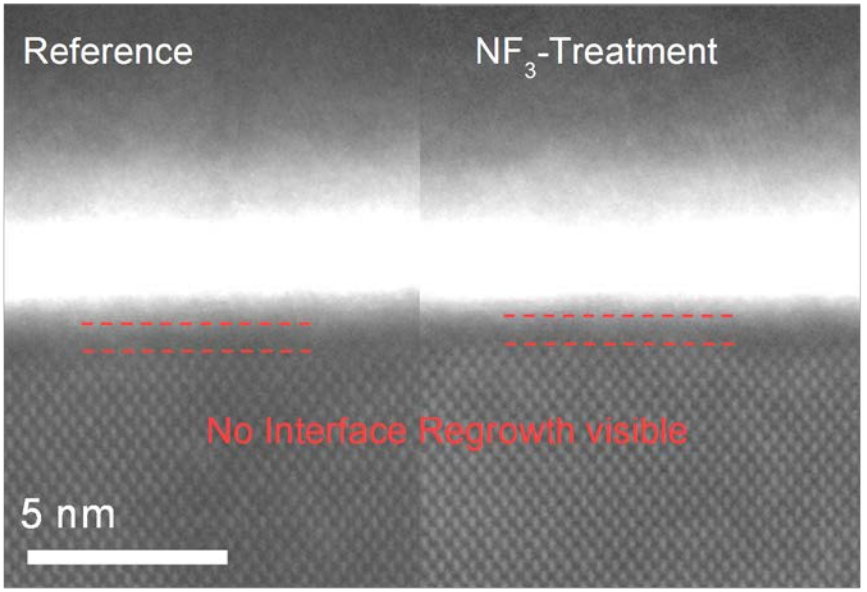
[1] M. Drescher et al., J. Vac. Sci. Technol. B **33**(2), 022204, Mar/Apr 2015

Example – Physical vs. Electrical characterization

- Physical metrology does not reflect changes in gate oxide sufficiently

Physical vs. Electrical Thickness Characterization



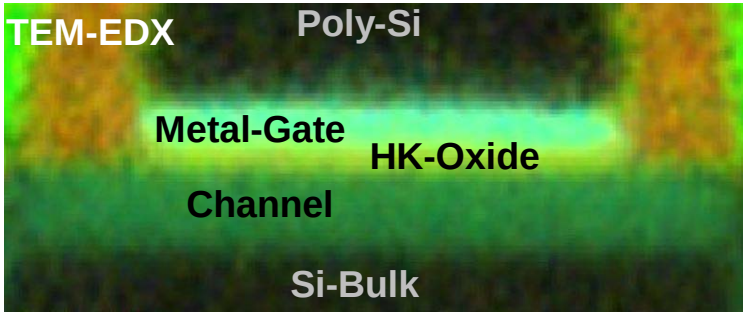


[1] M. Drescher et al., J. Vac. Sci. Technol. B **33**(2), 022204, Mar/Apr 2015

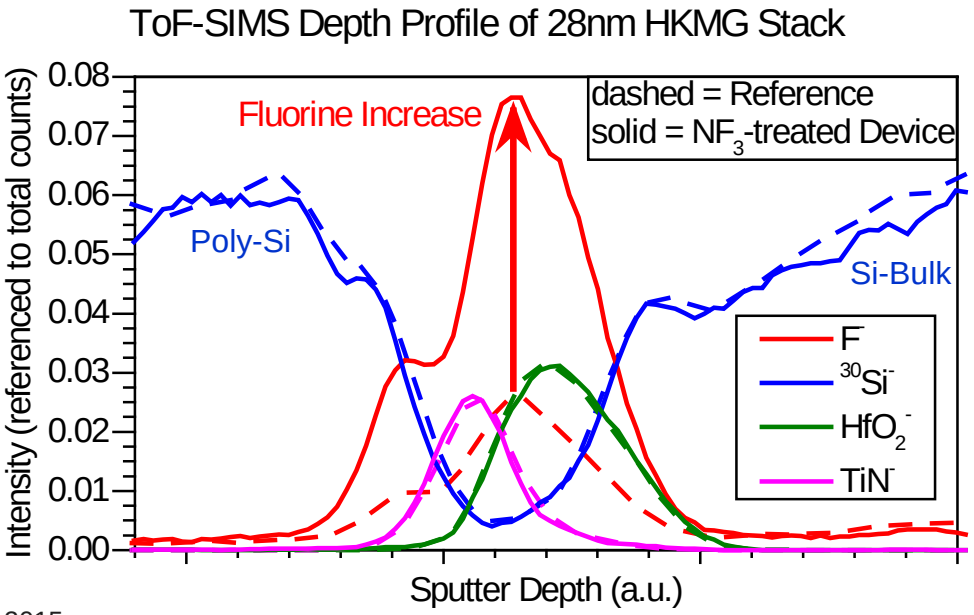
Example – Limits of characterization methods

- The detection of impurities within complex gate stacks is challenging as detection limits might not be sufficiently low enough.

  → TEM-EDX cannot detect fluorine in gate stack, ToF-SIMS can however the exact positions of fluorine within the gate stack remain unclear



Fluorine not detectable with TEM-EDX



[1] M. Drescher et al., J. Vac. Sci. Technol. B **33**(2), 022204, Mar/Apr 2015

Resolving gate stack is possible but at which effort?

- Advanced electron microscopy techniques are capable of resolving the 28nm gate stack layers and detecting impurities in the material
- Sample preparation time and cost have to be taken into account in order to find a balance between the needs of the industry and the efforts put in the analysis.

Qualcomm NMOS

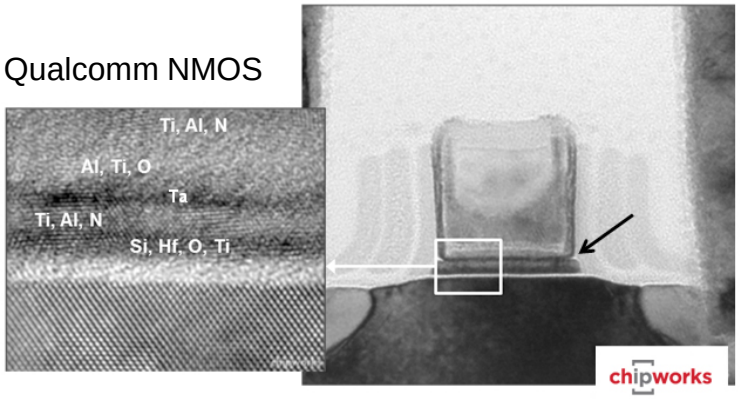


Figure 1 NMOS Transistor in Qualcomm Snapdragon 800

Qualcomm PMOS

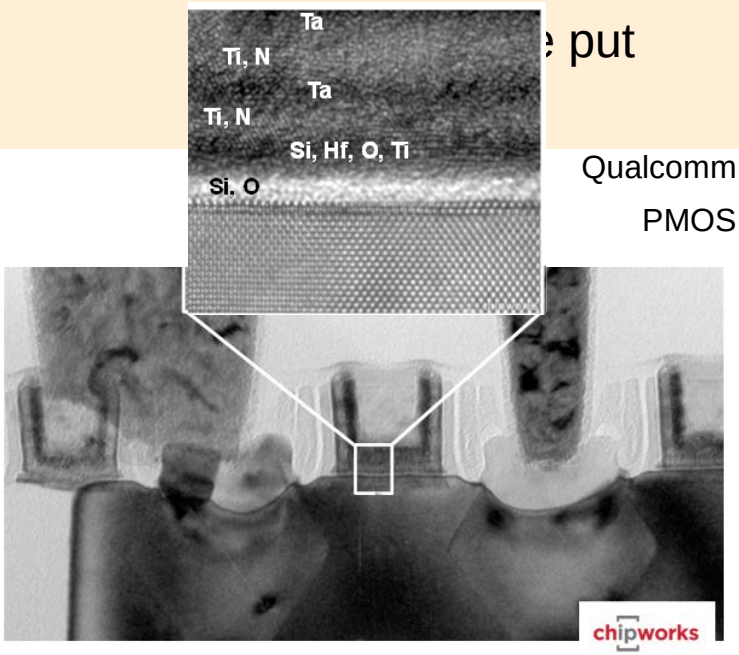


Figure 3 PMOS Transistor in Qualcomm Snapdragon 800

http://www.chipworks.com/en/technical-competitive-analysis/resources/blog/tsmc-20nm-arrives/

Resolving gate stack is possible but at which effort?

- **Atom Probe Tomography** is a promising method for investigating the gate stack on atomic scale.

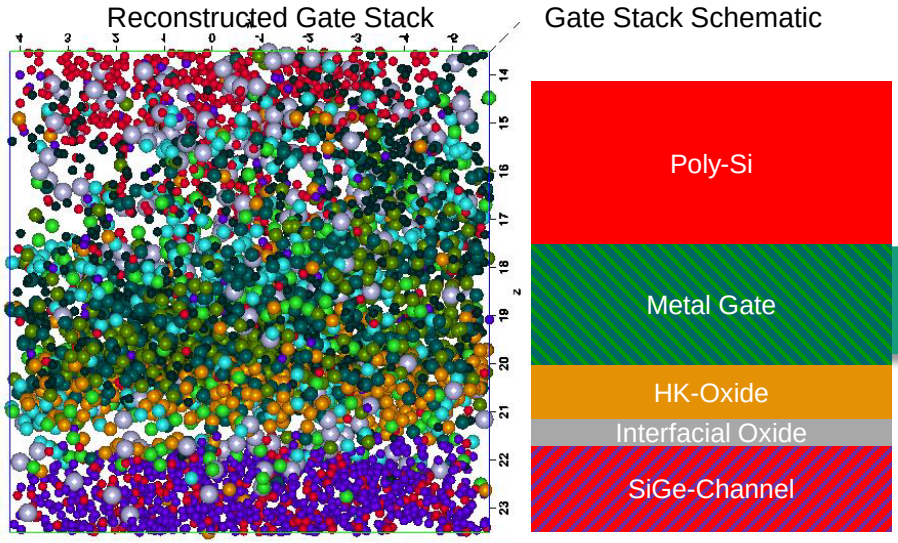
  → time and cost (!) consuming sample preparation, measurement and data analysis.

  → The different material properties cause great challenges.

Layer intermixing in the gate stack is observed by 3D APT

  → Real phenomenon or measurement artefact?

  → Meaning for process control?



Summary: Characterization challenges in future nodes

Industrial progress

Scientific explanation

…

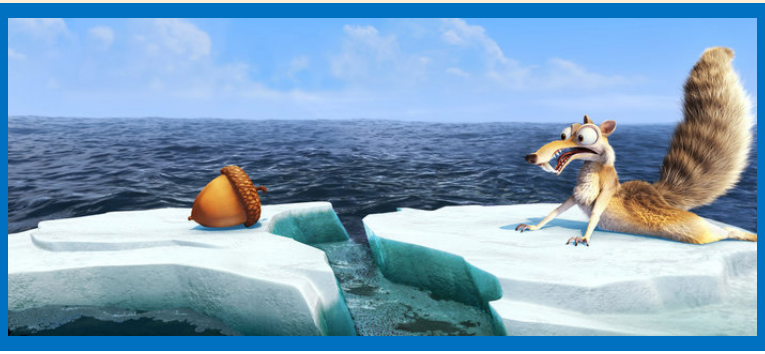
40nm

28nm

22nm

14nm

…



Summary: Characterization challenges in future nodes

- Variety of analytical challenges requires combinations of complementary analytical methods (imaging, physical, chemical and electrical analysis)
- Benefit-cost analysis is necessary for process control in a productive environment
- Understanding the 28nm technology in much more detail is important for the nanoelectronic industry to further optimize their products with respect to power, performance and energy efficiency.