Issues with Electrical Characterization of Graphene Field Effect Transistors

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Outline

• Motivation
• A Simple “Universal” Model for Transport in Single Layer Graphene
• Effect of Device Dimensions on Mobility
• Effect of Contacts
• CVD Graphene Vertical Tunnel Transistors
• Conclusions
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Motivation

Tunnel FETs or SymFET

- While the use of the FET test structure is common, there have been few investigations to systematically determine whether assumptions associated with characterizing the transport properties of graphene using this test structure are valid.

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Two Point Probe measurement setup. Contact Resistance extracted from the model.

Mobility extracted from $R$-$V_{bg}$ measurements using the model proposed Kim et al.

Also extracted is the intrinsic carrier concentration $n_0$.

The model assumes that the mobility is carrier concentration independent.

Question
Is this model for transport calculations and extraction consistent with other methods?
• Observed $\mu_H$ vs. $n$ trend agrees with reported trend for exfoliated graphene in literature

$$W. \ Zhu \ et \ al., \ Phys. \ Rev. \ B, \ 80, \ 235402 \ (2009)$$

• Mobility values from all models comparable at high bias.

• Difference in mobility at low bias attributed to the use of intrinsic carrier conc. $n_0$ in the constant mobility model.

• Extracted mobility is seen to have a significant dependence on the contact resistance

$\mu_{\text{const}}$ without $R_c$

$$\mu_{\text{const}}(296 \ K) \sim 2342 \ \text{cm}^2/\text{Vs}$$
$$\mu_{\text{const}}(77 \ K) \sim 2931 \ \text{cm}^2/\text{Vs}$$

A. Venugopalan et al., Journal of Appl. Phys. 109, 104511 (2011)
Comparison of Mobility Models

- Mobility reported in literature and mobility extracted using constant mobility model compared.

*Mobility reported in literature and mobility extracted using constant mobility model compared.*

<table>
<thead>
<tr>
<th>Sample</th>
<th>Description</th>
<th>Reported Mobility (cm²/Vs)</th>
<th>Extracted Mobility (cm²/Vs)</th>
</tr>
</thead>
<tbody>
<tr>
<td>UTD</td>
<td>Back-gate, measurement at ~300K</td>
<td>X</td>
<td>24381</td>
</tr>
<tr>
<td>Ref. 2</td>
<td>Top gate (Al₂O₃ dielectric), measurement at ~300 K</td>
<td>8600</td>
<td>8407</td>
</tr>
<tr>
<td>Ref. 1-1</td>
<td>Back-gate, measurement at ~5 K</td>
<td>30000</td>
<td>26134</td>
</tr>
<tr>
<td>Ref. 1-2</td>
<td>Back-gate, measurement at ~5 K</td>
<td>230000</td>
<td>201634</td>
</tr>
</tbody>
</table>

- Extracted and reported mobilities seen to be consistent
- Trends in sheet resistance at a given carrier concentration follow the trend in extracted mobilities as expected.


Mobility and Impurities

It is found that the product of mobility and impurity density is a constant for a wide variety of interfacial conditions, annealing conditions, top dielectrics and measurement temperatures.

\[ \mu \times n_0 \approx 1.15 \times 10^{15} \text{ /Vs} \]

A Simple “Universal” Model for SLG Transport

\[ R = R_c + R_{ch} \]
\[ R_{ch} = \frac{L/W}{n(V_{bg})q\mu} \]
\[ \rho_{sh} = \frac{R_{ch}}{L/W} \]
\[ n(V_{bg}^*) = \sqrt{n_{ind}(V_{bg}^*)^2 + n_0^2} \]
\[ n_{ind}(V_{bg}^*) = \frac{C_{ox}V_{bg}^*}{q} \]
\[ V_{bg}^* = V_{bg} - V_{Dirac} \]
\[ \mu \times n_0 \approx 1.15 \times 10^{15} /Vs \]

A. Venugopal et al., accepted Solid-State Communications (2012)
The maximum resistance of a single layer graphene device cannot be strongly changed.

The minimum resistance for high quality (low $n_0$) graphene is limited by $R_c$. As $n_0$ increases and $\mu$ decreases, the influence of $R_c$ on the minimum $R$ is less important.

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Dependence of $\mu_{\text{eff}}$ on $L_{\text{ch}}$

- Mobility determined to be dependent on channel length
- $L_{\text{ch}}$ dependence previously attributed to
  - device operating partially in the ballistic and diffusive regime
  - damage from e beam lithography

$R_{\text{ch}} = \frac{L/W}{n(V_{bg})q\mu}$

A. Venugopal et al., Journal of Appl. Phys. 109, 104511 (2011)

Z. Chen et al., IEDM (2008)

I. Meric et al., Nanoletters 11, 1093(2011)
**$\mu_{\text{eff}}(L_{\text{ch}}, W_{\text{ch}})$ – Dependence on $t_{\text{ox}}$**

- Extracted $\mu_{\text{eff}}$ plotted as a function of channel length ($L_{\text{ch}}$), width ($W_{\text{ch}}$) and underlying oxide thickness ($t_{\text{ox}}$).
- For comparable $L_{\text{ch}}$ and $W_{\text{ch}}$, mobility is seen to decrease with decreasing oxide thickness $t_{\text{ox}}$.

*A. Venugopal et al., Journal of Appl. Phys. 109, 104511 (2011)*
Graphene on 300 nm SiO₂ – Strip Capacitor


![Diagram of graphene strip]

- Uniformity of charge density distribution in the channel region depends on the aspect ratio, $W_{ch}/t_{ox}$ (ratio of the device width and the thickness of the dielectric).

- Comparable $W_{ch}$ and $t_{ox}$ results in enhanced charge density at the edges.

Nishiyama et al., IEEE Trans. on Components, Hybrids and Manufacturing Technology, 13, 417(1990)


Graphene on SiO$_2$ – Strip Capacitor

- Charge accumulation at the edges results in enhanced conductivity in the channel.

- Trend seen in conductivity vs. channel width manifests itself in the extracted mobility.


A. Venugopal et al., Journal of Appl. Phys. 109, 104511 (2011)
## Mobility Values

<table>
<thead>
<tr>
<th>Reference</th>
<th>Dielectric Type</th>
<th>tox (nm)</th>
<th>L (µm)</th>
<th>W (µm)</th>
<th>Temp. (K)</th>
<th>Mobility (cm²/Vs)</th>
</tr>
</thead>
<tbody>
<tr>
<td>[1]</td>
<td>SiO₂ (BG)</td>
<td>300</td>
<td>~5</td>
<td>~0.5</td>
<td>300-500</td>
<td>3000-10000</td>
</tr>
<tr>
<td>[25]</td>
<td>SiO₂ (BG)</td>
<td>300</td>
<td>2-4</td>
<td>0.5-4</td>
<td>350</td>
<td>2500</td>
</tr>
<tr>
<td>[25]</td>
<td>SiO₂ (BG)</td>
<td>300</td>
<td>2-4</td>
<td>0.5-4</td>
<td>350</td>
<td>2500</td>
</tr>
<tr>
<td>[26]</td>
<td>SiO₂ (BG)</td>
<td>300</td>
<td>5</td>
<td>5</td>
<td>1.7</td>
<td>10000</td>
</tr>
<tr>
<td>[27]</td>
<td>SiO₂ (BG)/HfO₂ (TG)</td>
<td>300</td>
<td>5</td>
<td>3</td>
<td>1.5</td>
<td>10000-17000</td>
</tr>
<tr>
<td>[21]</td>
<td>SiO₂ (BG)/NFC HfO₂ (TG)</td>
<td>300</td>
<td>17</td>
<td>1.5</td>
<td>300</td>
<td>8500</td>
</tr>
<tr>
<td>[18]</td>
<td>SiO₂ (BG)</td>
<td>300</td>
<td>10-15</td>
<td>5-10</td>
<td>300</td>
<td>25000</td>
</tr>
<tr>
<td>[4]</td>
<td>SiO₂ (BG)</td>
<td>300</td>
<td>3</td>
<td>1.5</td>
<td>5</td>
<td>25000</td>
</tr>
<tr>
<td>[4]</td>
<td>SiO₂ (BG)</td>
<td>300</td>
<td>3</td>
<td>1.5</td>
<td>5</td>
<td>200000</td>
</tr>
<tr>
<td>[13]</td>
<td>SiO₂ (BG)/Al₂O₃ (FG)</td>
<td>300</td>
<td>2.4</td>
<td>10</td>
<td>300</td>
<td>8500</td>
</tr>
<tr>
<td>[28]</td>
<td>SiO₂ (BG)</td>
<td>300</td>
<td>7.3</td>
<td>0.4</td>
<td>300</td>
<td>4780</td>
</tr>
<tr>
<td>[29]</td>
<td>h-BN (BG)</td>
<td>14</td>
<td>~3.5</td>
<td>~1.5</td>
<td>4</td>
<td>60000</td>
</tr>
<tr>
<td>[30]</td>
<td>SiO₂ (BG)</td>
<td>300</td>
<td>4</td>
<td>7</td>
<td>300</td>
<td>4500</td>
</tr>
<tr>
<td>[31]</td>
<td>SiO₂ (BG)</td>
<td>300</td>
<td>3-20</td>
<td>3-20</td>
<td>1.6</td>
<td>2000-20000</td>
</tr>
<tr>
<td>[32]</td>
<td>SiO₂ (BG)</td>
<td>300</td>
<td>3-5</td>
<td>1-3</td>
<td>300</td>
<td>8200</td>
</tr>
<tr>
<td>[32]</td>
<td>Al₂O₃ (BG)</td>
<td>72</td>
<td>3-5</td>
<td>1-3</td>
<td>300</td>
<td>7400</td>
</tr>
</tbody>
</table>


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\[ R_{tot} = 2R_{con} + R_{ch} \]

- Scatter in data reduces with increasing carrier concentration
- The contact resistance obtained using TLM is equivalent to the total resistance at high \( V_{bg} \).

Contact Resistance as a Function of Metal Type

- No appreciable difference between $R_c$ measured in air vs. $R_c$ measured in vacuum
- No dependence on metal work function
- Possible reasons:
  - residue at the interface dominates any difference that metal type might have
  - charge transfer does not contribute appreciably to the contact resistance ($R_c$)
Dependence of $R_c$ on $W_c$

Typical current flow paths

Current flow path in a graphene device (assumption)

![Graphene sheet](image)
## Contact Resistance Values

<table>
<thead>
<tr>
<th>Reference</th>
<th>Metal</th>
<th>Pre-/Post Process Conditions</th>
<th>Measurement Conditions</th>
<th>Contact Resistance</th>
</tr>
</thead>
<tbody>
<tr>
<td>[44]</td>
<td>Ti/Au</td>
<td>N/A</td>
<td>TLM at 0.25-4.2 K</td>
<td>800 Ω-µm</td>
</tr>
<tr>
<td>[15]</td>
<td>Ni</td>
<td>N/A</td>
<td>TLM at room temp</td>
<td>800-2000 Ω-µm²</td>
</tr>
<tr>
<td>[41]</td>
<td>Cr/Au</td>
<td>PMA (H₂/Ar, 300 °C, 1 hr)</td>
<td>CBKR at room temp</td>
<td>10⁻³-10⁶ Ω-µm</td>
</tr>
<tr>
<td>[41]</td>
<td>Ti/Au</td>
<td>PMA (H₂/Ar, 300 °C, 1 hr)</td>
<td>CBKR at room temp</td>
<td>10⁻³-10⁶ Ω-µm</td>
</tr>
<tr>
<td>[41]</td>
<td>Ni</td>
<td>PMA (H₂/Ar, 300 °C, 1 hr)</td>
<td>CBKR at room temp</td>
<td>500 Ω-µm</td>
</tr>
<tr>
<td>[45]</td>
<td>Pd/Au</td>
<td>N/A</td>
<td>TLM at room temp</td>
<td>230 Ω-µm</td>
</tr>
<tr>
<td>[45]</td>
<td>Pd/Au</td>
<td>N/A</td>
<td>TLM at 6 K</td>
<td>90-130 Ω-µm</td>
</tr>
<tr>
<td>[46] (CVD)</td>
<td>Ti/Pd/Au</td>
<td>5 nm Al followed by etch</td>
<td>I-V at room temp</td>
<td>2000-2500 Ω-µm</td>
</tr>
<tr>
<td>[47] (Epi)</td>
<td>Ti/Au, Ni/Au, Pt/Au, Cu/Au, Pd/Au</td>
<td>PMA (Forming Gas, 450 °C, 15 min)</td>
<td>TLM at room temp</td>
<td>&gt;1000 Ω-µm²</td>
</tr>
<tr>
<td>[42] (Epi)</td>
<td>Ti/Au, Ni/Au, Pt/Au, Cu/Au, Pd/Au</td>
<td>O2 Plasma Clean and PMA (Forming Gas, 450 °C, 15 min)</td>
<td>TLM at room temp</td>
<td>~7.5 Ω-µm²</td>
</tr>
<tr>
<td>[47] (Epi)</td>
<td>Cr/Au</td>
<td>N/A</td>
<td>TLM at room temp</td>
<td>0.005 Ω-µm²</td>
</tr>
<tr>
<td>[47] (Epi)</td>
<td>Cr/Au</td>
<td>N/A</td>
<td>TLM at 673 K</td>
<td>0.003 Ω-µm²</td>
</tr>
<tr>
<td>[47] (Epi)</td>
<td>Ti/Au</td>
<td>N/A</td>
<td>TLM at room temp</td>
<td>0.06 Ω-µm²</td>
</tr>
<tr>
<td>[47] (Epi)</td>
<td>Ti/Au</td>
<td>N/A</td>
<td>TLM at 673 K</td>
<td>0.05 Ω-µm²</td>
</tr>
</tbody>
</table>

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Improved performance by 80 °C in-situ anneal

- Mobility as high as 7200 cm²/Vs at room temperature (65 x 15 μm²)
- Mobility as high as 12700 cm²/Vs at 77K, highest reported CVD graphene with FET structure

Approaching Exfoliated Graphene

- Electrical behavior of CVD graphene is similar to that of exfoliated graphene on SiO$_2$ substrate
- Mobility approaches the limit (~10,000 cm$^2$/Vs) of graphene reported on SiO$_2$* 
- The mobility is by impurity scattering at low temperature and both phonons and impurities at room temperature.


Vertical Graphene Tunnel FET Literature

- Tunneling for a graphene-hBN device with 6 ± 1 layers of hBN as the tunnel barrier.
- Room temperature switching ratio:
  - ≈ 50 with h-BN
  - ≈ 10000 with MoS$_2$[1]

Vertical Graphene Tunnel FET Literature

- Negative differential resistance can be observed when Dirac points of two graphene layers line up\textsuperscript{[2-3]}

\[2\] Feenstra et al., *J. Appl. Phys.*, 111 (2012)
Fabrication process and sample preparation:

- Thermal growth of SiO$_2$ on p-doped Si
- Wet transfer of CVD graphene
- CVD graphene anneal in 2% forming gas
- Graphene etch in oxygen plasma
- Lift-off of Ni/Au drain metal contacts
- E-beam evaporation of Ti seeding layer on graphene
- Atomic layer deposition of dielectric
- Wet transfer of top graphene layer
- Graphene etch in oxygen plasma
- Lift-off of Ni/Au source metal contacts
- Anneal of top graphene layer in 2% forming gas
- 80 °C anneal of devices in vacuum prior to measurement
Gate Voltage Dependence of Current

\[ S = \frac{dI_D}{dV_G} = \frac{\partial I_D}{\partial V_D} \frac{\partial V_D}{\partial V_G} \]

- Subthreshold swing for TiO_x/Al_2O_3 – 120 mV/dec
- Subthreshold swing for TiO_x/TiO_2 – 70 mV/dec
- \( I_{ON}/I_{OFF} \approx 10^6 \)
Drain Voltage Dependence of Current

\[ S = \frac{dI_D}{dV_G} = \frac{\partial I_D}{\partial V_D} \frac{\partial V_D}{\partial V_G} \]

- Upon decoupling gate oxide capacitance
  - “subthreshold swing” \((\partial I_D/\partial V_D)^{-1} \approx 27 \text{ mV/dec for TiO}_x (2 \text{ nm})/\text{TiO}_2 (5 \text{ nm})\)
  - 10 mV/dec for TiO\(_x\) (1 nm)/Al\(_2\)O\(_3\) (1 nm)/TiO\(_2\) (1 nm)

- Symmetric current for symmetric barrier
- Drive current extremely low
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• A simple model for the total device resistance indicates that the maximum graphene resistance is approximately independent of mobility and that the minimum resistance is limited by the contact resistance.
• Mobility depends on both the device length and width. Large device dimensions should be used when extracting mobility.
• Current saturation at large fields is due to the contact resistance.
• The width dependence of contact resistance suggests preferential injection at the edges of graphene.
• A transfer process for CVD graphene has been developed which achieves mobility consistent with exfoliated graphene.
• Vertical tunnel FETs have been fabricated using bilayers of CVD graphene.