Economies of CMOS Scaling

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Revenue and R&D Forecasting

- 1970-1995 Revenue Trend: 16% cagr
- 1995-2004 Revenue Trend: ~5-10% cagr

R&D outgrowing revenue...
Increasing Investment in R&D

- New process development > $300M
  - Time to revenue > 4 years
- New wafer fab > $2B
  - Time to revenue > 2-3 years
- New product development > $10M × 100
  - Time to revenue > 1.5 years

- High risks with long cash flow
  - Volatile market
  - Difficult execution
  - Rapid innovation cycles
**Pricetrend Baseline CMOS**

**Foundry Data**

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**Average Si wafer Price ($/cm^2)**

- **Node (um)**: LTPS : 1-1.5 $/cm^2
- **Price Trend (time) at fixed Node**
- **2ML, 13 masks**
- **7LM, 36 masks**

**Cost per die for same function**

**Source:** [2004] Carel van der Poel, Philips Research

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**Min = 2/3 * Average**

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**Technology for Innovators**

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**Source:** [2004] Carel van der Poel, Philips Research
Next Generation CMOS Challenges

- Immersion 193 lithography with extensive RET
- Low leakage and high performance sub 40nm CMOS transistors
  - Strain engineering
  - High-k gate dielectric and metal gate
- Cu interconnect with ultra low-k dielectrics

- Power Management
- Analog and RF integration on the driver product
- Process development on 300mm
Limited market opportunity for consumables

Sources: IBM, SEMI and WaferNews
Increasingly complex
Increasingly expensive

**0.25um**
- size adjusts
- iso/dense selective size adjusts for poly
- line end extension

**0.18um**
- size adjusts
- iso/dense selective size adjusts (SSA)
- hammerheads and serifs
- model based OPC for active and poly
- attenuated PS for holes and poly
- vector e-beam reticle write for active and poly

**130 nm**
- size adjusts
- iso/dense selective size adjusts (SSA)
- hammerheads and serifs
- model based OPC for active and poly
- attenuated PS for holes
- alternating PS for poly
- advanced OPC strategies
- vector e-beam reticle write for all critical levels

**65 nm**
- size adjusts
- model-based iso/dense SSA
- hammerheads and serifs
- model based OPC for active, poly, contacts and metal
- attenuated PS for holes
- alternating PS for poly
- vector e-beam reticle write for all critical levels
- Scattering bars for multiple levels

**90 nm**
- size adjusts
- model-based iso/dense SSA
- hammerheads and serifs
- model based OPC for active, poly and metal
- attenuated PS for holes
- alternating PS for poly
- advanced OPC strategies
- vector e-beam reticle write for all critical levels

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Complexity of Contact SRAFs

Single Isolated Contact:
Requires sub-resolution assist features to print

Nearby Contact:
Requires sharing of sub-resolution assist features

Multiple Contacts
Conflicts require complicated conflict resolution code

Production Layouts
Millions of SRAF compromises followed by model based sizing of every contact
Tight Design Rules

- Contact patterning is no. 1 lithography challenge for 65nm
- Tight gate-to-contact spacing results in little margin for contact edge roughness or deformation, or for alignment
- Significant work needed for OPC, to optimize photo and etch processes
Strained Silicon

- PMD liner
- Capped poly
- Raised S/D
- Implant S/D strain
- Substrate orientation
- Recess S/D epi (SiGe)
- STI liner
- Active area epi

Normal Si lattice

Strained Si lattice

Improved mobility

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Holes in [110] Uniaxially Compressed Si

Unstrained Heavy Hole (HH)

Strained Heavy Hole (HHS)

Mobility Improves

Mobility Degrades
Gate Insulator

**Good News**

- **Gate Leakage** vs. **EOT (nm)**
- **Dielectric Constant** vs. **Breakdown Strength (MV/cm)**

**Bad News**

- **SiO₂ (k=3.9)**
- **HfO₂ (k=21), ZrO₂ (k=29)**
- **TiO₂ (k=60-95)**
- **Si₃N₄ (k=7.5), Al₂O₃ (k=9)**
- **Ta₂O₅ (k=19-26), La₂O₃ (k=27), Pr₂O₃ (k=31)**
- **SrTiO₃ (k=50-200)**

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Metal Gate

Valence Band
Optimum for PMOS
Mid-Gap
Optimum for NMOS
Conduction Band

Work Function (eV)

La
Ta
Zr
In
Cd
Ag
Al
Nb
V
Zn
Sn
Cr
W
Mo
Ru
Ti
Os
Re
Rh
Ir
Pt

5.20
4.63
4.05

3.0
3.5
4.0
4.5
5.0
5.5
6.0
New Silicide: NiSi

Ni moves into the silicon; affected by strain
New Materials and Markets

Limited market opportunity for consumables

Sources: SEMI and WaferNews
Interconnect Integration

- Bond pad
- TaN & Aluminum Dep
- OxyNitride Dep
- HDP FSG Dep
- LD/IMD Etch
- SiN E-Stop Dep
- Cu Seed Dep
- TaN liner
- OSG IMD Dep
- OSG IMD-3
- OSG IMD-2
- OSG ILD-3
- OSG IMD-4
- FSG dual damascene V4-M5
- HDP PSG Dep
- ARC DEP (SRN)
- CuNitrile ES
- PETOS Cap SiO2
- He Pretreat
- W CVD Dep
- SiN E-Stop Dep
- W SiC E-Stop Dep
- OSG IMD-1
- OSG IMD-2
- OSG IMD-3
- OSG IMD-4
- OSG IMD Dep
- SiC E-Stop Dep
- OSG IMD Dep
- TaN liner
- STI Dep
- He Pretreat
- W CVD Dep
- Contact Liner
- HDP PSG Dep
- PMD Liner
- Salicide Dep PVD Co
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Low k Dielectric Cracking

- Crack propagation from die saw edge into the die
- Interface engineering
- Optimization of dummy fill structures

Delamination crack broke through old scribe seal
Interconnect RC trends

- Capacitance continues to decrease linearly.
- Resistance is increasing on a steep exponential for minimum pitch lines due to boundary scattering.
- For fixed pitch line lengths (1000x) R increase swamps C decrease node-to-node.
1) **Subthreshold Leakage** – traditional component
   - Shorter channel lengths
   - Higher channel doping
   - Threshold Voltage not scaling as fast as Vdd
2) **Gate Oxide Leakage or Tunneling Current**
   - As oxide thins, leakage increases exponentially
3) **Gate Induced Diode Leakage (GIDL)**
   - Band to band tunneling
   - Shallow junctions
   - Higher doping of Source & Drain
Off-Current vs Node

Reported $I_{\text{off}}$ (nA/µm) vs Node

- Competition
- TI nodes
- 45nm projection
- 45nm design

Node:
- 350nm
- 250nm
- 180nm
- 130nm
- 90nm
- 65nm
- 45nm

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Product Power Management

Power Management Strategies:

- *Dynamic Voltage & Frequency Scaling*
- *Multiple Voltage Domains*
- *Multiple Vt Libraries*
- *Sleep modes*
- *Drowsy modes*
- *Substrate biasing*
- *Tapered metal routers*
- *Non-orthogonal Place & Route*

![Diagram](image)
Manufacturing

• The science of manufacturing is finding all the relevant (systematic and random) defects and eliminate them, in parallel
  – Yield is no longer limited by manufacturing: design greatly affects yield -> DFM

• The business of manufacturing is to maximize the scalability of capacity, taking advantage of the upturns and reducing the impact of the downturns
  – Processes and designs have to be portable between fabs
Signal to Noise in Defect Metrology

Today’s highly sensitive defect metrology finds “everything”

Challenge:

➢ How do we know which of these defects are Yield killers?

Even Bigger Challenge:

➢ How do we know which of these defects are reliability issues?

Dominated by very small defects (noise or signal?!)?
Improving ROIC

Advanced Logic

Mixed-Signal Analog

High-Performance Analog

2 Years Peak To Peak

3 Years Peak To Peak

5 Years or More Peak To Peak

Foundries

Migrate Factories

Migrate Equipment

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Sub 100nm CMOS is Different

- Many new materials and processes to keep the physics going
  - Cu, Low-k, NiSi, SiGe, HfSiON, FUSI, etc
  - Immersion litho, millisecond annealing, constant angle implant, strain engineering, etc.
- Leakage has reached the ceiling
  - Easiest way to increase current drive
  - Several new components: gate dielectric & junction tunneling
- Interconnect not scaling
  - Makes up half the delay in a critical path
  - Capacitance is materials and integration limited
  - Resistivity increasing for narrow lines
- Increased variances; design for manufacturing
  - Doping fluctuations, supply-threshold voltage reduction, interconnect R&C
  - Physical design affects process yield
- Product requirements go beyond digital
  - High voltage I/O, mixed signal, analog, RF integration, non-volatile memory
Summary

• The major challenges to sustain CMOS scaling are
  – Economics/Complexity of new materials and processes
  – Cost/Complexity of physical design
• Product Innovation will be enhanced by
  – Analog, RF, High Voltage integration
  – Package contributions
  – Architecture differentiation
Technolog Scaling

180nm (C05)
- Die Size: 78mm²
- DSP Core: 360 MHz
- 200mm (8") wafer
- Die Count: 396

130nm (C09)
- Die Size: 51mm²
- DSP Core: 720 MHz
- 200mm (8") wafer
- Die Count: 518

90nm (C027)
- Die Size: 32mm²
- DSP Core: 1 GHz
- 200mm (8") wafer
- Die Count: 828

90nm (C037)
- Die Size: 32mm²
- DSP Core: 1 GHz
- 300mm (12") wafer
- Die Count: 1182

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TExAS INSTRUMENTS
Advanced 200mm Analog

HPA07 High Performance OP AMP
.25 Pitch
29000 Chips/Wafer

99% Yield