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PIONEERS IN COLLABORATIVE RESEARCH®

2003 International Conference
Characterization & Metrology for ULSI Technology

CMOS Devices and Beyond
A Process Integration Perspective

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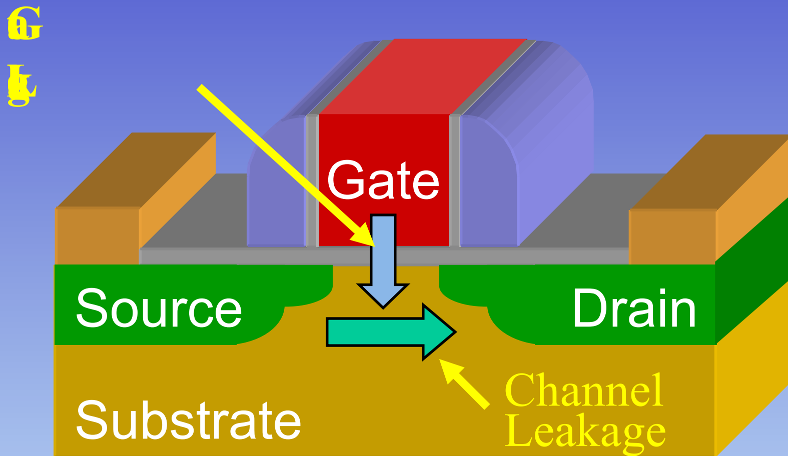
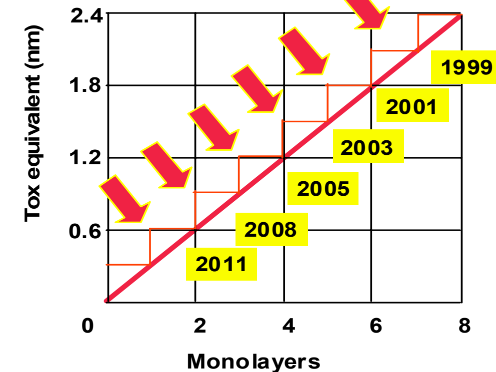
March 25, 2003

Conventional Bulk-Si MOSFET Scaling Issues





Primary barriers to MOSFET scaling are:

- High I_{on}/I_{off} ratio (I_{off} = Channel leakage current)
- Low Standby leakage current (Gate + Channel leakage)
  - Low channel leakage current (Electrostatic scaling)
  - Low gate leakage current

2001 ITRS Projections Vs. Simulations of Direct Tunneling Gate Leakage Current Density for *Low Power Logic*

J_{gate} (A/cm^2)

1.E+02
1.E+01
1.E+00
1.E-01
1.E-02
1.E-03
1.E-04
1.E-05
1.E-06
1.E-07

T_{ox} (nm)

3
2.5
2
1.5
1
0.5
0

2001 2003 2005 2007 2009 2011 2013 2015

Year

Simulated J_{gate}, oxynitride

Specified J_{gate}, ITRS

Tox

Beyond this point, oxynitride too leaky; high K needed

(Simulations courtesy of C. Osburn, NCSU and ITRS and ISMT P. Zeitzoff)

Implementation of high-k will be driven by Low Power Logic in 2005

2001 ITRS Projections Versus Simulations of Gate Leakage Current Density for *High-Performance Logic*

1.E+06
1.E+05
1.E+04
1.E+03
1.E+02
1.E+01
1.E+00
1.E-01

J_g (A/Cm^2)

2
1.5
1
0.5
0

EOT (nm)

Maximum J_g (<$I_{sd,leak}$ per 2001 ITRS)

Simulated J_g, oxynitride

EOT

2001 2003 2005 2007 2009 2011 2013 2015

Year

CMOS Devices and Beyond

Outline

- **CMOS Devices ...**
  - MOSFET Scaling Issues
  - Non-Classical CMOS Structures
    - Ultra-Thin Body MOSFETs
    - Channel Engineered Structures
    - FinFETs
    - Double Gate Structures
- **… And Beyond - Novel FET Structures and/or New Information Processing Architectures**
  - Potential of Molecular, Nanowire and Nanotube Electronics
    - MOSFET-like switches?
    - New Information Processing Technology?
  - Limits on Integration Density - Device Size or Power?
- **Conclusions**

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CMOS Devices ….

A Process Integration Perspective

Bulk-Si Performance Trends

Maintaining historical CMOS performance trend requires new semiconductor materials and structures by 2008-2010... Earlier if current bulk-Si data do not improve significantly.

Normalized Device Performance

10.00
1.00
0.10

1985 1990 1995 2000 2005 2010 2015 2020

Year

IEDM Benchmark Technologies
ITRS Projections
Experimental (bulk-Si) Data
: Projected forward
Bulk-Si Transport Properties "Best Case"
Historical Trend (17% per year)

New Materials & Non-Classical Structures for CMOS

Relative Device Performance

100

10

1

— Conventional Bulk CMOS
— SOI (silicon-on-insulator) ≤ 1.2 x bulk
— Strained Si/SiGe ≤ 1.6 x bulk
— Double-Gate ≤ 1.8 x bulk

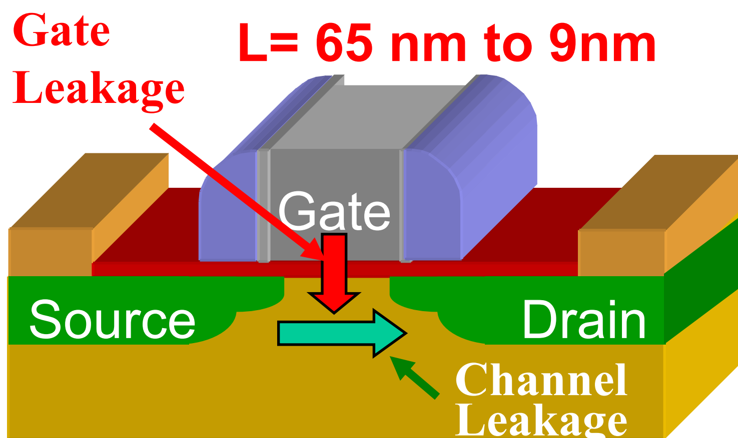
17%/Year

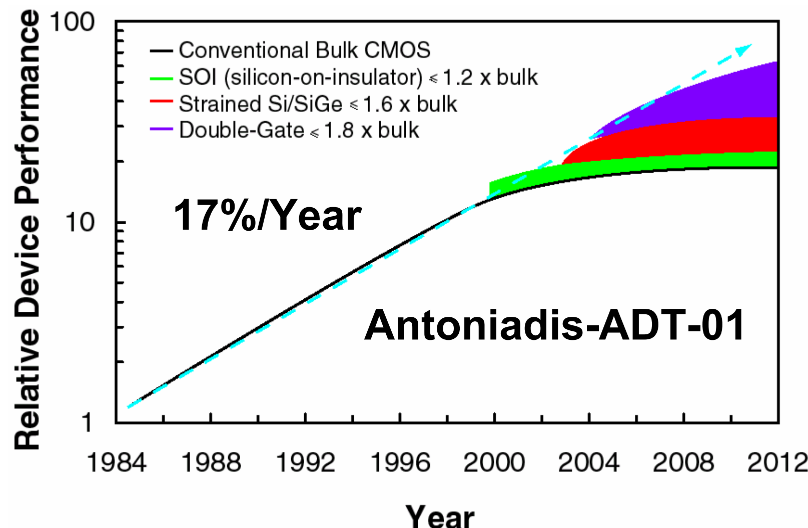
Antoniadis-ADT-01

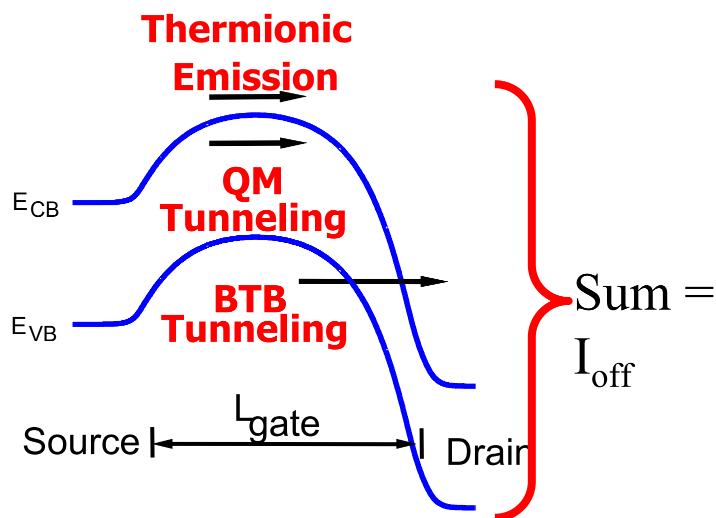
1984 1988 1992 1996 2000 2004 2008 2012

Year

Nano-FET Scaling Fundamental Issues





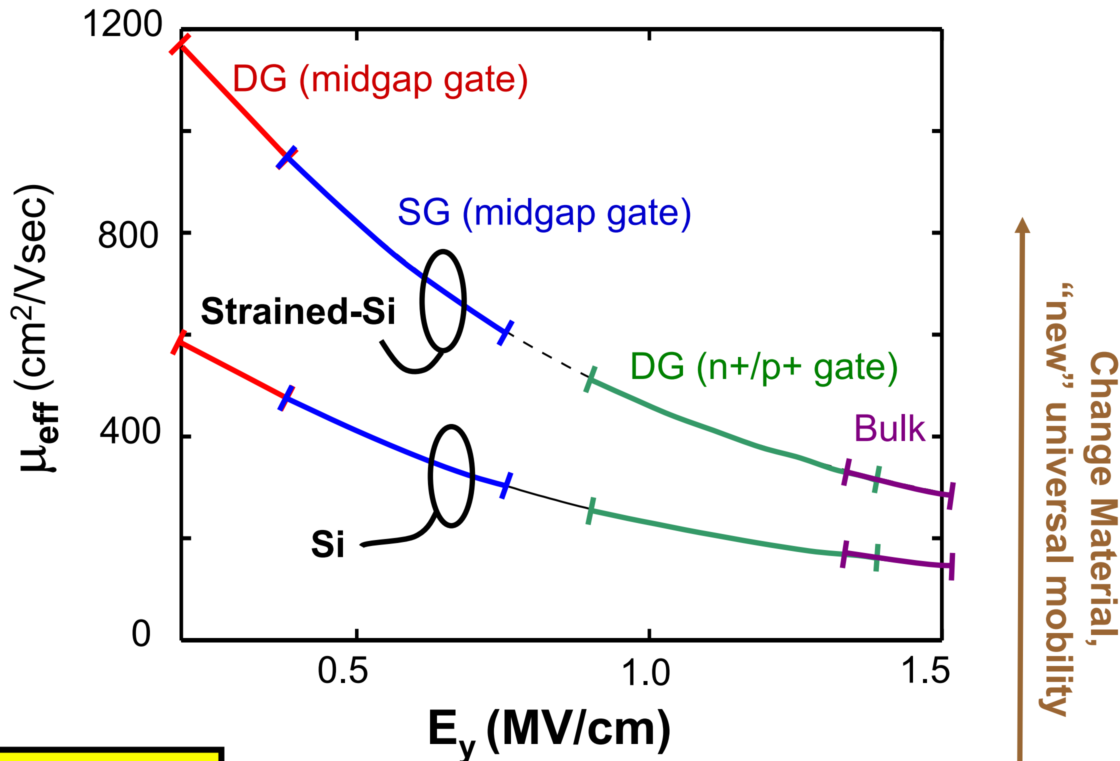


Electrostatic and quantum scaling (I_{on}/I_{off})

- Increase carrier transport and ballistic efficiency.
- Reduce quantum tunneling of electrons and holes.
- Break the tyranny of the universal mobility curve.
  - Bandgap engineered FET
  - New device architecture

Breaking the tyranny of the universal mobility: Alternative device structures & new Si-based materials

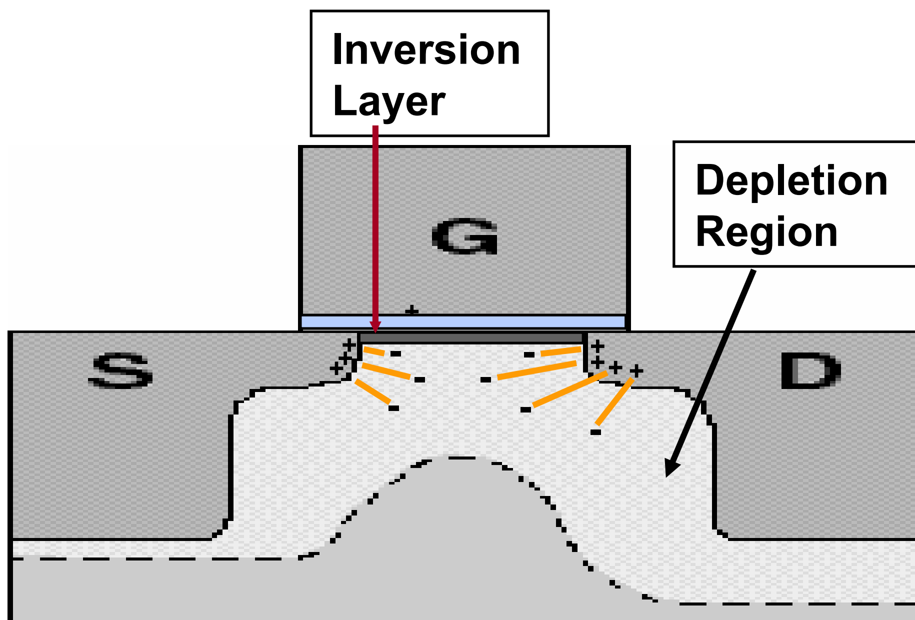
E_y for *constant inversion charge* range for four device architectures



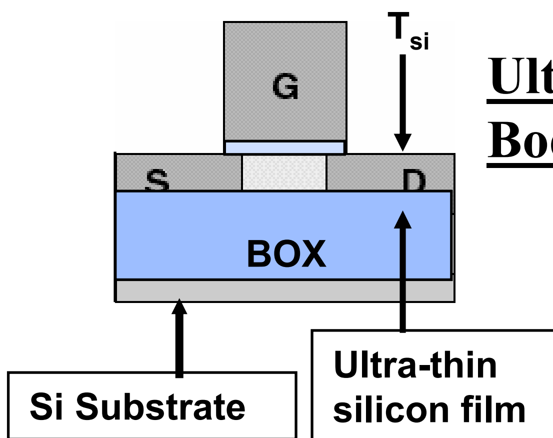
MIT - D. Antoniadis

Change Architecture,
“bulk-Si” universal mobility but reduced doping

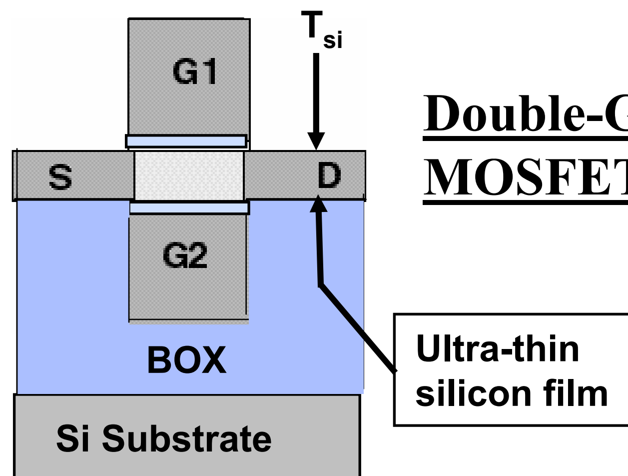
Schematic cross section of planar bulk, UTB SOI, and DG SOI MOSFET



Bulk MOSFET

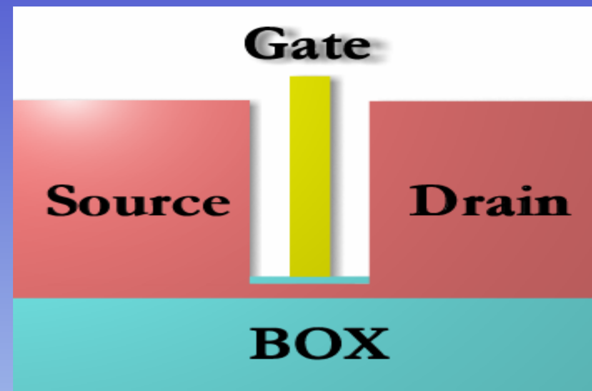


Ultra-Thin Body SOI



Double-Gate SOI MOSFET

Ultra-Thin-Body MOSFET



Advantages

- Suppresses channel leakage
- Improves V_t controllability
- Raised Si/Ge source/drain improves I_{on}

Challenges

- Requires ultra thin silicon channel
- Gate Stack
- Device characterization
- Compact model - parameter extraction

UTB SOI MOSFET Scaling

- **Issues for bulk-Si MOSFET scaling obviated**
  - Body does not need to be heavily doped
  - T_{ox} does not need to be scaled as aggressively
    - EOT can be 5% lower for same I_{gate} however (L. Chang *et al.*, *IEDM 2001*)
  - Ultra-shallow S/D junction formation is not an issue
- **Body thickness must be less than ~1/3 x L_{gate}**

Scale length $l = \sqrt{T_{ox} d\, \varepsilon_{si} / \varepsilon_{ox} + d^2/2}$ **where $d = T_{Si}$**

Formation of uniformly thin body is primary challenge

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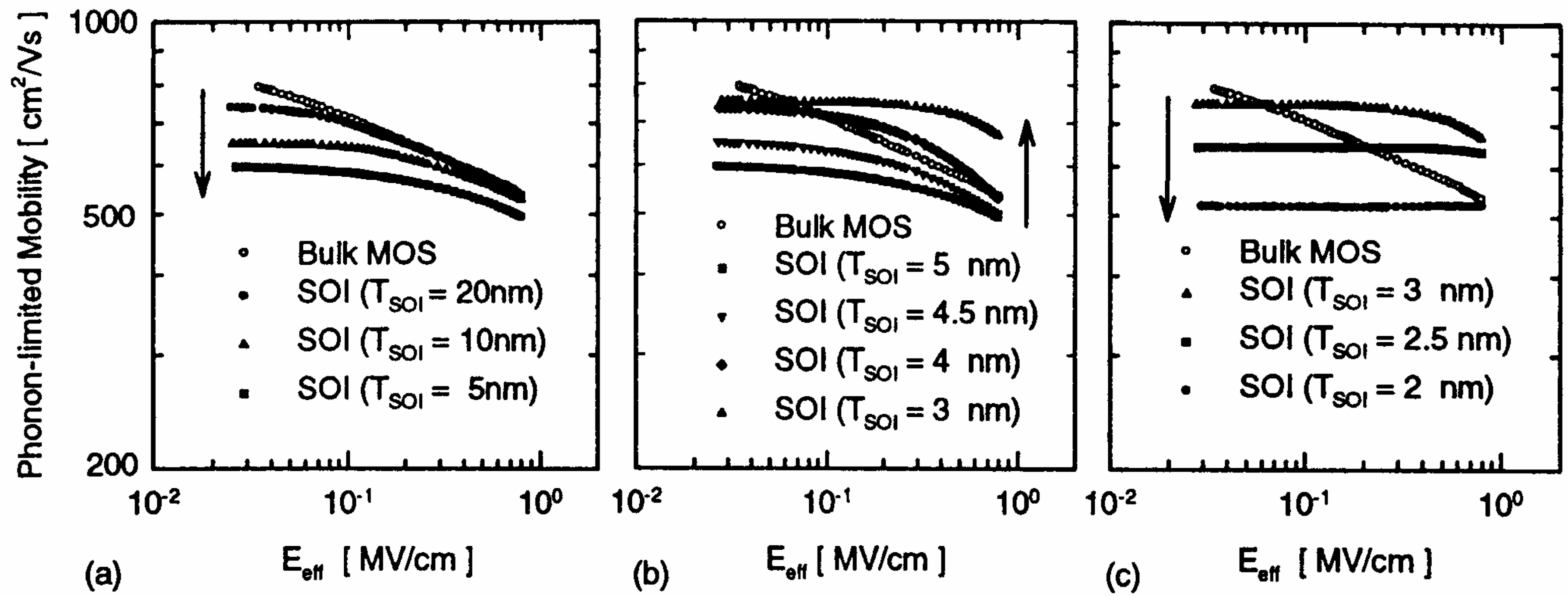
Theoretical mobility as function of silicon film. At Tsoi = 3 - 5 nm, mobility becomes higher than that in bulk Si MOSFET.



(S.Takagi et al.; SSDM ’97, p.154)

Advanced Gate Stack Materials for Thin-Body SOI MOSFETs

- **High-κ gate dielectrics**

  Desirable for reducing $T_{ox,eq}$ to
  - improve I_{dsat}
  - reduce short-channel effects

- **Metal gate materials**

  Desirable to
  - eliminate gate depletion effect
  - reduce gate-line resistance

  Necessary to achieve proper V_t in UTB MOSFETs
  (due to low body doping N_{body})

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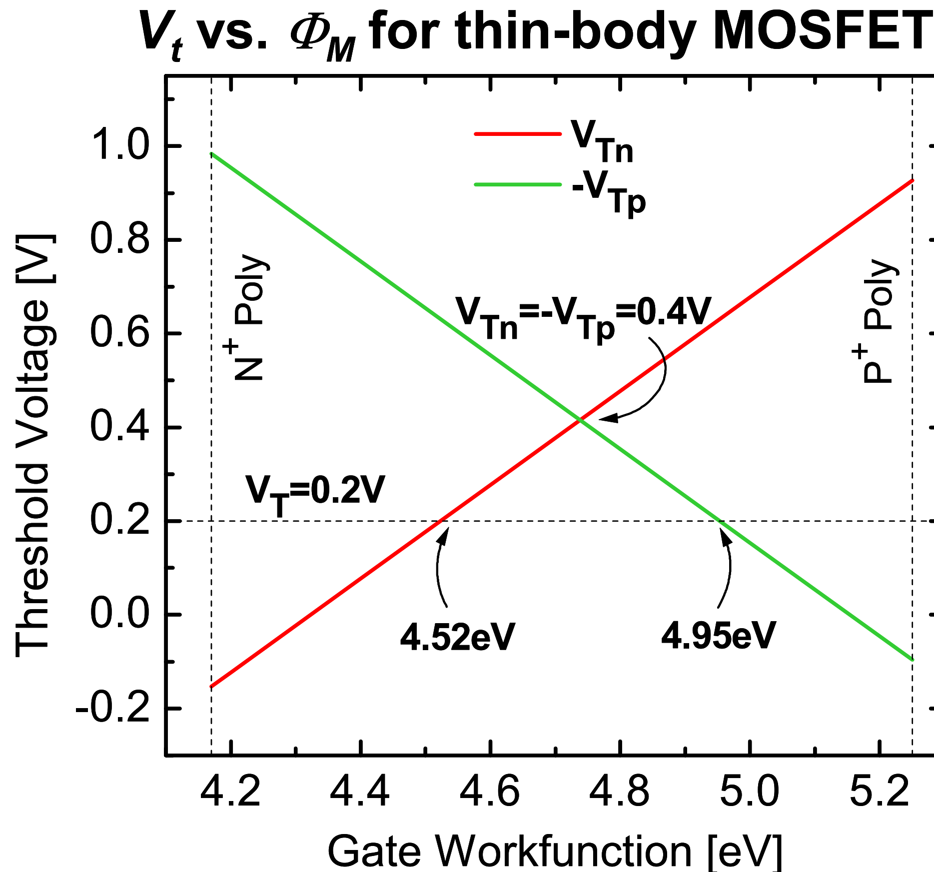
Thin-Body MOSFET V_t Control

Gate Work-Function Engineering



L. Chang *et al.*, *IEDM Technical Digest*, pp. 719-722, 2000

- **Low and symmetrical V_t's are desirable**
  - **dual N^+/P^+ poly-Si**
    - ⇒ $V_{tn} = -V_{tp} = -0.1V$ ← ***too low***
  - **mid-gap gate material**
    - ⇒ $V_{tn} = -V_{tp} = 0.4V$ ← ***too high***

⇒ **Need dual-work-function metal gates w/ tunable Φ_M**

~4.5V for NMOS; ~4.9V for PMOS

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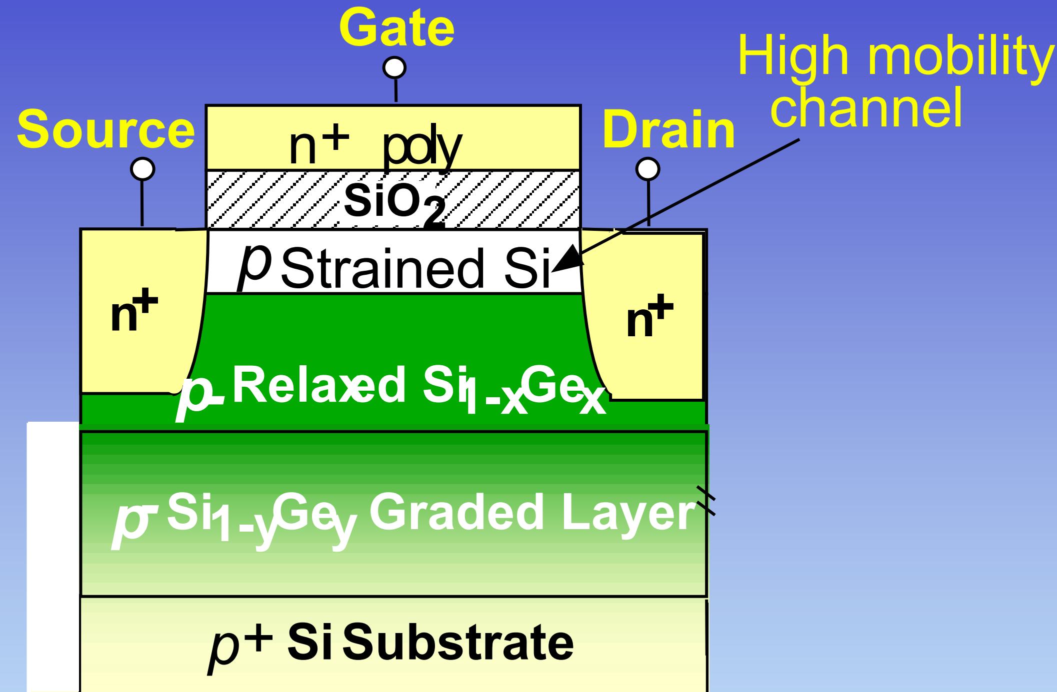
Band Engineered Transistor
(Strained Si/SiGe Mobility Enhanced Channel)



Advantages

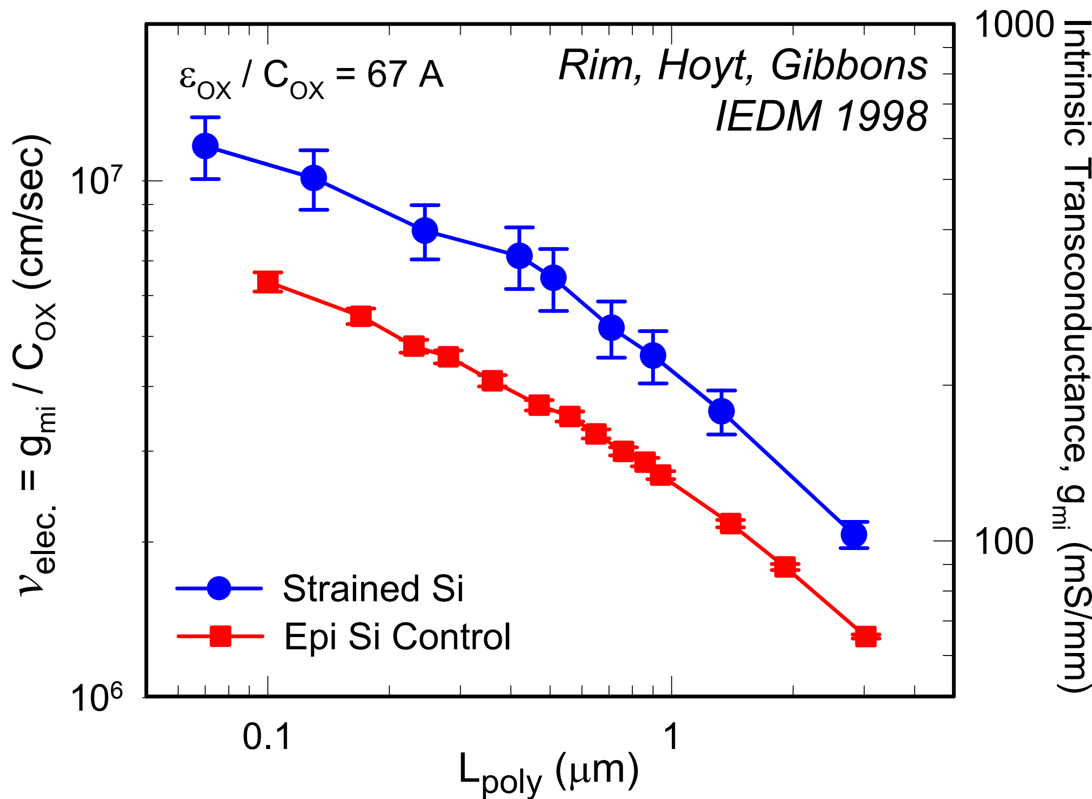
- Higher drive current (I_{on})
- Compatible with bulk and SOI CMOS

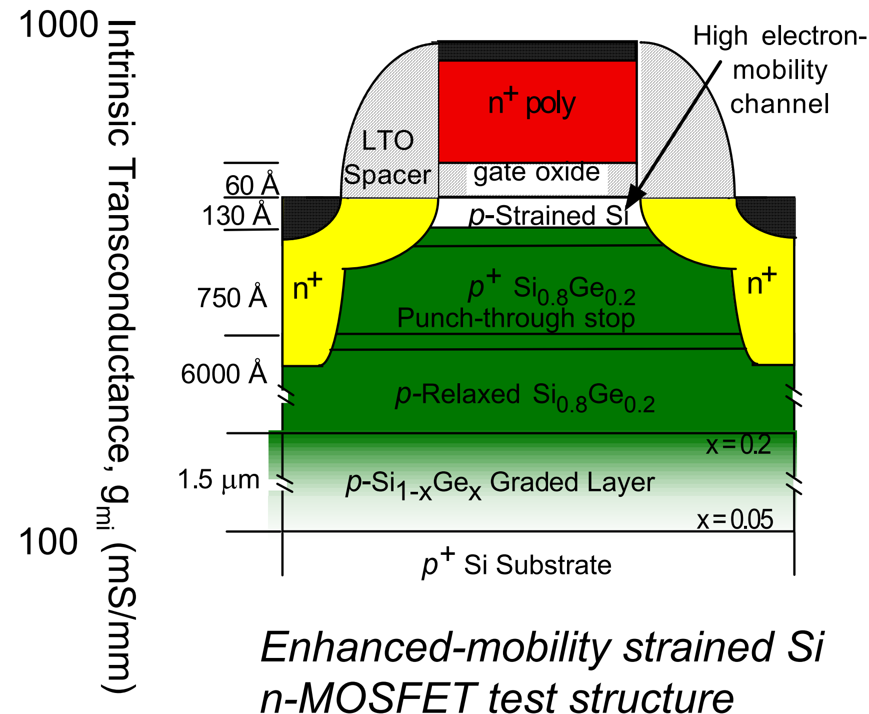
MIT - J. Hoyt

Challenges

- High mobility channel film thickness for SOI
- Gate stack
- Integration process
- Device characterization

Mobility Enhancement in Strained-Si-Channel n-MOSFETs

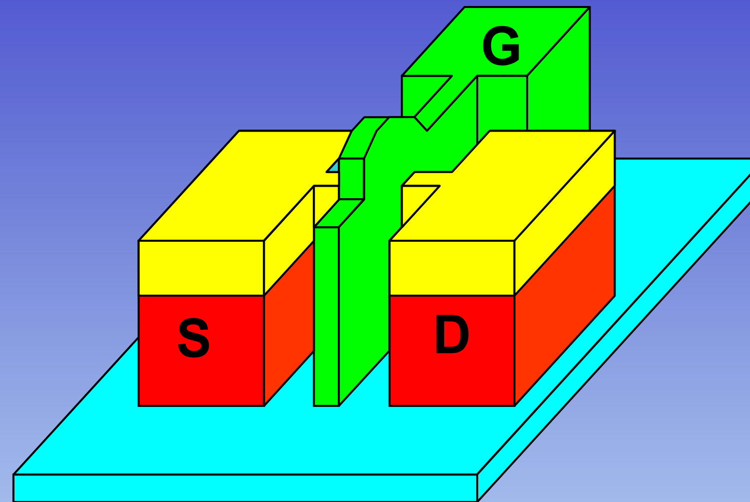




Enhanced-mobility strained Si n-MOSFET test structure

MIT - J. Hoyt

FinFET Structure



Advantages

- Higher drive current (I_{on})
- Improved subthreshold V_t slope
- Improved short channel effect (electrostatics)
- Stacked NAND gate

Challenges

- Silicon film thickness
- Gate stack
- Process complexity
- Gate width available in integral steps
- Accurate TCAD

FinFET Scaling

- **Compared with UTB-MOSFET:**
  - Reduced short-channel effects => more scalable
  - Higher current drive due to
    - steeper subthreshold swing (60 mV/dec)
    - lower channel electric field => higher carrier mobilities
- **Fin width must be less than 2/3 x L_{gate}**

  Scale length $l = \sqrt{T_{ox} d\, \varepsilon_{si} / \varepsilon_{ox} + d^2/2}$ **where d = 0.5xT_{Si}**

  Formation of narrow fin is primary challenge

  - sub-lithographic process needed

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FinFET V_t Roll-Off Characteristics

Threshold Voltage, V_t [V] vs. Gate Length, L_g [nm]

NMOS / PMOS curves for W_{fin}=10nm, W_{fin}=26nm, W_{fin}=34nm

Y-axis: 1.4, 1.2, 1.0, 0.8, 0.6, 0.4, 0.2, 0.0, -0.2, -0.4

X-axis: 0, 10, 20, 30, 40, 50, 60, 70, 80

Narrow W_{fin} shows less V_t roll-off.

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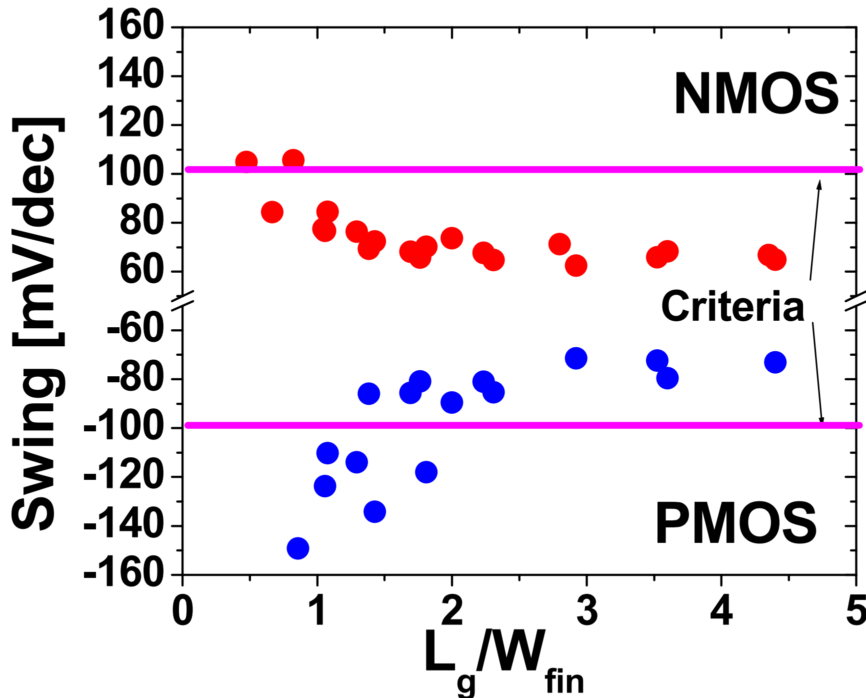
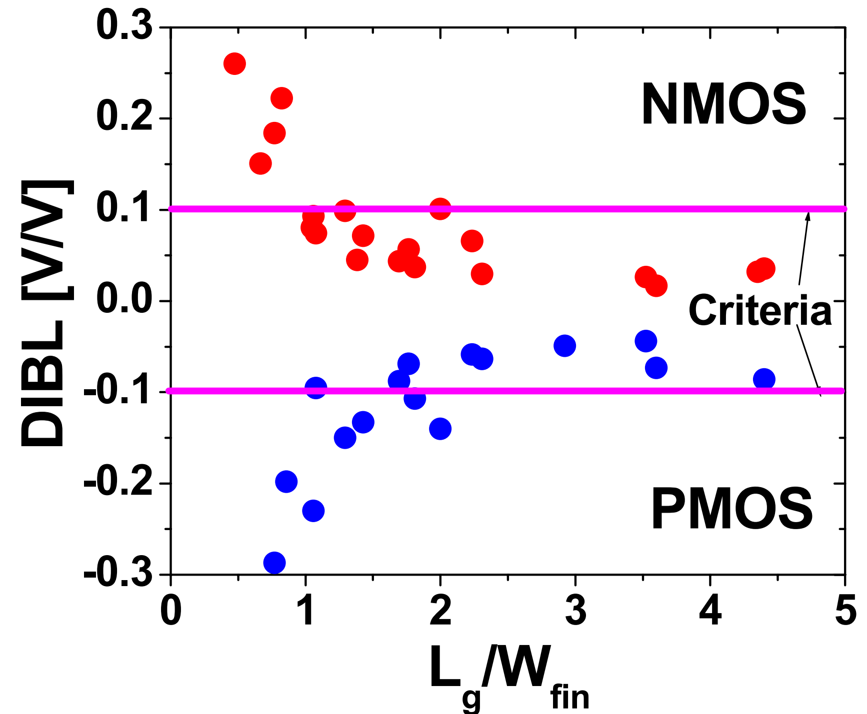
Subthreshold Swing and DIBL





When L_g/W_{fin} > 1.5, S < 100mV/dec and DIBL < 0.1V/V.

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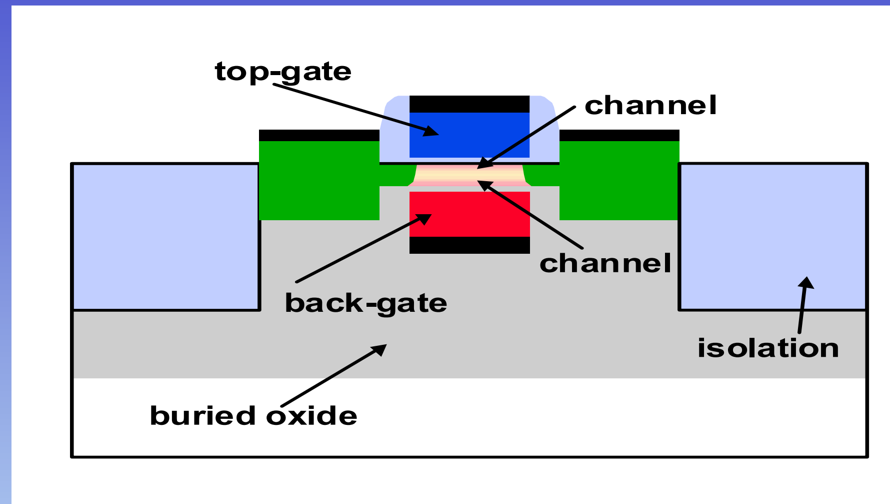
Performance of Intel's Tri-Gate p - and n - MOSFETs (Similar to the FinFET)

Company	Channel Length (nm)	n- or p- Channel	Subthreshold Slope (mV/dec)	DIBL (mV/V)	Ion (mA/um)	Ioff (nA/um)	Vcc (V)
Intel	60	n-MOS	75	45	1.18	60	1.3
Intel	60	p-MOS	70	40	-0.65	-9	-1.3

Double Gate Transistor



Advantages

- Higher drive current (I_{on})
- Improved subthreshold V_t slope
- Improved short channel effect (electrostatics)
- Stacked NAND gate

Challenges

- Gate alignment
- Silicon film thickness
- Gate stack
- Process complexity
- Accurate TCAD

Technology Scaling & Challenges

SRC

- High-κ gate dielectrics not necessary to control short-channel effects, but will be helpful for achieving high I_{dsat} (High-κ gate dielectrics will be necessary for low standby power applications)
- Parasitic resistance will be an issue for T_{Si} < 10nm
  - Raised S/D technology – but $C_{overlap}$ cannot be too high
  - Schottky S/D technology eventually needed
- Metal gate electrodes (*different from those used for classical MOSFETs*) will be needed
  - Multiple-V_t technology will require tunable metal gate Φ_M
- Structures which are provide for dynamic control of V_t are desired by circuit designers
- Strained Si (for enhanced mobility) will be difficult to achieve

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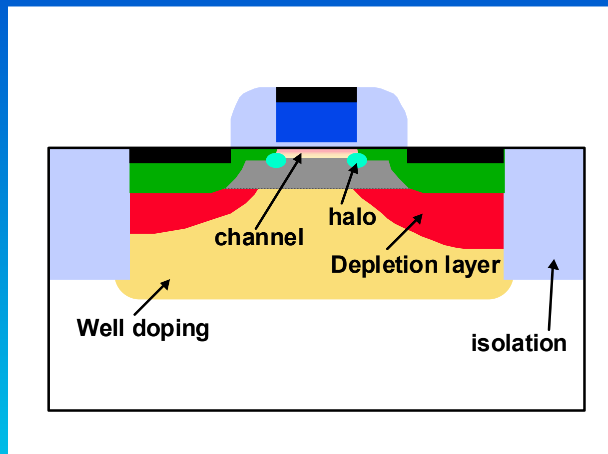
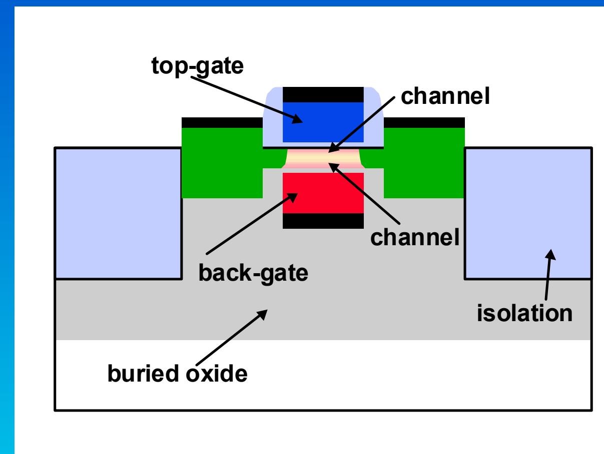
…. and Beyond

Fundamental Limits to Scaling Nanoelectronic Switch Elements

Scope of Emerging Research Devices

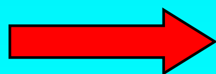




Bulk CMOS

Double-Gate CMOS

New Memory Technologies

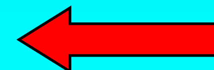


Nanotubes

Molecular devices

Quantum cellular automata

New Architecture Technologies



Emerging Information Processing Concepts

Ideal von Neumann's Computer

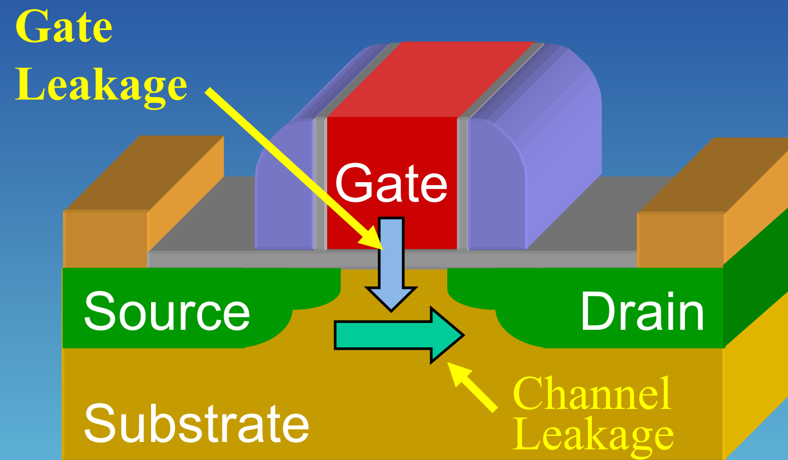
- Highest possible integration density
- Highest possible speed
- Lowest possible energy consumption

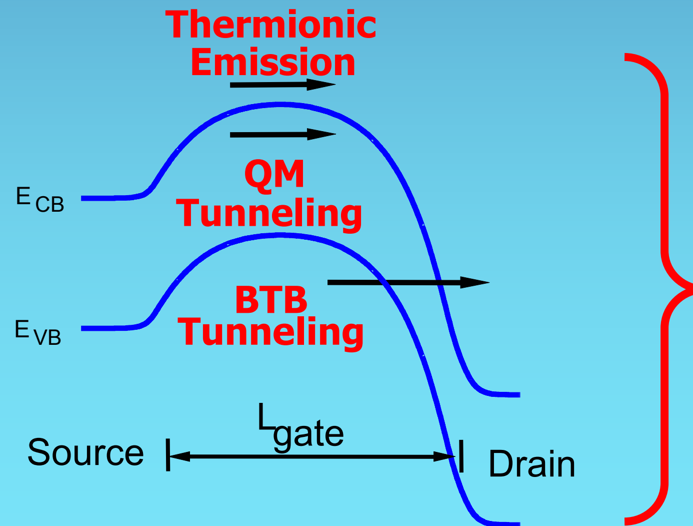
Two Questions

1. What is the best direction to pursue for alternate information processing technologies (e.g., carbon nanotubes, molecular electronics, etc.)?
   - Replicate CMOS technology with new switches, gates, etc., directly one for one sustaining the von Neumann architecture? **Or**
   - Eventually invent and develop a completely new information processing technology and systems architecture?

2. What is the best application of CMOS ***gate or switch replacement*** technologies, e.g., carbon nanotube switches or molecular switches?
   - A completely new technology embodying not only the switch, but also the interconnect, I/O, etc. (completely replace CMOS) **Or**
   - Use of the CNT or molecular switch to replace the channel of a silicon MOSFET, thus extending the silicon MOSFET infra-structure process technology for a longer time?

Field Effect Transistor Electronic Switch





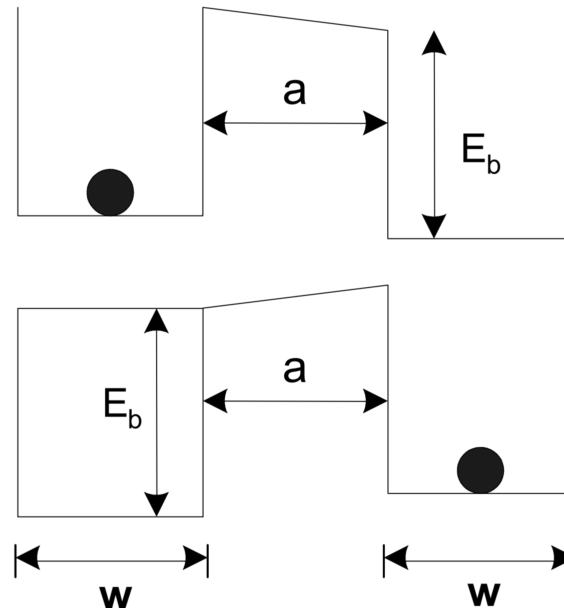
Sum = I_{off}

Channel Leakage

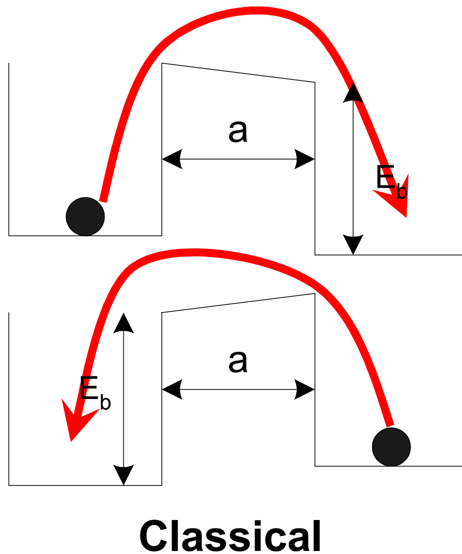
Lowest Barrier: Distinguishability Barrier

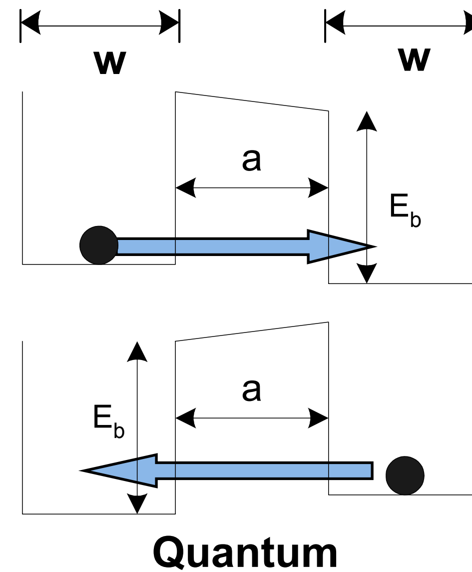
Distinguishability ***D*** implies low probability Π of spontaneous transitions between two wells (error probability)

***D=max*, Π=0** **D=0, Π=0.5 (50%)**



Classic and Quantum Distinguishability





Limit Performance of Charge Based Switch

Minimum Barrier Width $a_{crit} = 0.6\, nm$

Minimum Switch Width

Maximum Gate Density $n = 1 \times 10^{14} \dfrac{gate}{cm^2}$

Minimum state switching time $t_{sc} = 2.3 \times 10^{-14}\, s$

Total Power Consumption $P_{chip} = 2.0 \times 10^{7} \dfrac{W}{cm^2}$

Comparisons with 2001 ITRS (2016)

- Gate density
  - This analysis $n = 1.0 \times 10^{14}$ gates/cm^2
  - ITRS $n = 1.4 \times 10^{9}$ gates/cm^2
- Switching time
  - This analysis $t = 23$ fs
  - ITRS $t = 150$ fs (CV/I)
- Power density
  - This analysis $P = 2.0 \times 10^{7}$ W/cm^2
  - ITRS $P = 93$ W/cm^2
- Power density normalized to density and switching time
  - This analysis $P = 43$ W/cm^2
  - ITRS $P = 93$ W/cm^2

Comparisons with 2001 ITRS (2016)

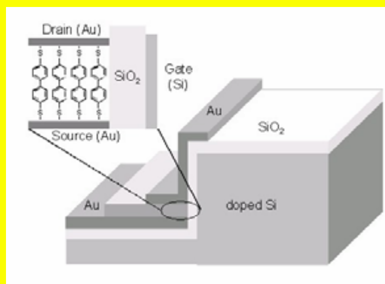
Observations

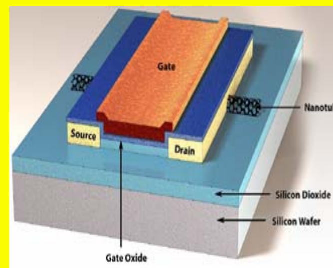
- Transistor critical dimension limited to ~ 1 nm (In the 2001 ITRS physical gate length = 9 nm for 2016)
- Power density, not critical dimension, limits gate density to ~ 1×10^9 gates/cm^2
- For the ITRS density and switching time, CMOS is approaching the maximum power efficiency

A Point of View - - -

Are the most attractive directions for research?

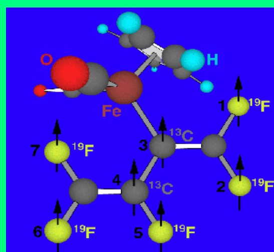
Near term

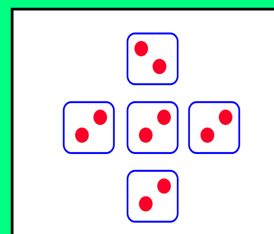




Exploration of materials and structures for integration of alternate channels in an otherwise silicon MOSFET structure.

Long term



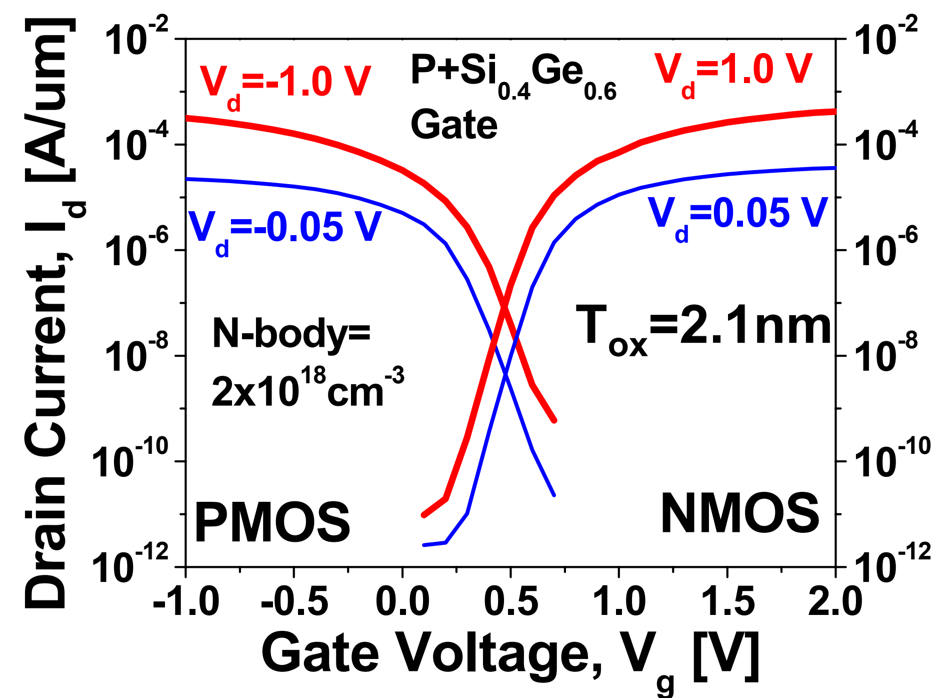


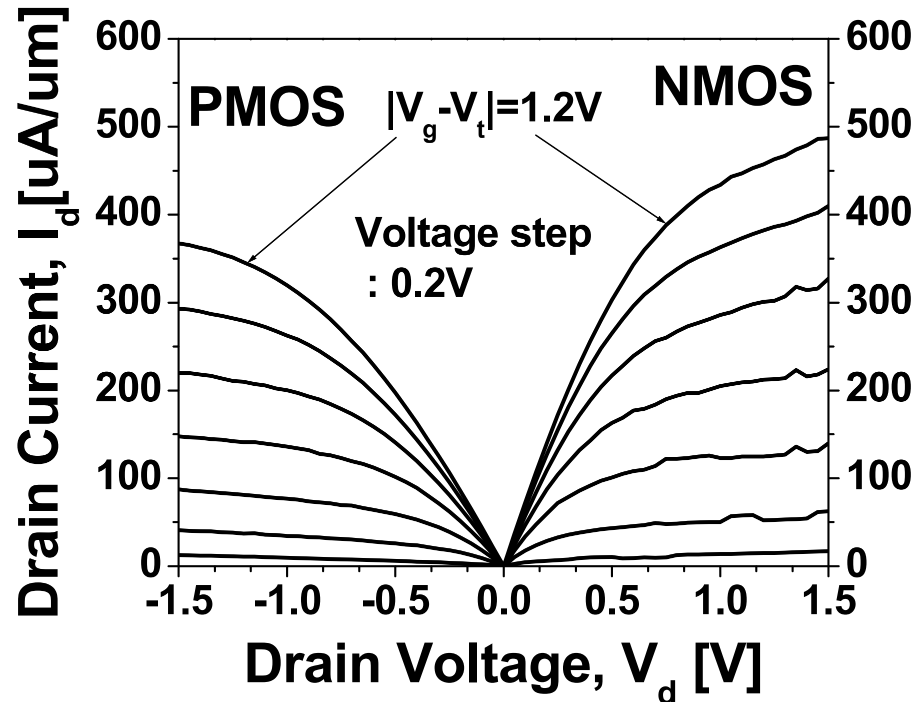
Synergistic exploration of new materials, structures and information processing architectures.

CMOS Devices and Beyond
Conclusions

- **CMOS Devices ...**
  - MOSFET Scaling Issues
    - Low Power MOSFETs WILL need High-K Dielectric in 2005
    - High Performance may stay with SiON Gate Dielectric
  - Non-Classical CMOS Structures
    - Ultra-Thin Body MOSFETs
    - Channel Engineered Structures
    - FinFETs (Good advancement by several laboratories)
    - Double Gate Structures
- **... And Beyond**
  - Potential of Molecular, Nanowire and Nanotube Electronics
    - Near Term - MOSFET-like Switches
    - Long Term - New Information Processing Technology
  - Limits on Integration Density - Power.

FinFET I-V Characteristics





L_g=15nm, W_{fin}=10nm

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