Low K & Ultra Low K
Metrology comes to the rescue

Don Frye, Carol Mohler
Semiconductor Fab Materials
1712 Building
The Dow Chemical Company
Midland, MI, USA

SiLK*
Semiconductor Dielectric

Acknowledgements

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Brian Landes for the SAX data.

D. Gidley, U of Mich. for the PALS data.

SiLKnet alliance *

* Trademark of The Dow Chemical Co.

Outline

- Introduction
- Potential Materials
  - Spin-on vs CVD
  - Low K
  - Ultra Low
- Integration Schemes & and some unit operations challenges
- Film Metrology
- Stack Metrology
- Patterned Stacks
- Conclusions

Common Low K materials

- Dow Chemical – SiLK* Semiconductor Dielectric Resin & porous SiLK* Y
  - All Organic Thermoset Polymer. Spin on application.
  - First placed into commercial production by Fujitsu at the 130 nm node.
  - porous SiLK is being evaluated for 45 nm node.
- ASM – Aurora ®
  - Organo Silicate Glass (OSG) materials. CVD application.
- Applied Materials – Black Diamond®
  - OSG material. CVD application.
- Novellus – CORAL ®
  - OSG materials. CVD application.

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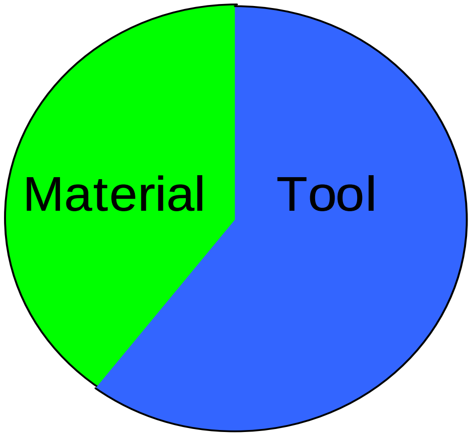
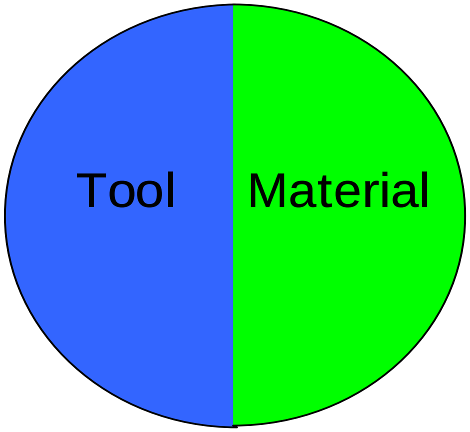
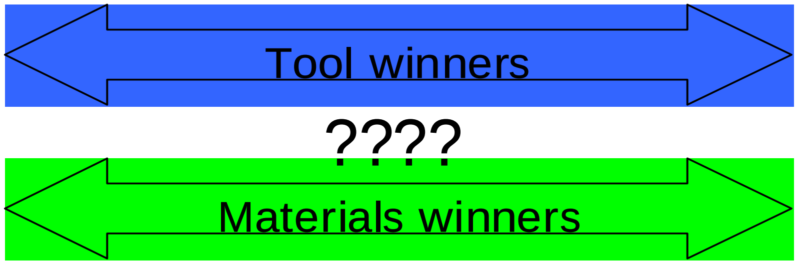
Why the CVD vs. Spin-on Issue is So Divisive -- <u>MONEY</u>


CVD Low-κ CoO
~$5.50/Layer


Spin-on Low-κ CoO
~$5.50/Layer

AMAT
ASM
Novellus

ATMI
Dow Corning
Schumacher


Tool winners

????

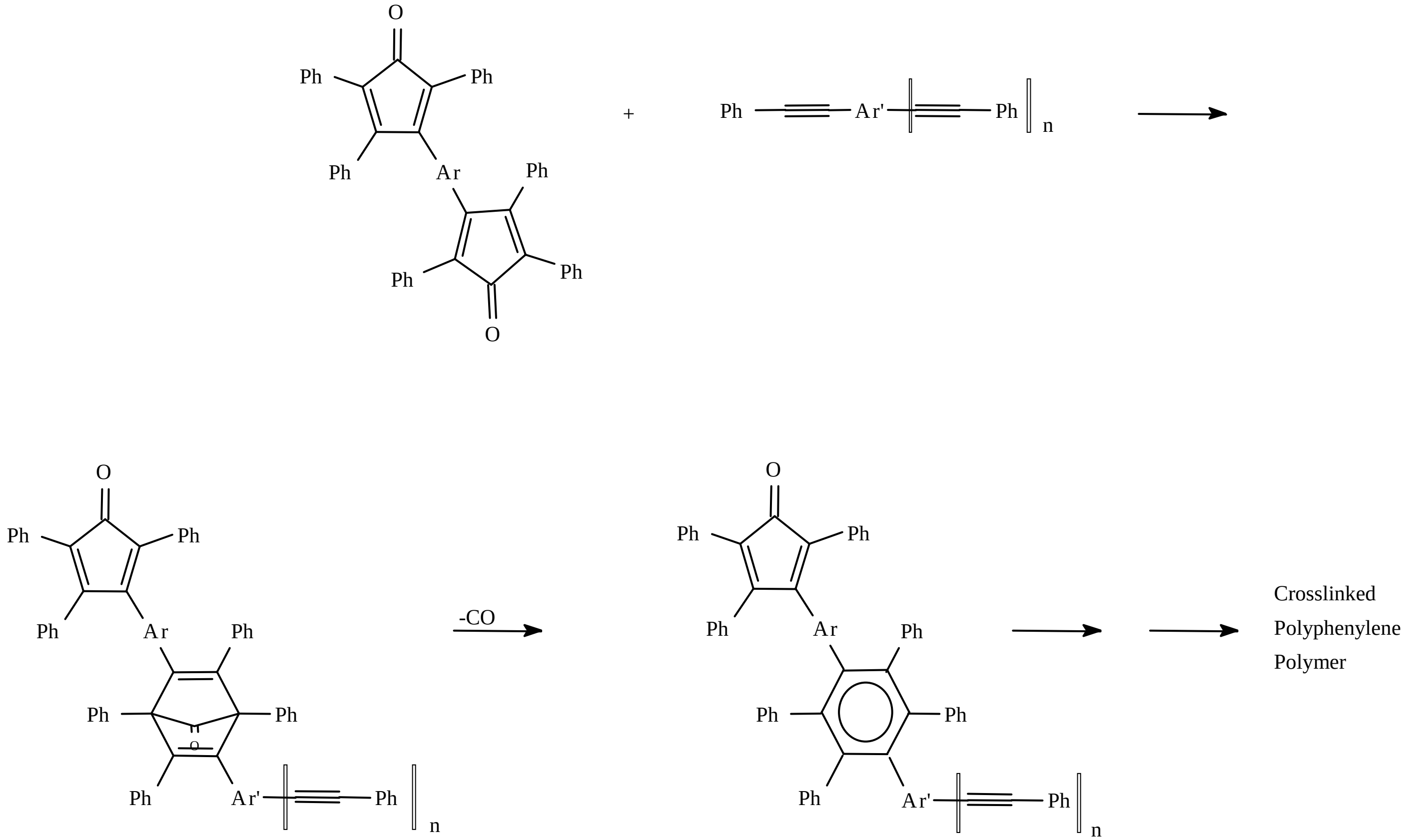
Materials winners

DNS
TEL

Dow Chemical
Honeywell
JSR
Shipley

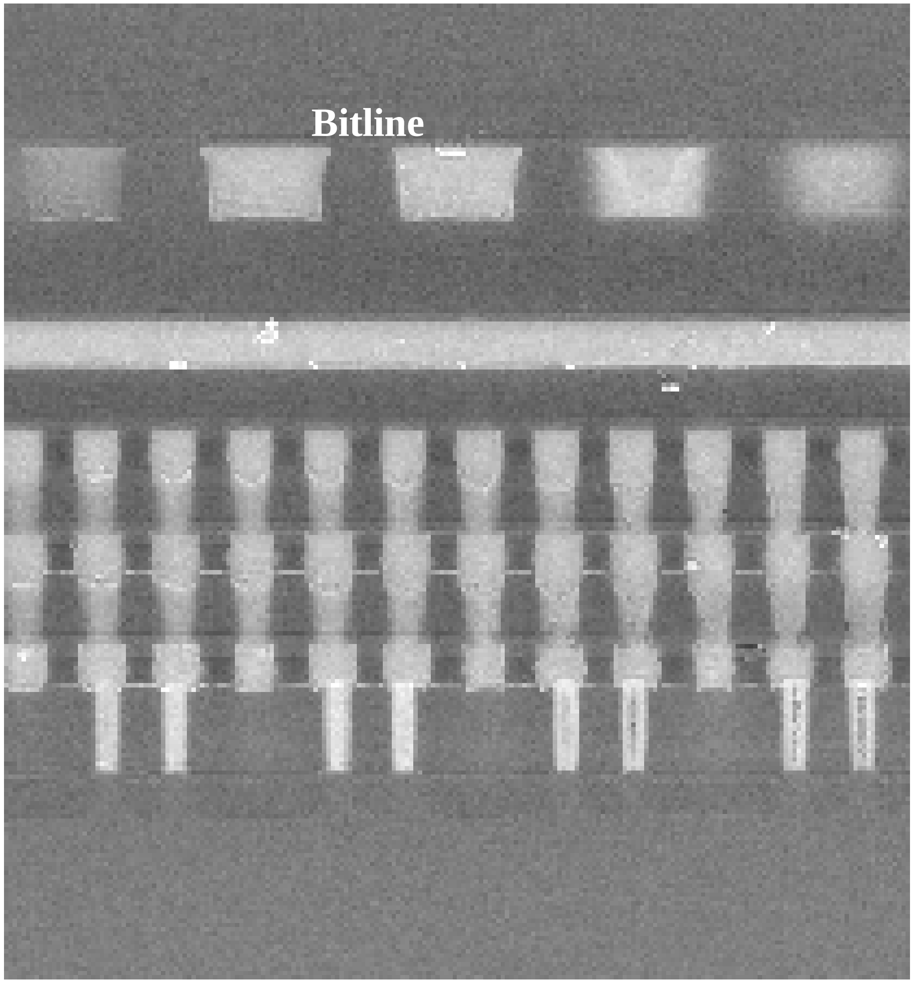
Organic Dielectric Films

- SiLK film– all organic dielectric



Cross sectional view of Fujitsu’s 130nm manufacturing technology.

Hybrid ILD

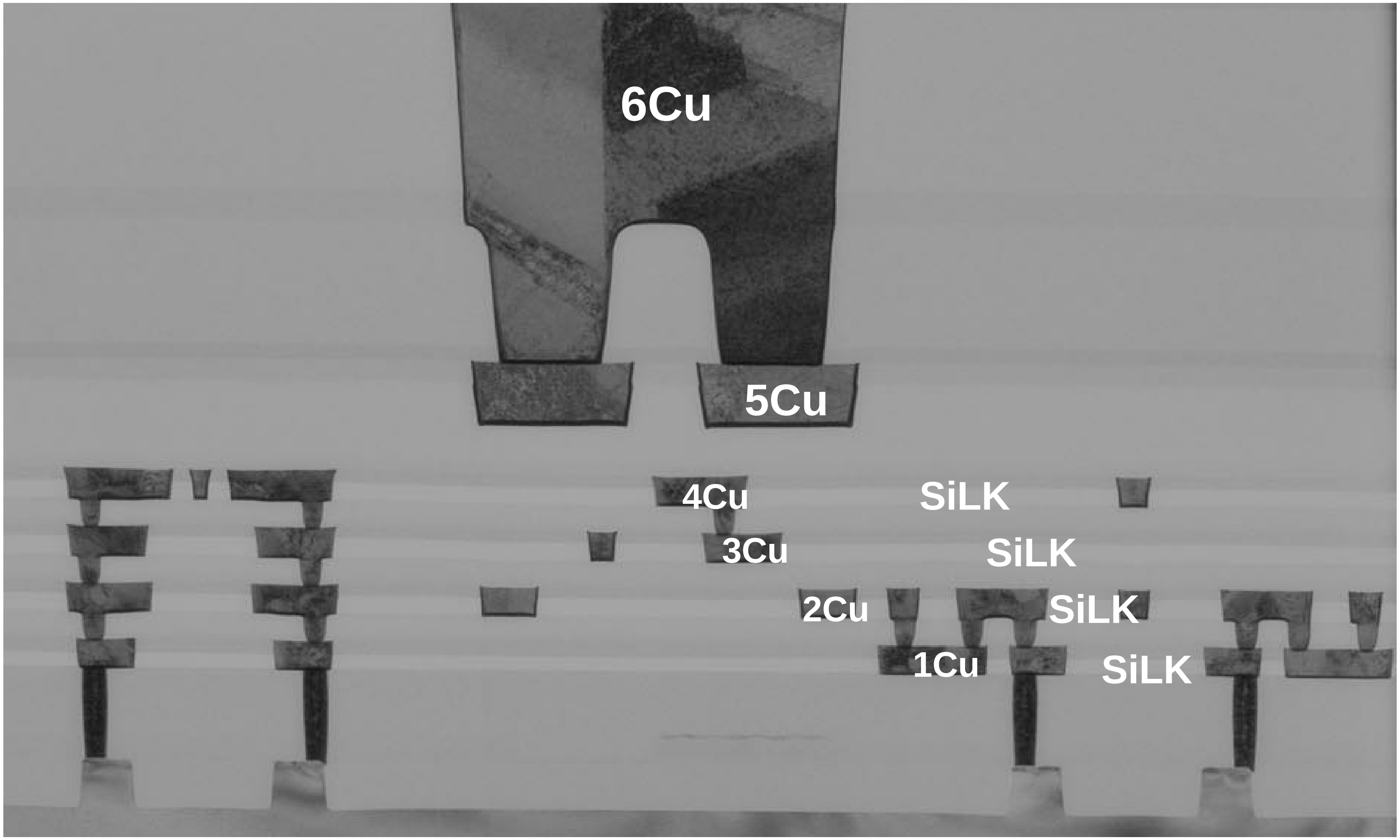


Courtesy of Fujitsu Ltd

Hybrid ILDs

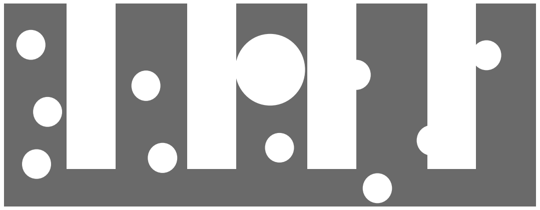
Courtesy of Toshiba & Sony

6 Levels Cu-DD/Low-k ILD Interconnect Structure for 65nm Node High Performance SoC



Porous Technical Challenges

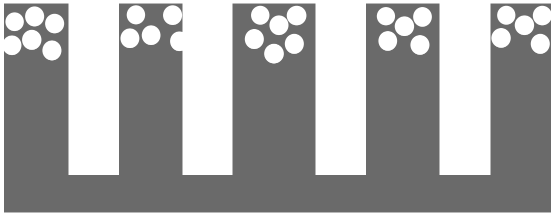
Small Pore Size



...protection from
electrical shorts

and

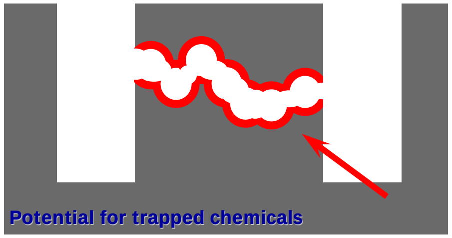
Uniform Distribution



...mechanical integrity,
dielectric performance

and

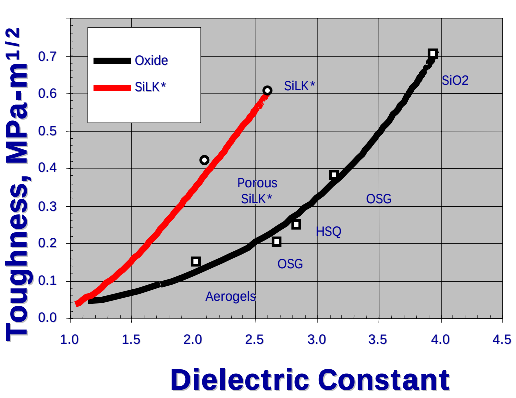
Closed Pore System



...protection from trapped
mat'ls, device yield

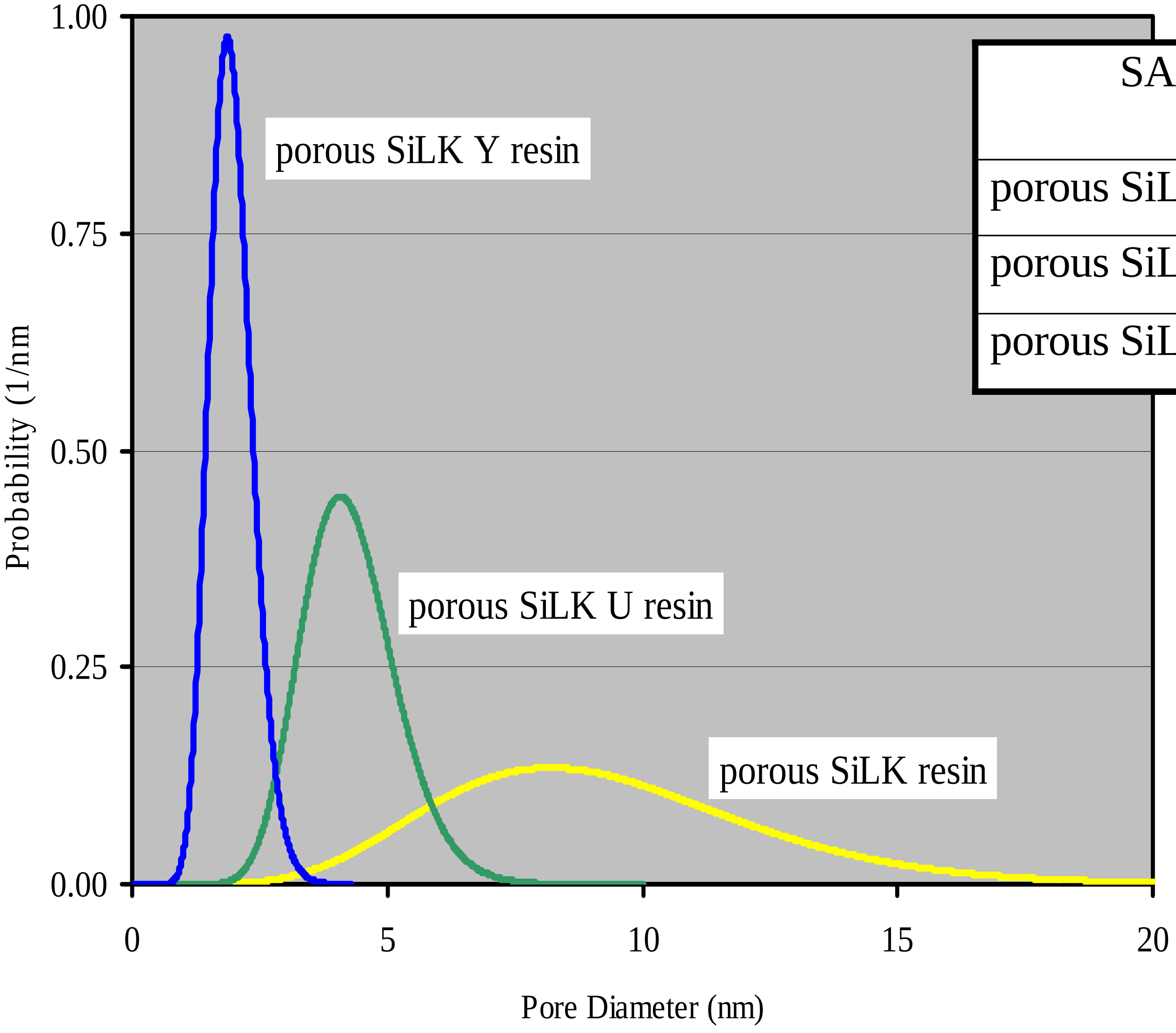
and

Fracture Toughness



Metrology Help Needed Here

SAXS Pore Size Distribution



SAXS	Average pore size	Pore size range
porous SiLK resin	8.2 nm	2.2 – 19.3 nm
porous SiLK U resin	4.4 nm	1.9 – 7.0 nm
porous SiLK Y resin	1.9 nm	0.9 – 3.2 nm

- On-wafer small angle x-ray scattering
- Highly reliable tool for porous SiLK system
  - Extensive model development
  - Pore size distribution determined at 99.5% confidence level

Landes et al, MRS Spring 2003

Pore Size by TEM & PALS

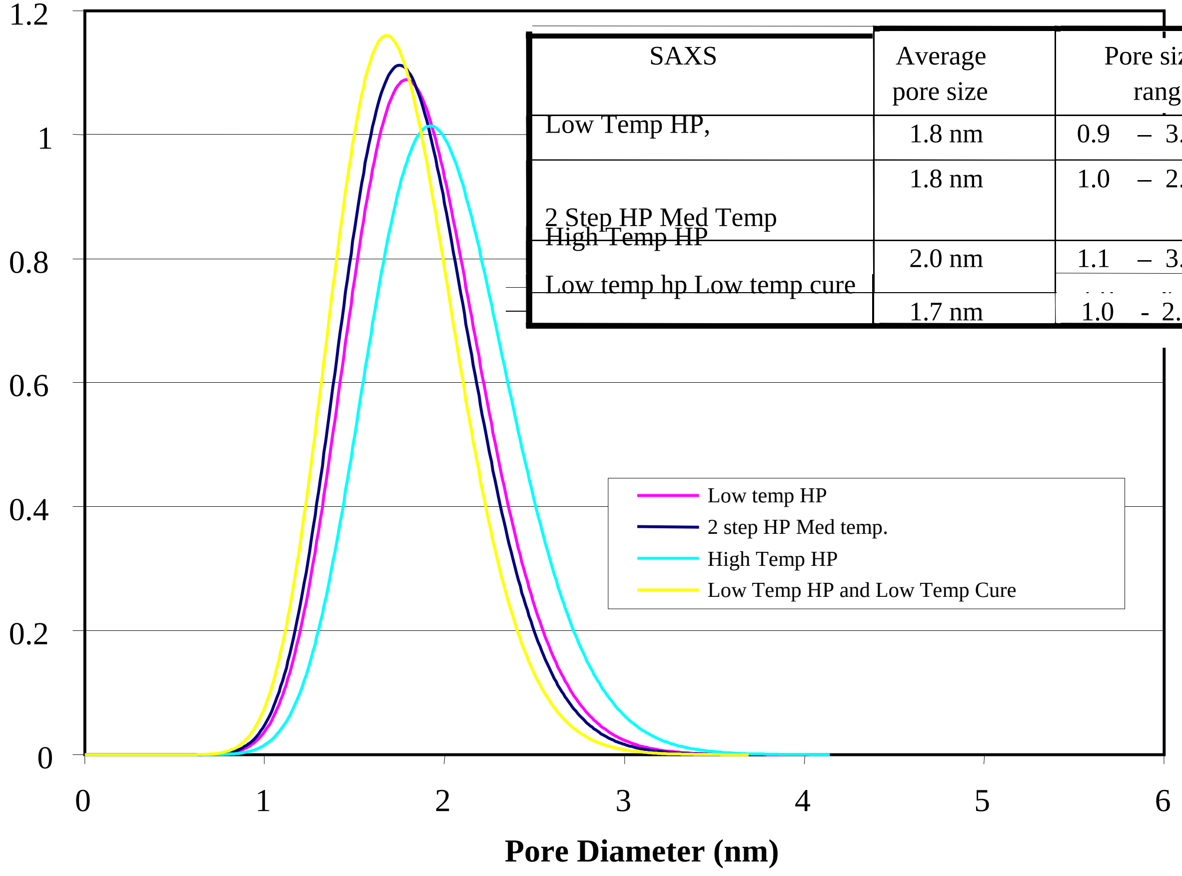
- PALS provides secondary confirmation of pore size

PALS	Cylindrical model	Spherical model
Mean free path	1.8 nm	1.5 nm

courtesy University of Michigan Positron Group

- Pores not visible by TEM
- TEM confirms absence of large pores

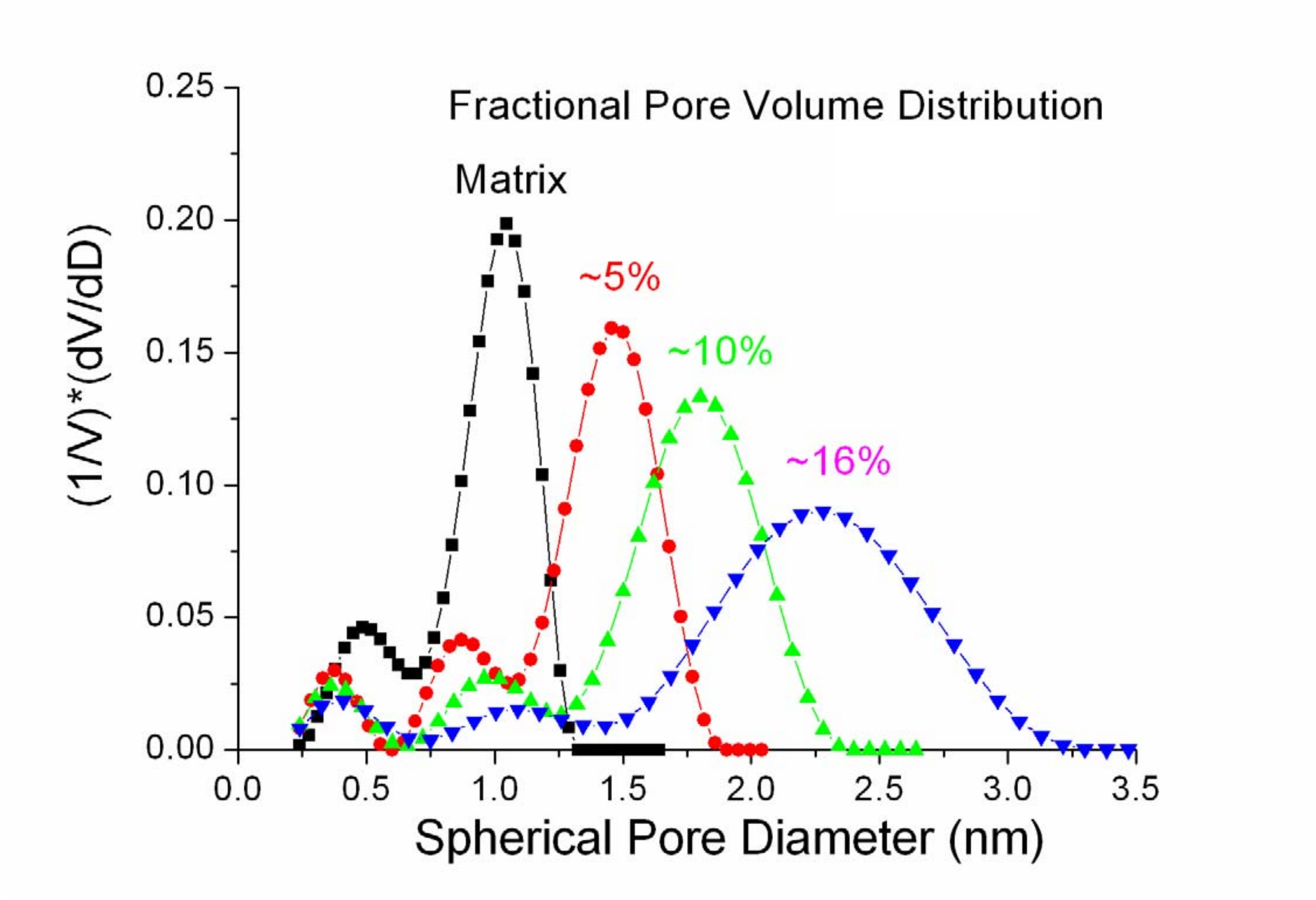
SAX - Hot Plate Bake Process Window



SAXS	Average pore size	Pore size range
Low Temp HP,	1.8 nm	0.9 – 3.0 nm
2 Step HP Med Temp	1.8 nm	1.0 – 2.9 nm
High Temp HP	2.0 nm	1.1 – 3.2 nm
Low temp hp Low temp cure	1.7 nm	1.0 - 2.8 nm

PALS – Pore Volume vs Pore Diameter

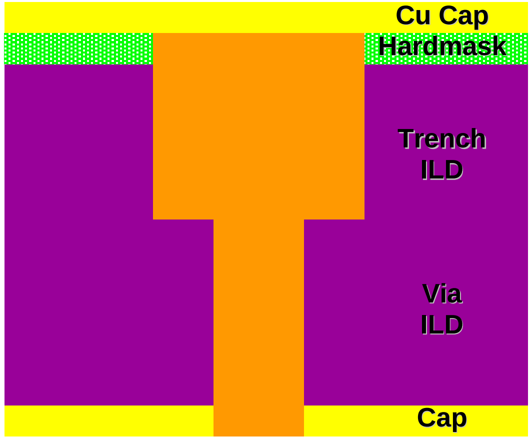
for porous SiLK Y like materials



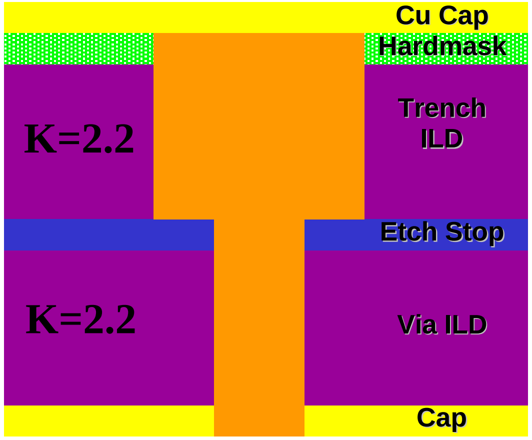
Hybrid integration

- Hybrid implies the use of 2 different inter-dielectric Materials per level
  - Via level : Coral (SiOCH)
  - Trench level : porous SiLK Y resin (org. polymer)
- Exploits the material differences to broaden process window
  - Etch selectivity, mechanical properties, Thermal Conductivities etc
  - Allows full via first allowing the highest design rule accuracy wrt misalignment
- Hybrid allows an elegant trade-off between performance and process window

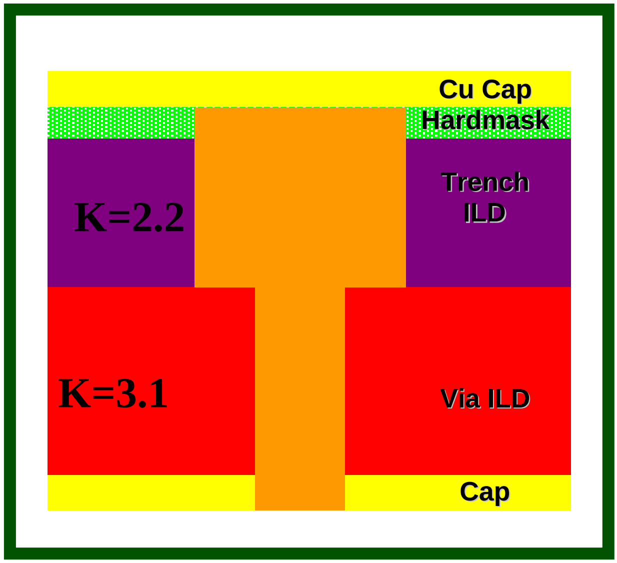
Integration vs performance



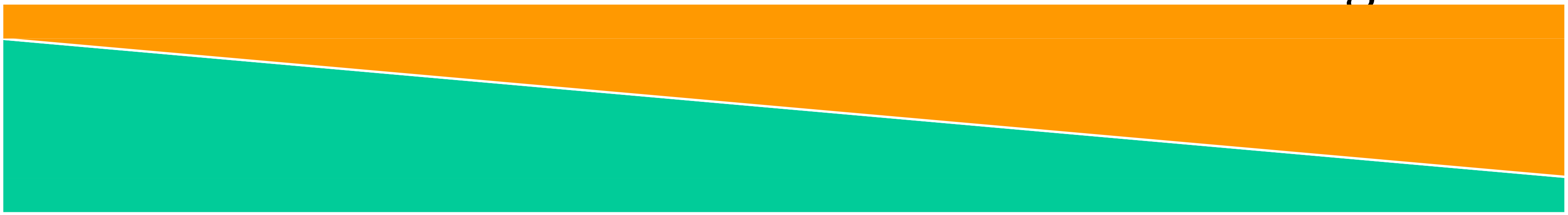
Full SiLK



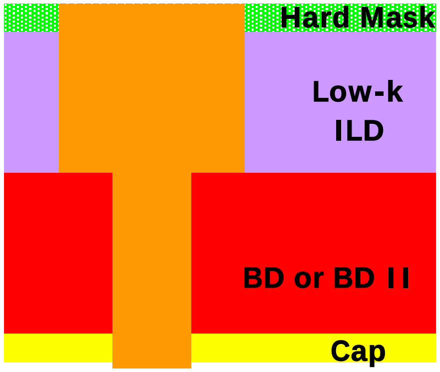
Buried
Etch Stop



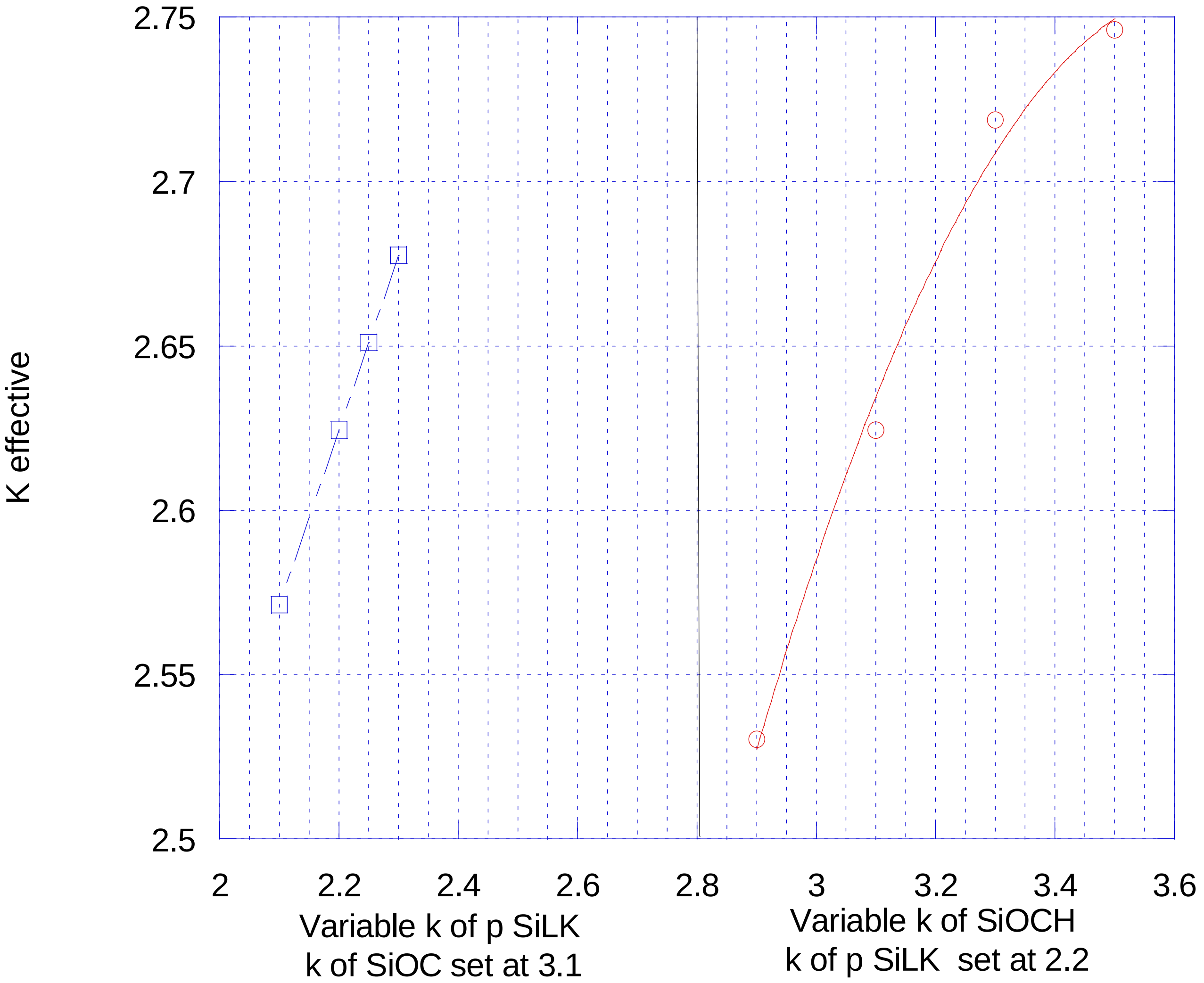
Hybrid ILD
Integration



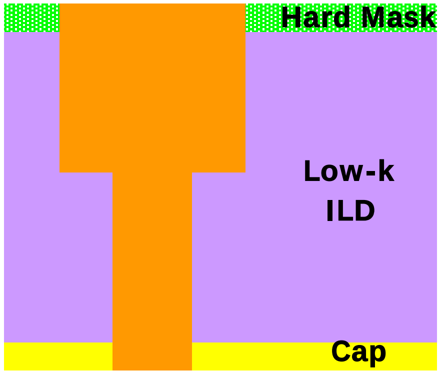
Performance and sensitivity



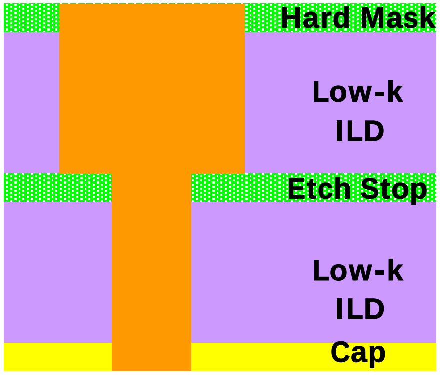
"Hybrid"



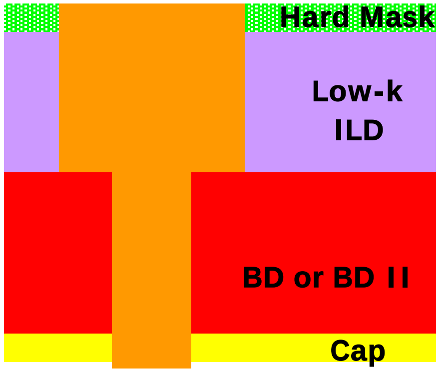
Low K Hardmasks can be CVD or Spin-on



Low-k w/Timed Etch



Low-k w/Etch Stop



“Hybrid”

Hybrid Hardmask

- ENSEMBLE* Dielectric Coatings is a new complimentary product to the Organic dielectric films. The material is actually an Organo-Silicate, but its inorganic properties are key here.

Material	Layer
ENSEMBLE HM	Top Hardmask- Inorganic
ENSEMBLE EB	Etch buffer layer - Organic
ENSEMBLE CS	CMP Stop - Inorganic
ENSEMBLE ES	Etch Stop Layer - Inorganic

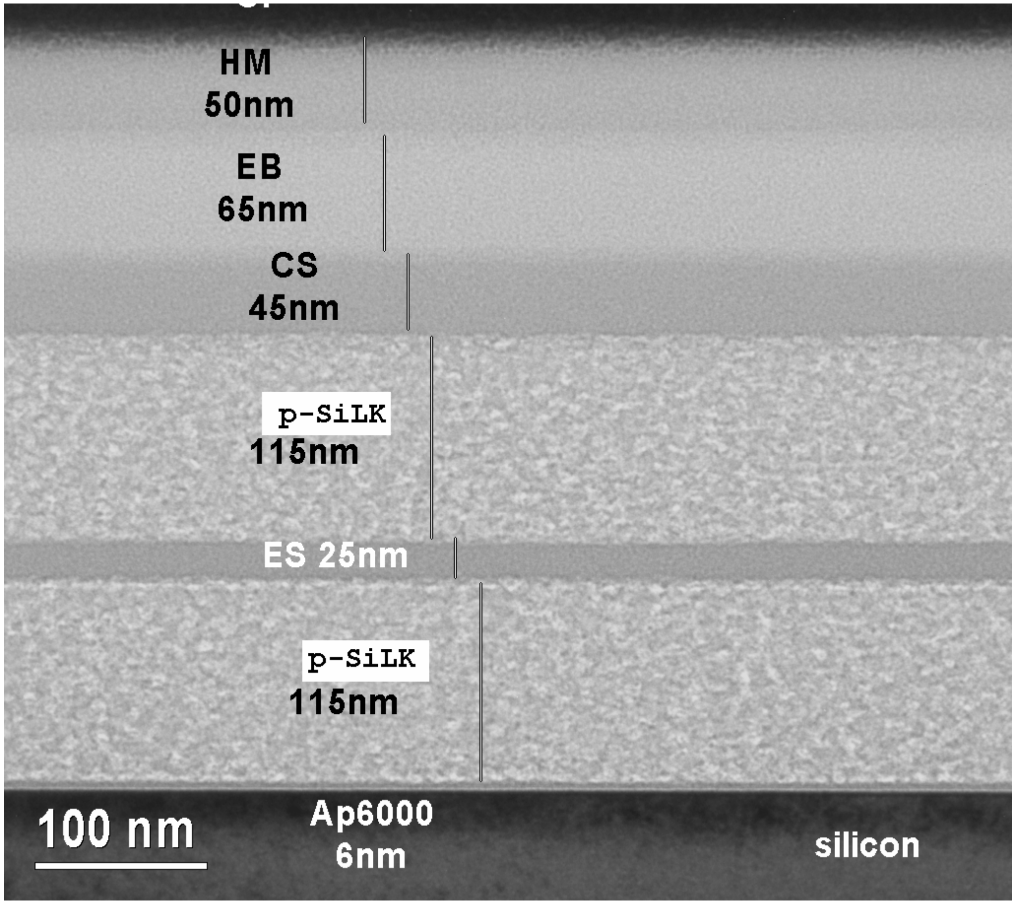
*Trademark of The Dow Chemical Co.

Integrated Stack Concept

Alternating *Chemistries in the Dielectric Stack*

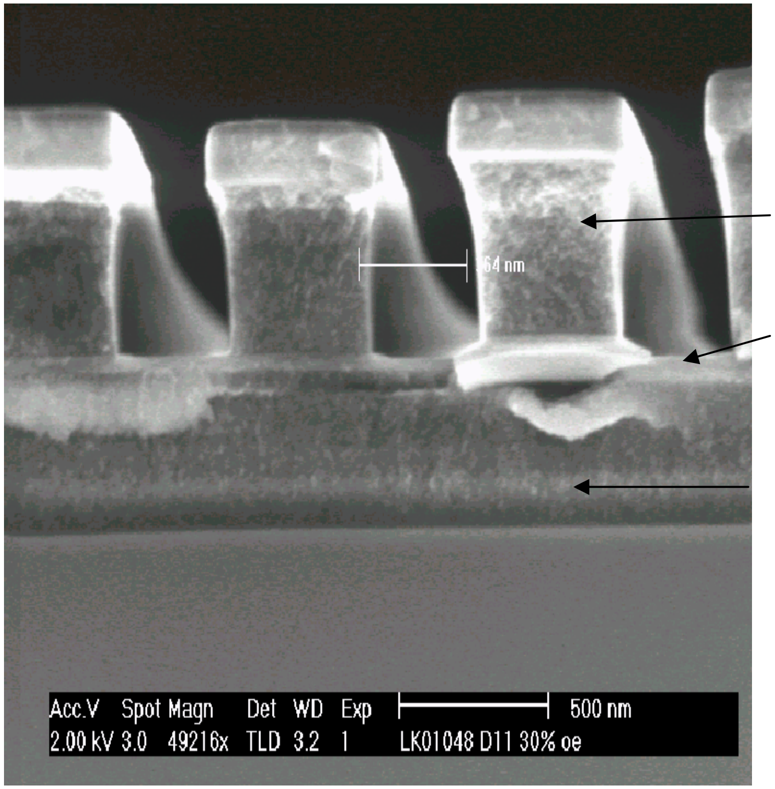
- Facilitates pattern formation in Etch
- Only requires 2 chemical families - simplifies module development (etch and clean)
    - SiLK, EB - hydrocarbon --> O2 etch
    - ES, CS, HM - Organosilicate--> CFx/CHxFy etch
- Entire stack of dielectric layers applied in one pass on a spin track
- The layers are optimized for compatibility

TEM of all Spin on Stack



Patterned Spin on Stack

Are we ready for barrier deposition?



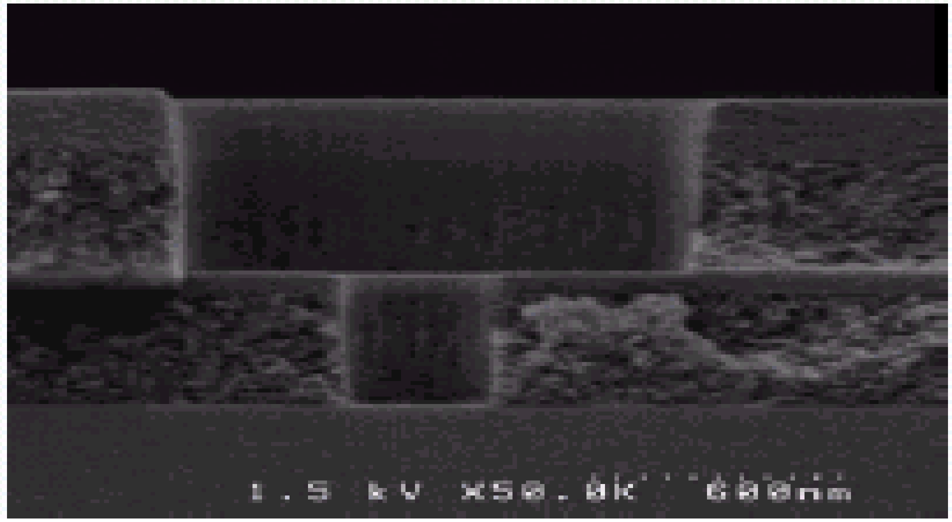
SiLK

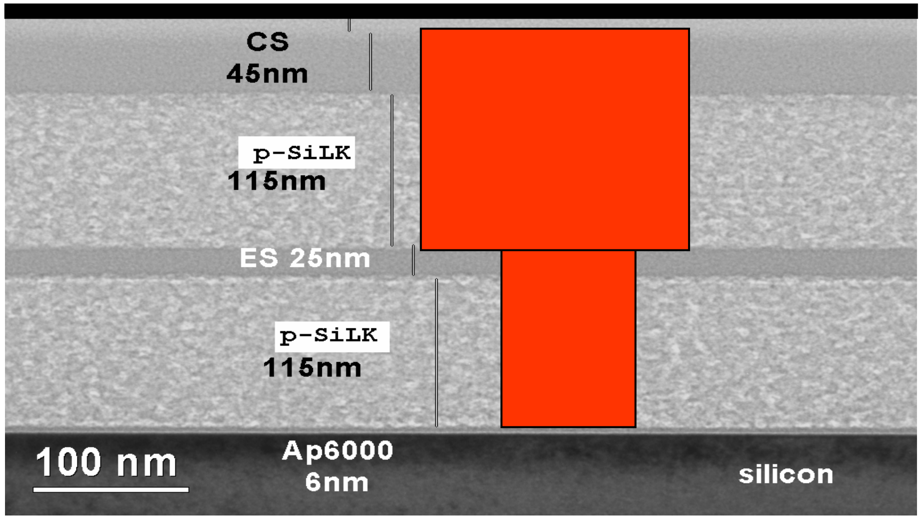
ENSEMBLE ES

SiLK

Photo courtesy of IMEC/Philips Research Leuven

All Spin On BEOL - porous-SiLK/ENSEMBLE Pattern Stack





RI changes of SiLK films after wet clean

Cleaner	% change in Refractive Index
ACT® NE-28	-0.24
ACT BNE-8000	-1.03
ACT BNE-8500	-0.36
ACT 970	0.12
ACT XT 1100	1.73

®Trademark of Ashland-ACT

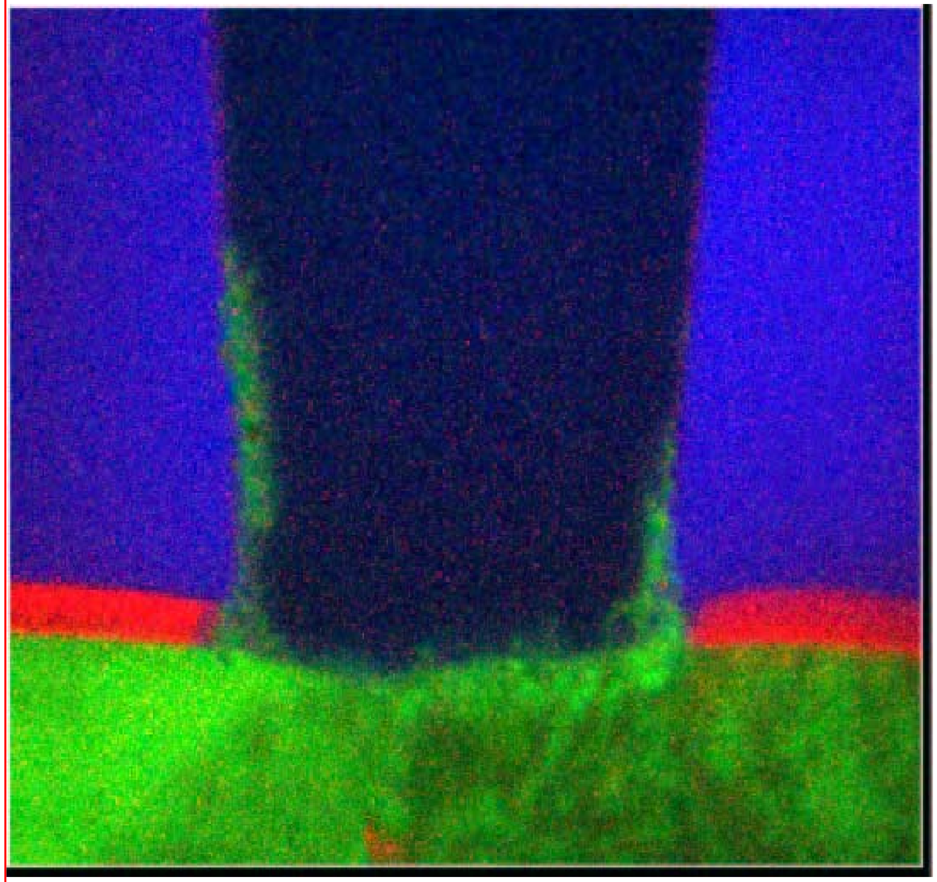
RI changes of porous SiLK films after wet clean

Cleaner	% change in Refractive Index
ACT® NE-28	-1.51
ACT BNE-8000	-0.33
ACT BNE-8500	5.32
ACT 970	0.07
ACT XT 1100	-0.73

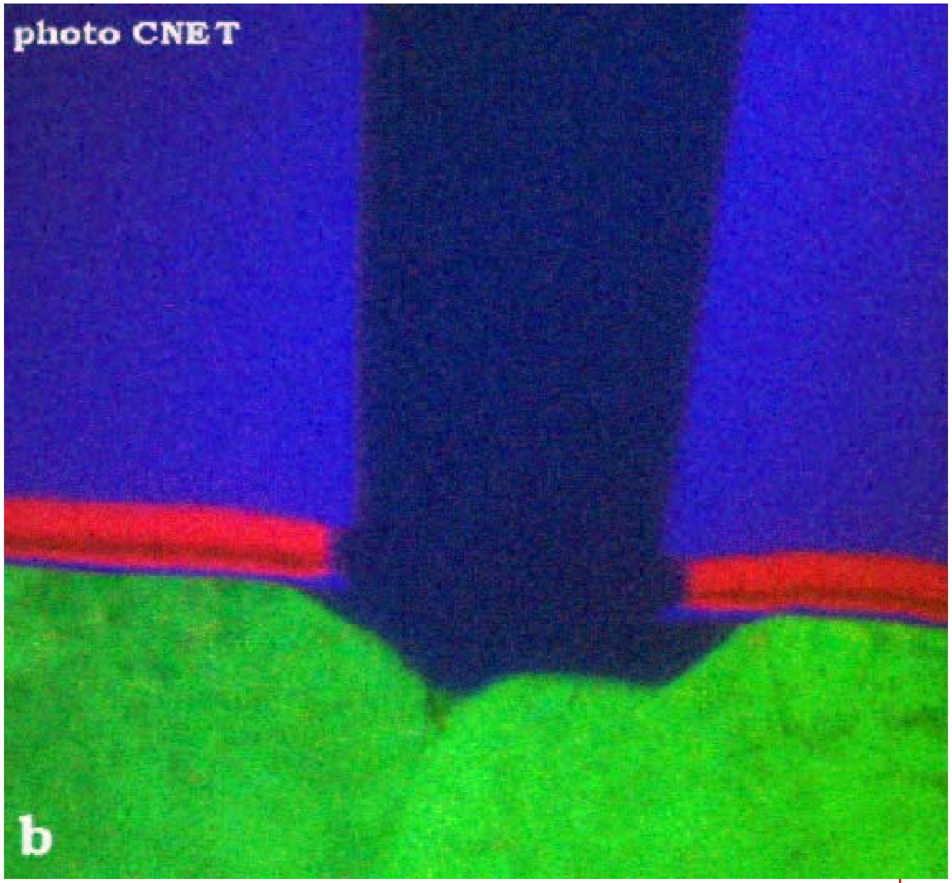
RI changes of ENSEMBLE films after wet clean

Cleaner	% change in Refractive Index
ACT® NE-28	-0.0
ACT NE-89	-0.88
ACT NE-111	0.0
ACT 970	-0.54
ACT BNE-8500	0.41

Copper Removal from Sidewall (Wet or Dry)



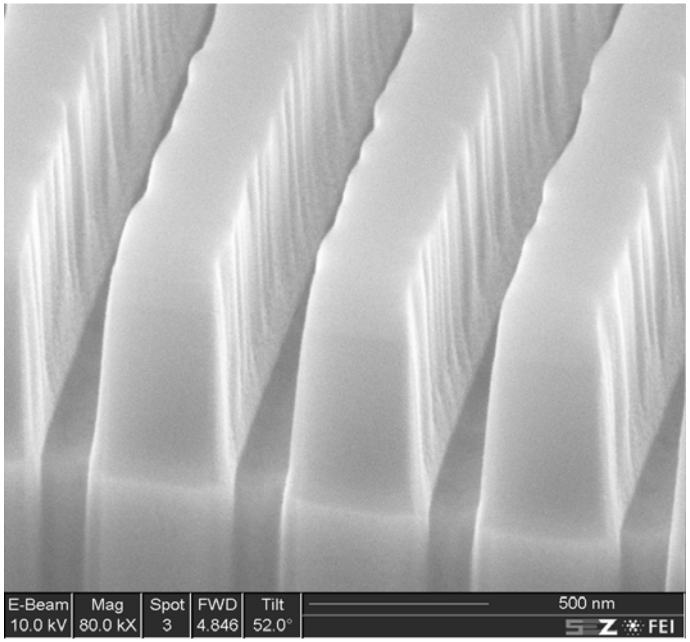
Before Wet Clean



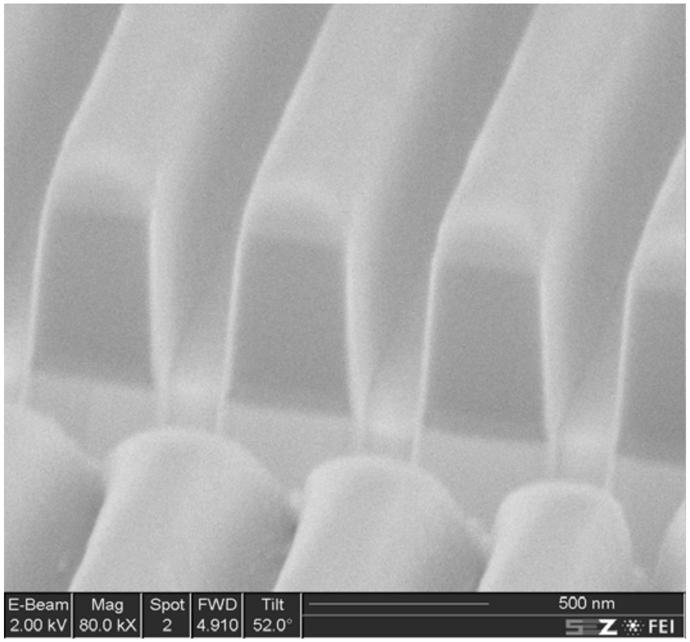
After Wet Clean

* Courtesy of EKC

Cleaning of Etched SiLK Structures



Pre-Clean



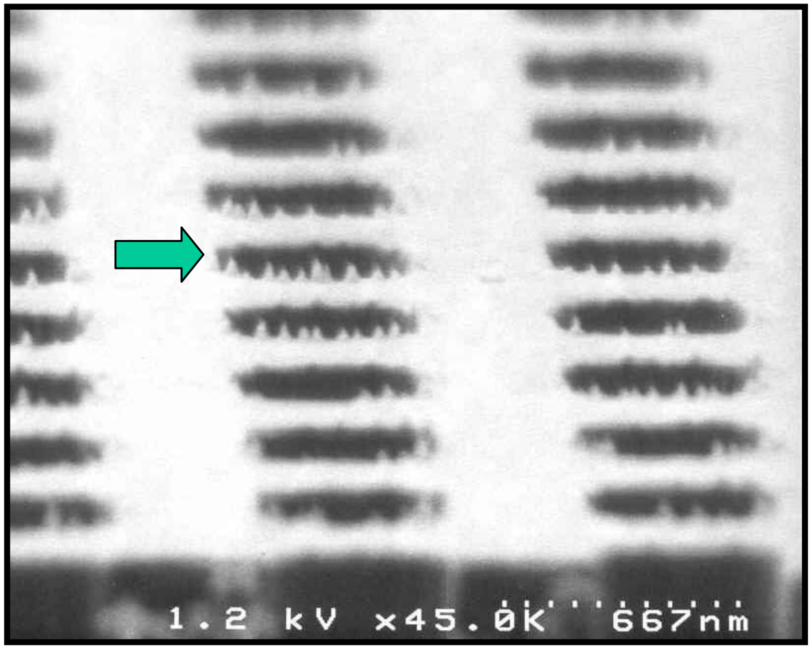
Cleaning Solution from Vendor A

But, is it really clean?

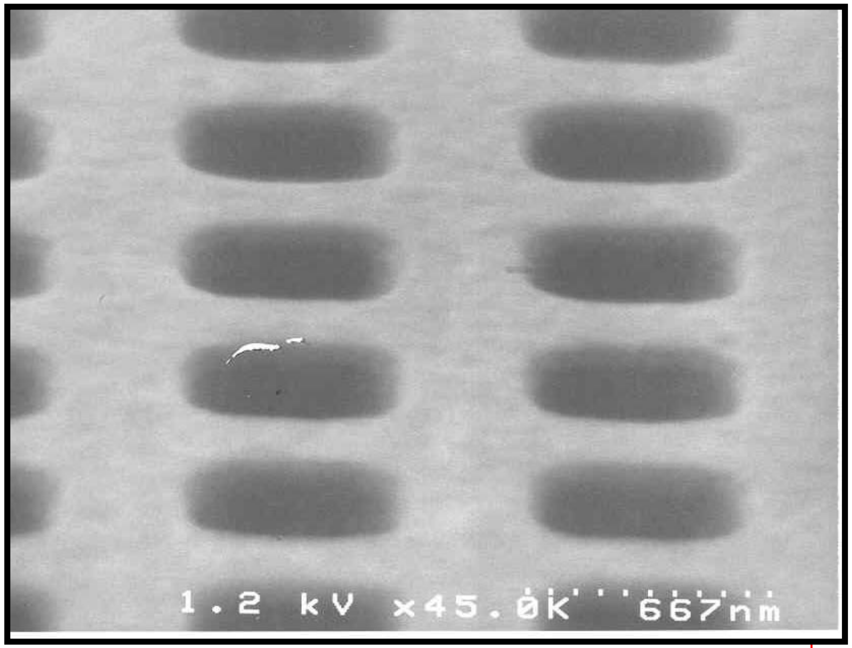
Courtesy of SEZ

Post Etch Clean of Porous SiLK Film

Before wet clean processing



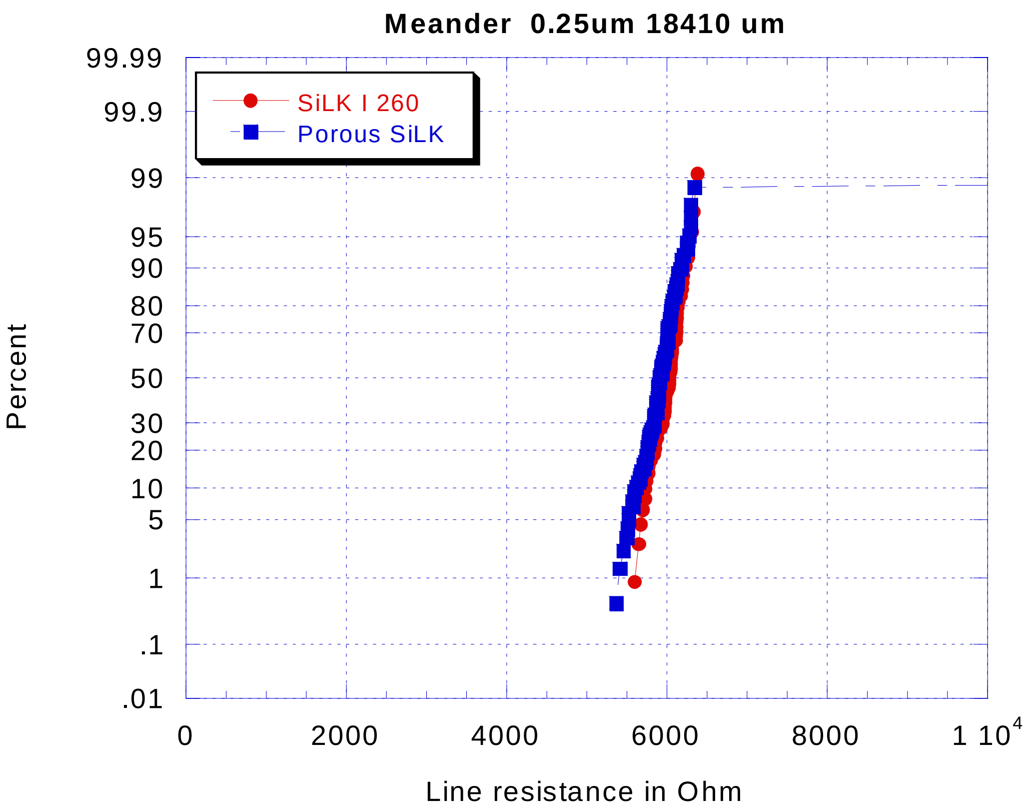
After wet clean processing



- Depending on the etch chemistry, in-situ deposition of polymers may occur
- Post etch clean removes this material prior to metallization
- Cleaning similar to dense SiLK film

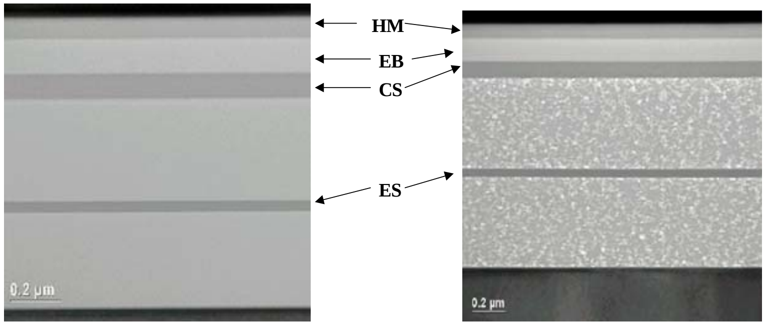
Single damascene integration of SiLK dielectric and porous SiLK dielectric using the identical wet clean processing with EKC 525

Single Damascene Integration
18 mm Meanders



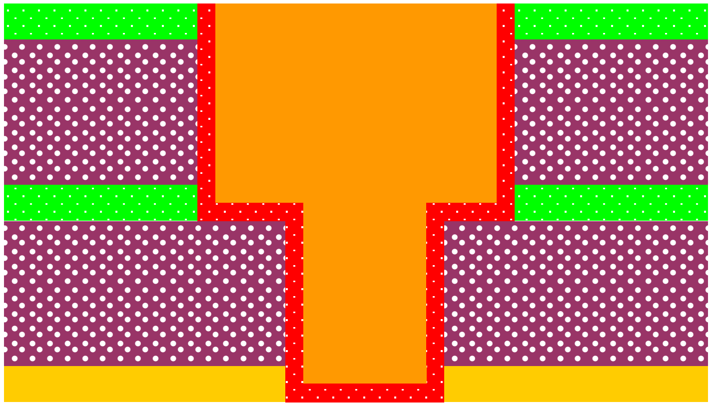
Courtesy of IMEC

SiLK Integrated Stack



Dense SiLK Stack

Porous SiLK Stack



Spin-on ENSEMBLE CS

Spin-on porous SiLK

Spin-on ENSEMBLE ES

Spin-on porous SiLK

CVD Barrier (SiC/SiCN)

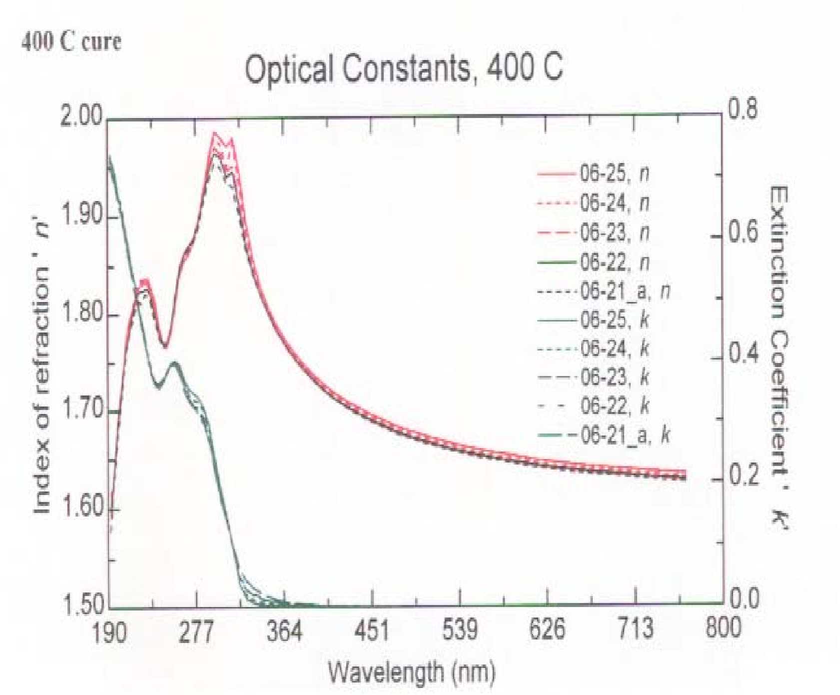
CMP copper, CMP TaN,
stop on ENSEMBLE **CS**

Issues to implement

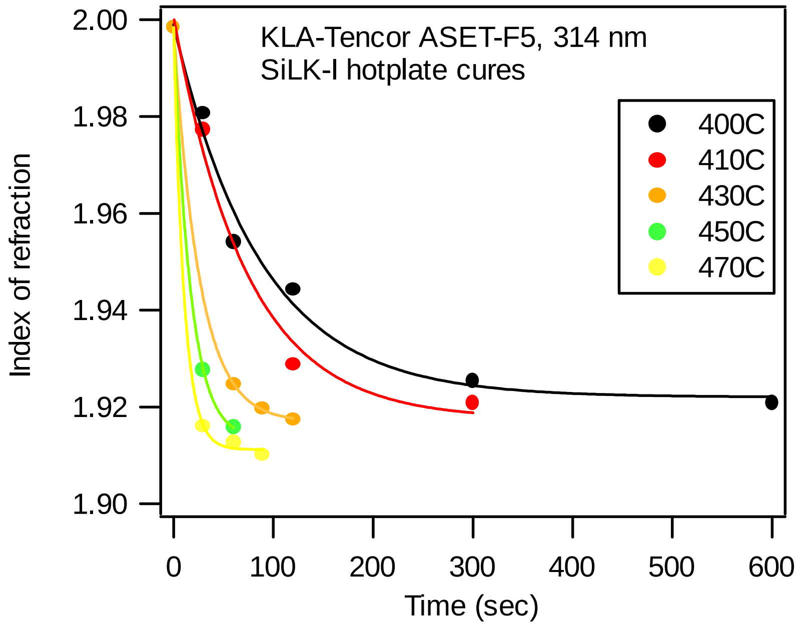
- Stack RI
  - Void fraction
  - Degree of Cure
  - Layer thickness
- Stack SAX – Porous or some other imaging of the Pores
- Barrier integration
  - 3D AFM
  - EP
- Effect Clean / process chemicals

Optical Constant Cure Method

- Most semiconductor fabs monitor cure of SiLK films by changes in optical constants (index of refraction), using ellipsometry
- Ellipsometric measurements are non-destructive, done on-wafer
- The index of refraction at 314 nm correlates with cure level of SiLK films



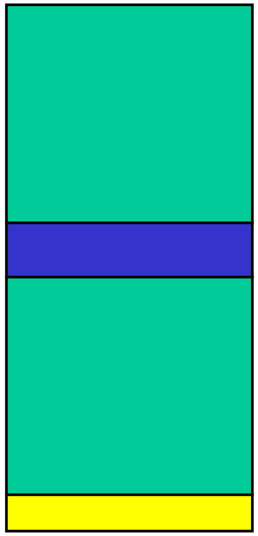
(Yang et al, Micro, 2000)



(Srivatsa et al, Yield Management, 2000)

SiLK-I/ENSEMBLE/SiLK-I/AP stack

Thickness
RI@314nm

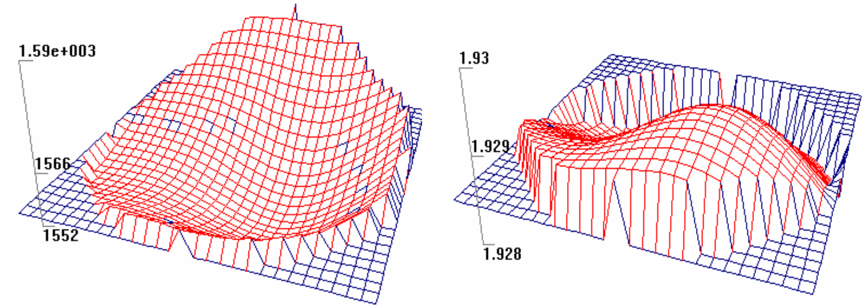


SiLK-I

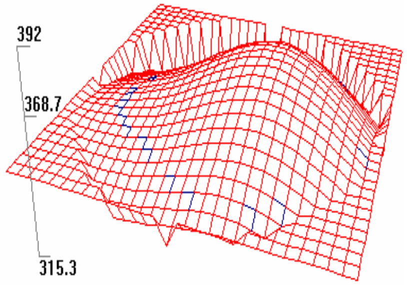
ENSEMBLE

SiLK-I

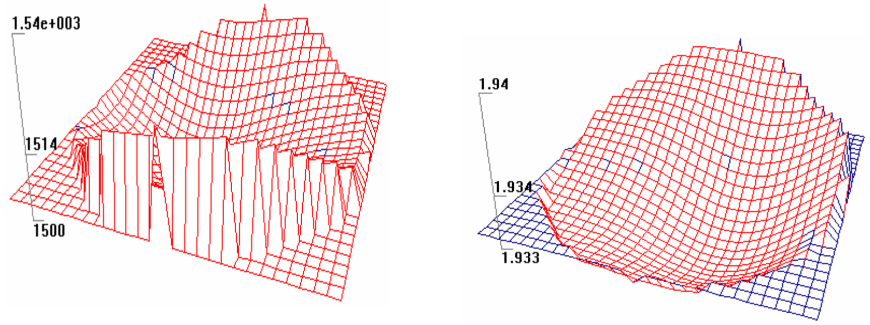
AP6000



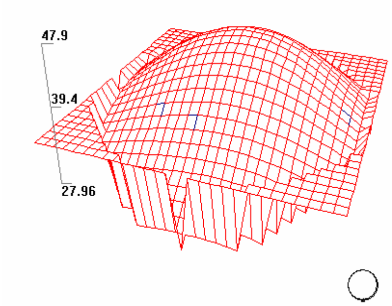
1565 ± 9 Å
1.9287 ± 0.0005



368 ± 15 Å

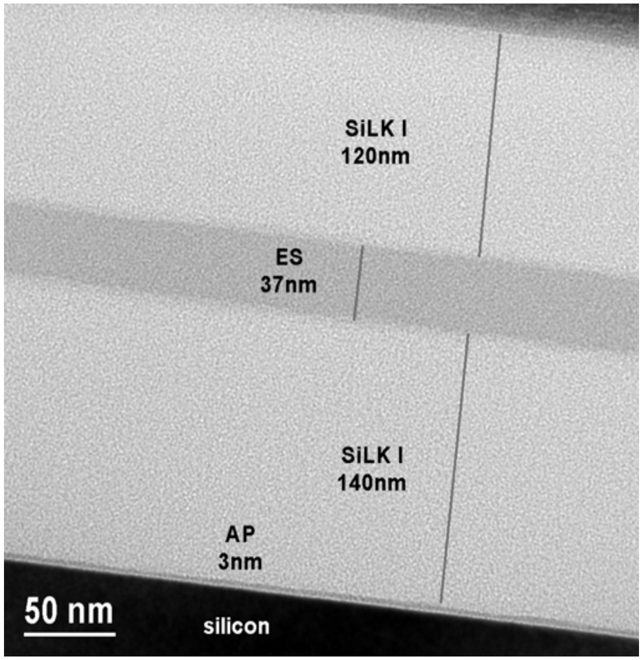


1513 ± 9 Å
1.9340 ± 0.0007



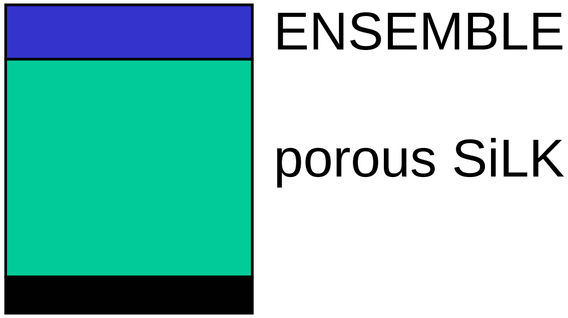
40 ± 5 Å

SiLK-I/ES/SiLK-I/AP stack thicknesses

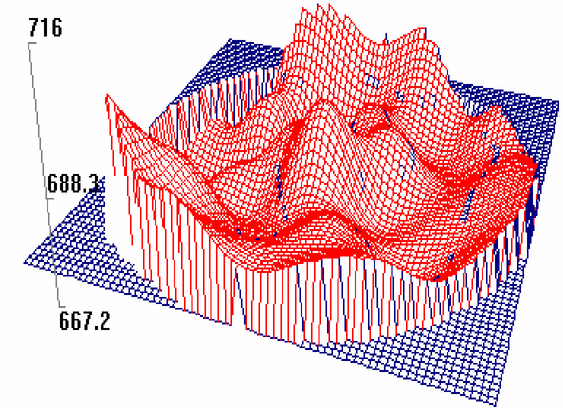


	Ellipsometry	TEM	XRR
SiLK-I	1565 ± 9 Å	1200 ± 60	1545
ES	368 ± 15	370 ± 20	348
SiLK-I	1513 ± 9	1400 ± 70	1623
AP 6K	40 ± 5	30 ± 3	--

Porous SiLK/ENSEMBLE stacks

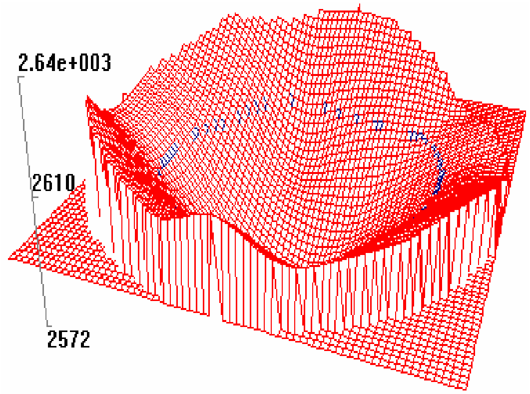


ENSEMBLE:

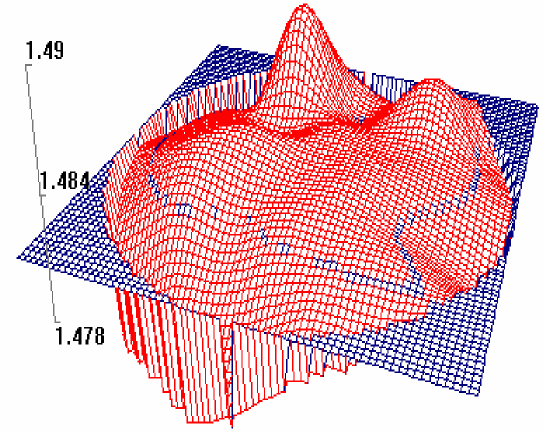


690 ± 10Å

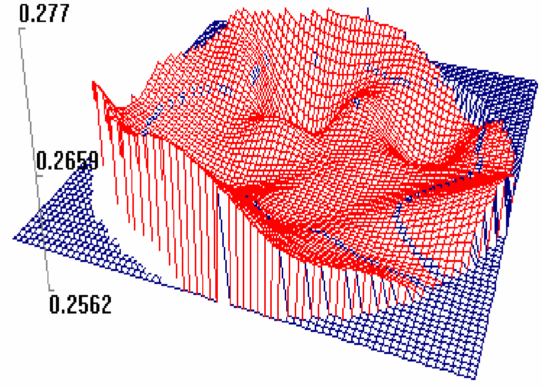
porous SiLK:



2615 ± 17Å



RI 1.484 ± 0.002



Pore Volume 26.7 ± 0.4 %

Conclusion

- Spin-on Stacks will reduce the total Dielectric constant of the structure. Plus, combined with Hybrid integration good reliable structures can be made.
- Many parts of the metrology solutions are out there.
- Integrated Metrology does not exist yet.
  - Multilayer stack with porosity.
  - Metrology value correlated to good structures.
- Low cost high throughput metrology has yet to be proven for 45 nm and beyond.
- The CoO of the all Spin on Stacks is competitive vs CVD stacks.