Metrology for Nanoelectronics:
The Impact of Nano-Sized Dimensions on Characterization and Metrology

Alain C. Diebold
AGENDA

• Evolution of Micro to Nanoelectronics
• Transistor (FEP) Metrology Challenges
• Nano Dimensions & Ultra Thin SOI
• Interconnect Metrology
• Patterning Metrology
• Trends & Conclusions
Transistor Metrology Evolution

Yesterday
90 nm ½ Pitch

Today
45 nm ½ pitch

CMOS
pMOS FINFET

Strain Enhanced Mobility

New Materials

High $\kappa$/interface & Metal Gate Metrology

Molecular Switches ?
Nanowire Transistor ?

Beyond CMOS

15 year Horizon
Non-classical CMOS

171 source
217 Gate
247 drain

Molecular Switches

Metrology For New Structures

UTB SOI

SEMATECH
Accelerating the next technology revolution.
Metrology R&D Rule #1

- Figure out what the next devices are and something about how they will work
  - Know just enough to be Dangerous!
  - Have Friends that Know The Field
Switching Speed of Long Channel Transistor - The Old Days

\[ I_{\text{dsat}} \propto \left( \frac{1}{L_g} \right) \left( \mu_{\text{Carrier Mobility}} \right) \left( \frac{1}{\text{EOT}} \right) \]

Transistor Gate Delay, \( \tau \), decreases as CD decreases but Gate Dielectric must also decrease in thickness.

As \( L_g \) gate length:

\[ I_{\text{dsat}} \uparrow \quad \text{as} \quad L_g \text{ gate length} \downarrow \]

Sounds Easy
- Just decrease the Gate length &/or increase mobility

TROUBLE As dielectric thickness decreases leakage current increases
General Rules for CMOS Scaling

\[ \frac{X_j}{L} \approx \frac{1}{3} \]

\[ \frac{T_{ox}}{L} \approx \frac{1}{30} \]

Today - All Scaling Rules are Violated

\[ \frac{T_{depletion}}{L} \approx \frac{1}{3} \]

\[ \frac{V_{th}}{V_{dd}} \approx \frac{1}{3} \]
Planar CMOS Evolution

ITRS PIDS Roadmap

Fully Depleted SOI

High k Gate Dielectric

Metal Gate Electrode

Strained Si

Multiple Gate MOS

Drivers: HP


First Year of "Volume Production"

High k = High Performance

Applications

Low Power

Applications

2006 PIDS Changes:

Delay Projected Date of Deployment of Key Innovations by 2 years for high-performance and LOP Logic (not LSTP).

Driven by concerns about feasibility of '08 deployment.

Intel and IBM announce 45 nm ½ pitch high k and metal gate in 2007

Intel and IBM announce 45 nm ½ pitch high k and metal gate in 2007

ITRS PIDS Roadmap

Accelerating the next technology revolution.
### New Transistor Devices (2006 ITRS)

<table>
<thead>
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<tbody>
<tr>
<td>DRAM 1/2 Pitch</td>
<td>80</td>
<td>65</td>
<td>45</td>
<td>32</td>
<td>22</td>
<td>14</td>
</tr>
<tr>
<td>Logic Gate Length</td>
<td>32</td>
<td>25</td>
<td>18</td>
<td>13</td>
<td>9</td>
<td>7</td>
</tr>
</tbody>
</table>

- **Planar Bulk CMOS**
- **UTB FD SOI**
- **Dual Gate or Multiple-Gate**

**2006 ITRS**
The Future – the Ultimate NanoTransistor

Short Channel Behavior

\[ I_{dsat} \propto \left( \frac{1}{L_0} \right) \left( \mu_{Carrie} \right) \left( \frac{1}{EOT} \right) \]

Nano Transistors

\[ I_{dsat} \sim W C_{ox} (V_G - V_T) \nu_{sat} \]

\[ \tau = C_{load} V_{DD} / I_{dsat} \]

C dependence

A = Lg x W
Dopant Conc.

See Lundstrom’s publications
Transition to Beyond CMOS: Make CMOS from NanoMaterials

Nanowire Electronics (Lieber - Nature)

NanoTube Electronics (Avouris – Chen, Science)

18 um long
Carbon nanotube

Ring Oscillator
5 CMOS inverters
= 10 FETs
Nano-Sized Transistor Features require Materials Characterization

SOI

Nanowire Sized Si or Ge channel

Ge nanowire

Nanowire Features require Materials Characterization
Transistor and Interconnect Delays

SPEED / PERFORMANCE ISSUE The Technical Problem

From ITRS and Mark Bohr (Intel)
Figure from IBM
**Interconnect Delay: GLOBAL LINE SCALING**

Global conductor lines getting smaller in cross-section but *NOT* in length. Signal delay is growing exponentially!

\[
\text{RC Delay} \approx \rho \cdot \varepsilon \cdot \frac{L^2}{W^2}
\]

- **LINEs** get smaller
- **But!**
- **CHIPs** don’t

- \( L \) Stays Same
- \( W \) Decreases
Future Interconnect (ITRS 2006)

- 3D Interconnect ?
  - Kreupl, Infineon

- Carbon Nanotubes ?

- Optical Interconnect ?

Intel

MARCO Center
AGENDA

• Evolution of Micro to Nanoelectronics

• Transistor (FEP) Metrology Challenges
  Extending Planar CMOS & Introducing Non-Planar CMOS
  - Stress and Film Thickness (& Sidewall)

• Nano Dimensions & Ultra Thin SOI

• Interconnect Metrology

• Patterning Metrology

• Trends & Conclusions
Today - ICs use Locally Strained Si
Considerable Process Diversity

NMOS – SiN Stress Liner
PMOS SiGe in Source & Drain

PMOS
Compressive Strain
increased hole mobility

NMOS
Tensile Stress SiN Layer
increased electron mobility

Dual Stress Liner
NMOS – Tensile SiN
PMOS – Compressive SiN

Courtesy Intel

AMD Athelon™ 350 Venice
Micro - Chipworks Corner
Dick James
Diversity in Dual Stress Liner Process Drives unique Metrology Solutions

AMD Athelon™ 350 Venice Micro - Chipworks Corner Dick James

Reported AMD Process
N&P MOS Compressive Si Nitride layer
Oxygen Implanted in NMOS area & Nitride becomes tensile OxyNitride

IBM –MP from Xbox 360 Micro - Chipworks Corner Dick James

Reported IBM Process
NMOS Spacer reduced
PMOS Multilayer Compressive Nitride
Survey of Stress (Strain) Measurement Methods

Nano-Raman and CBED

- Micro-Raman, XRD
- Photoreflectance Spectroscopy

Micro-Area Level Stress

- Laser Interferometry
- Oraxion Method

Transistor Level Stress

Die Level Stress

- Laser Interferometry
- Oraxion Method

Wafer Bow

Laser Interferometry, Oraxion Method
Strain measurement
Convergent Beam Electron Diffraction (CBED)
HOLZ Line Fitting

Lattice constants determined by least-squares ($\chi^2$) fitting of experimental to simulated HOLZ line patterns for [340] zone.

ASACSTM software by Soft Imaging Systems Inc (from “STREAM” project).

3-D lattice fitting under constraints of plane strain approximation.


J. M. Zuo, Ultramicroscopy 41, 211 (1992)
TEM sampling will not be easy

Differences in PMOS and NMOS mobility: iso vs Dense
pMOS difference 14%
nMOS difference 8%
nMOS to pMOS difference ratio 22%

Much more complicated for real design

Fichtner – at 2005 Nano Transistor Conference
Trend: Use Modeling to connect what you want to measure with what you need to know. Example: Metrology of Strained Channel Devices

Short Channel NMOS Gain

MD Giles, et al, VLSI Symposium 2004
Film Thickness at Nano-Dimensions

- **Transistor Gate Dielectric**
  - Complicated Dielectric Stack with SiO₂ Interface

- **Metal Gate**
  - Thin Metal Layer with Dual Work Functions for NMOS vs PMOS
Physical Film Thickness Metrology

Spectroscopic Ellipsometry

X-Ray Reflectivity

Incident X-ray

\[ n = 1 \]

\[ n_s < 1 \]

index of refraction for X-rays

Reflected X-ray

\[ \theta_{\text{crit}} = \frac{\lambda}{r_o \rho_e} / \pi \]

\[ \theta_{\text{crit}} \]

\[ D = 2.33 \text{ g/cm}^3 \]

\[ \text{Si} \]

\[ \text{Glancing angle (degrees)} \]

Intensity

Light source (Xe, D\text{2}, lasers)

monochromator

polarizer

analyzer

p

s

Polarization after sample

Expt

fit
Optical/X-ray vs Electrical Measurement

C-V Structures receive Further Processing
Optical thickness vs electrical EOT
Capacitance of a very thin interface can have big effect

\[ t_{\text{optical}} = t_{\text{int}} + t_{\text{high}} \]

\[ EOT = t_{\text{int}} + \left( \frac{3.9}{\kappa} \right) t_{\text{high}} \]

See also: C Richter (NIST) in Char & Met for ULSI 2000
Traditional High Precision SiO2 Thickness

- Single Wavelength Ellipsometry

- Optical constant at one wavelength – only n needed - k close to zero in visible wavelength range

- Oxynitrides – same principle works for thickness - nitrogen concentration not easy to pin down to 0.1 atomic % optically even with SE
Spectroscopic Ellipsometry

Lab – Far IR to VUV

In-line – Near IR to VUV

Dielectric Properties are a function of wavelength of light

Film data (t, n, k, etc.)
Cody-Lorentz optical model used for parametric modeling of gate dielectrics.

\[
\varepsilon_2 \propto \text{Exp} \left[ \frac{(E - E_t)}{\beta} \right], \text{for } E \leq E_g.
\]

\[
\varepsilon_2 \propto (E - E_g)^2, \text{for } E > E_g.
\]

New Optical Models
Variability with Composition and Process
See Jimmy Price’s talk for SE of defects in High K

Optical Constants

Imag(Dielectric Constant), $\varepsilon_2$

- HfO$_2$
- HfSiO (10% silicate)
- HfSiO (20% silicate)
- HfSiO (40% silicate)
- HfSiO (60% silicate)
- HfSiO (80% silicate)

Photon Energy (eV)
Thin Metal film metrology

Dielectric function of a Metal film

Drude response in IR

Damped Lorentz response after plasmon

Plasmon

Challenge: Stable Recipe over wide range of thickness

Overall absorption
Lorentz (interband contribution)
Drude (free carrier contribution)
Wrap Around Gate Metrology

**FINFET (IBM)**

- Fin line edge roughness
- Fin thickness uniformity

**NMOS - MOSFET**

**PMOS – FINFET**

**MUGFET**

- Fin line edge roughness
- Fin thickness uniformity

Side Wall and Top Dielectric Thickness and Composition
Front End Metrology Other Measurements

Shallow Trench Isolation

Pattern & Implant Wells

Pattern & Gate Dielectric

Pattern Poly/metal Implant LDD

Pattern & Implant S/D
AGENDA

• Evolution of Micro to Nanoelectronics
• Transistor (FEP) Metrology Challenges
• Nano Dimensions & Ultra Thin SOI
  • Example of SEMATECH Work (Price & Diebold)
• The Future of Materials Characterization
• Interconnect Metrology
• Patterning Metrology
• Nano - Characterization and Metrology
• Trends & Conclusions
Optical Constants Properties:

- Bulk Si optical properties are well known
- Optical properties of nano-scale materials are not well known.
- Shifts in nano-scale SOI films can be observed at room temperature
Data Proves the Problem is Real:

<table>
<thead>
<tr>
<th>Layer Description</th>
<th>Thickness</th>
</tr>
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<tbody>
<tr>
<td>3 native oxide</td>
<td>15.166 Å</td>
</tr>
<tr>
<td>2 bulk soi</td>
<td>101.78 Å</td>
</tr>
<tr>
<td>1 buried oxide layer (box)</td>
<td>1606.4 Å</td>
</tr>
<tr>
<td>0 silicon substrate</td>
<td>1 mm</td>
</tr>
</tbody>
</table>

Difference between optical model & data.

- 10 nm SOI: 6.7 % Δ TEM
- 8 nm SOI: 15.1 % Δ TEM
- 4 nm SOI: 18.5 % Δ TEM
- 2 nm SOI: 19.8 % Δ TEM
Optical Absorption at Critical Points

\[ k = (\pi/a)(1,1,1) \quad k = (0,0,0) \quad k = (\pi/a)(1,0,0) \]
Summary of techniques:

• Crystallinity $\rightarrow$ no effect.
• P composition $\rightarrow$ possible $E_1$ amplitude decrease for high P concentration.
• Strain $\rightarrow$ Red shift for $E_1$ transition.
• Quantum confinement $\rightarrow$ Blue shift for $E_1$ transition.

Must determine to what extent strain may be impairing the critical point energy shift!
Other sources of shifts in the optical properties?

Shows Importance of cross-method characterization

1. Confirmed Crystallinity → TEM
2. Dopant Profiles → SIMS
   (No Oxidation induced P Buildup at Interface)
3. No Strain Observed → Raman and XRD
4. Quantum Confinement Observation → SE
Clearly, quantum confinement effects are observed with decreasing thickness of the silicon layer.

Provided the thickness values are fixed by independent means (e.g., TEM), data inversion method is able to extract optical constants for quantum confined silicon.
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Interconnect Metrology

Pattern Low $\kappa$
Control Film Stack Thickness,
Line width/depth and shape

Low k / barrier etch stop / low k

Deposit barrier and copper
Control barrier/copper & voiding

Chemical Mechanical Polishing
Control Flatness
Modeled Effective Dielectric Constants

If bulk dielectric = 2.6 (SiLK*) then $k_{\text{eff}} = 2.94$
If bulk dielectric = 2.2 then $k_{\text{eff}} = 2.57$
If bulk dielectric = 1.5 then $k_{\text{eff}} = 1.96$
If bulk dielectric = 1.0 (Air) then $k_{\text{eff}} = 1.5$

* SiLK Semiconductor Dielectric, Trademark of the Dow Chemical Company

Thanks to Navjot Chhabra
Example of Need for Multiple Methods
Low K Stack (STEM-EELS)

Si epoxy

20 nm

Position (nm)

Intensity (a.u.)

carbon K EELS
nitrogen K EELS
oxygen K EELS
silicon L2,3 EELS

Image Intensity
Optical Metrology
SE analysis: Single Layer Model

Generated and Experimental

cauchy Optical Constants

<table>
<thead>
<tr>
<th>Wavelength (nm)</th>
<th>Index of refraction (n)</th>
<th>Extinction Coefficient (k)</th>
</tr>
</thead>
<tbody>
<tr>
<td>200</td>
<td>2.20</td>
<td>0.000</td>
</tr>
<tr>
<td>400</td>
<td>2.15</td>
<td>0.010</td>
</tr>
<tr>
<td>600</td>
<td>2.10</td>
<td>0.020</td>
</tr>
<tr>
<td>800</td>
<td>2.05</td>
<td>0.030</td>
</tr>
<tr>
<td>1000</td>
<td>2.00</td>
<td>0.040</td>
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</table>

\[ n @ 630 \text{ nm} = 1.9609 \]

Unable to detect interfaces

Still Method of Choice for Manufacturing
due to small Spot size
**Thin film Thickness & Density**

Bragg equation:

\[ 2t \sin \theta = n \lambda \]

\[ \lambda = 1.5406 \text{ Å} \]

\[ \theta_{\text{crit}} = \frac{\lambda}{2t} \]

Index of refraction for X-rays:

\[ n_s < 1 \]

Total reflection:

\[ \text{Si} \quad D = 2.33 \text{ g/cm}^3 \]

λ = X-ray wavelength = 1.5406 Å

\[ r_o = \text{classical electron radius} = 2.8 \times 10^{-15} \text{ m} \]

\[ \rho_e = \text{electron density} \]
XRR analysis: multi-layer and interfaces

Total thickness
- XRR Thickness = 99.0 nm and SE Thickness = 99.8 nm
- XRR shows three interfaces

FFT thickness

<table>
<thead>
<tr>
<th>Layer#</th>
<th>Formular</th>
<th>Thickness (Å)</th>
<th>Density (g/cm³)</th>
<th>Roughness (Å)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Layer#1</td>
<td>SiCN;</td>
<td>254.7</td>
<td>2.049</td>
<td>4</td>
</tr>
<tr>
<td>Layer#2</td>
<td>SiCN;</td>
<td>27.4</td>
<td>2.272</td>
<td>2.1</td>
</tr>
<tr>
<td>Layer#3</td>
<td>SiCN;</td>
<td>217.8</td>
<td>2.024</td>
<td>4</td>
</tr>
<tr>
<td>Layer#4</td>
<td>SiCN;</td>
<td>25</td>
<td>2.224</td>
<td>1.7</td>
</tr>
<tr>
<td>Layer#5</td>
<td>SiCN;</td>
<td>176.1</td>
<td>1.99</td>
<td>1.1</td>
</tr>
<tr>
<td>Layer#6</td>
<td>SiCN;</td>
<td>23.7</td>
<td>2.228</td>
<td>0.7</td>
</tr>
<tr>
<td>Layer#7</td>
<td>SiCN;</td>
<td>265.4</td>
<td>2.012</td>
<td>5.4</td>
</tr>
<tr>
<td>Layer#8</td>
<td>Si;</td>
<td>-1.0</td>
<td>2.33</td>
<td>3.7</td>
</tr>
</tbody>
</table>

Total thickness
- XRR Thickness = 99.0 nm and SE Thickness = 99.8 nm
- XRR shows three interfaces
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**Lithography Technology**

**Near Term Dual Patterning & Immersion 193**

### Timeline:

<table>
<thead>
<tr>
<th>Year</th>
<th>1/2 Pitch</th>
<th>193 nm Immersion</th>
<th>193 nm Immersion</th>
<th>193 nm Immersion</th>
<th>EUV</th>
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<td>2010</td>
<td>45 nm</td>
<td>2013</td>
<td>2016</td>
<td>2019</td>
<td></td>
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<td>2006</td>
<td></td>
<td>2009</td>
<td>2012</td>
<td>2015</td>
<td></td>
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<tr>
<td>2009</td>
<td></td>
<td>32 nm</td>
<td>22 nm</td>
<td></td>
<td></td>
</tr>
<tr>
<td>2012</td>
<td></td>
<td></td>
<td>193 nm Immersion</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Process Steps:**

1. Exposure 1
2. Etch 1
3. Exposure 2
4. Etch 2
5. Etch 2

**Techniques:**

- Resist
- BARC

**Imaging Methods:**

- 193 nm Immersion
- EUV

**Schematic Diagram:**

- Reticle stage
- C1 collector
- Gas jet assembly
- Laser-produced plasma
- C2, C3 pupil optics
- Spectral purity filter
- Drive laser beam
- Projection optics
- Wafer stage
Dual patterning for contacts (two exposures with etch steps) overlay control

Exposure 1
Etch 1

Exposure 2
Etch 2

Resist
BARC

Litho 2 = Litho 1
■ Equal lines

Litho 2 > Litho 1
■ Thinner lines
■ Pairs of lines (AB:AB)
■ Across area CD’s identical

Overlay error
■ Different line width alternating

Courtesy Bart Rijpers
Overlay Metrology Requirements

- $OL = \sqrt{(OL1)^2 + (OL2)^2}$
- $OL = 70\%$ single exposure $OL$
Low Energy SEM for CD Measurements

CD-SEM is Extendable to 32 nm Node

Thanks to David Joy
Scatterometry for CD Measurements

Scatterometry is Extendable to 32 nm Node
Potential New CD Methods also apply To Other Areas & Beyond CMOS

CD-SAXS

He Ion Microscope New Imaging Physics

Win – Li Wu  NIST

Alis Corp. (part of Zeiss)
CD Control Range – will it be relaxed?

• Vt behavior already dominates gate length for circuit performance and functionality

• Performance fluctuations due to CD will be dominated by leakage power and not by gate delay/speed
  – Frequency range of 30-35% == leakage spread of 20X
  – Borkar (Intel), 2002

• Ongoing ITRS Design TWG Discussion
Conclusions

- **CMOS Extension and Beyond CMOS both Require Characterization and Metrology at the NanoScale**
- Interfacial Measurement is Increasing in Difficulty & Importance
- Sidewall Control will become more important
- New Problems often require New Methods such as Optical Second Harmonic Generation
- Dimensional Confinement and Surface State Effects must be included in Optical Modeling
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