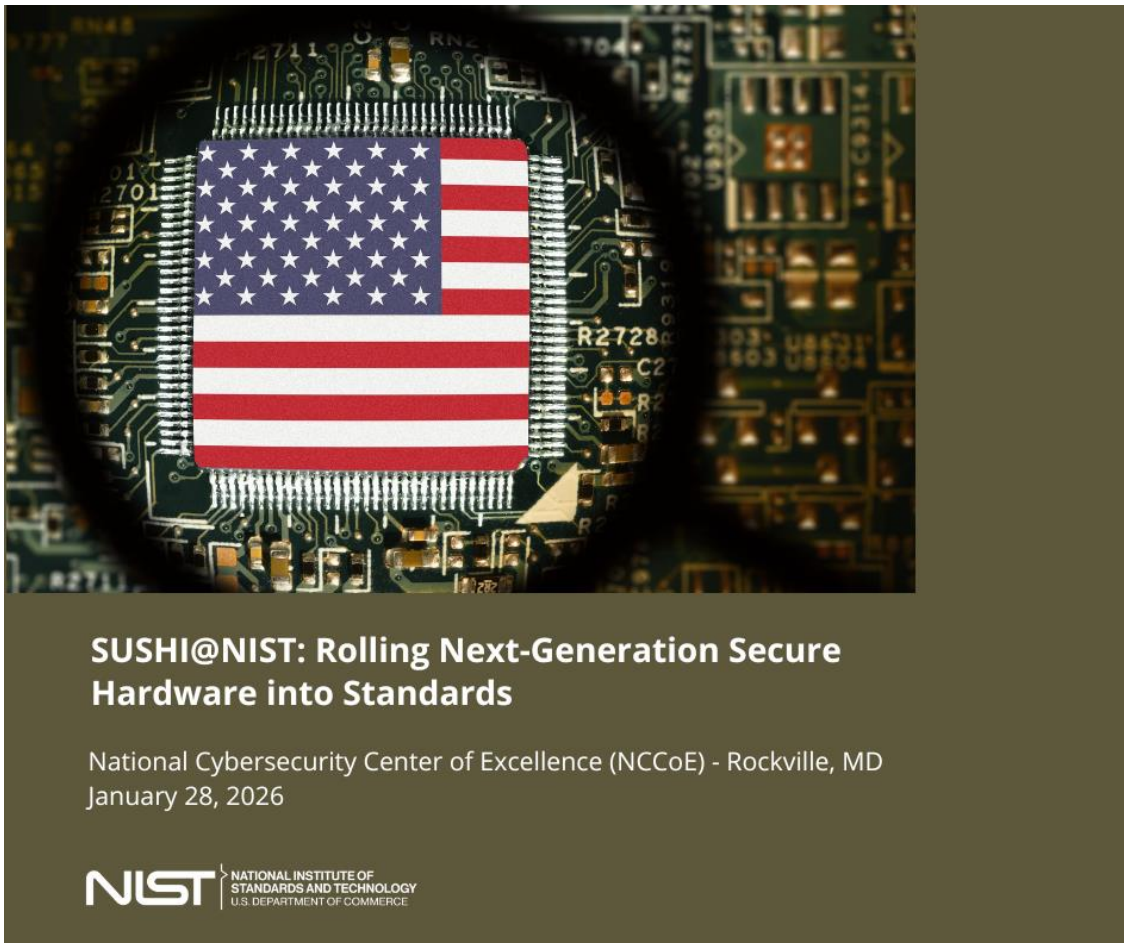

8:30	**NIST Safety Briefing** **Jay Rekhi, NIST**
8:35	**Welcome and Introduction to NIST** Jim St. Pierre, NIST
08:50	**Opening Remarks by Organization Committee** Ahmad-Reza Sadeghi, TU Darmstadt
	Session 1 **Chair:** Ahmad-Reza Sadeghi, TU Darmstadt
09:00	**A Roadmap Towards Scalable Security Assurance** Jason Fung, *Intel*
09:30	**Security in Memory and Storage** Tamara Schmitz, *Micron*

10:00	**Hardware Attacks on AI Inference Chips** Marc Witteman, *Keysight*
10:30	**BREAK**
	Session 2 **Chair:** Jeyavijayan Rajendran, Texas A&M
10:45	**NIST Semiconductor Standards Activities** Mary Bedner, *NIST*
11:15	**NSF/CISE Security, Privacy, and Trust in Cyberspace (SaTC 2.0)** Selcuk Uluagac, *NSF*
11:45	**Standards-Based Assurance for Trusted Electronics** Jim Will, *USPAE*
12:00	**LUNCH**
	Session 3: **Chair:** Jay Rekhi, NIST
13:00	**AI Provenance and Traceability** Jeremy Muldavin, *Cadence*
13:30	**The Fundamentals of Semiconductor & Hardware Security for an AI World** Reed Hinkel, *Synopsys*
14:00	**Siemens Tessent** Lee Harrison, *Siemens*
14:30	**BREAK**

14:45	**Government Panel** Moderator: Christine Rink, MITRE Panelists: Qiaoyan Yu (NSF), Jim Will (USPAE), Robert Aitken (CHIPS), Eric Eilertson (Microsoft), Robert Watson (University of Cambridge)
15:45	**Breakout Sessions** • **Challenges in adopting hardware security in semiconductors**, Moderators: Cvitan, Sandra (CHIPS) • **Secure Lifecycle Management**, Moderator: Matthew Areno (Rickert-Areno Engineering, LLC) • **Emerging Threats**, Moderator: Jason Fung (Intel)
16:45	**Closing Remarks**
17:00	**End of Workshop**