Morning Agenda (AM ET)

Time	Session	Speaker
7:30AM – 8:30AM	Check-in	
8:30AM – 8:40AM	Welcome Remarks	**Laurie Locascio** Director of NIST and the Under Secretary of Commerce for Standards and Technology
8:40AM – 8:45AM	Proposer's Day Expectations	**Dev Palmer** Director, CHIPS NAPMP
8:45AM – 9:00AM	NAPMP Program Overview	**Subu Iyer** Senior Technical Advisor, CHIPS NAPMP
9:00AM – 9:30AM	Advanced Packaging Research & Development (R&D) NOFO Overview	**Dev Palmer** Director, CHIPS NAPMP
9:30AM – 10:00AM	CHIPS R&D Office Policy Overview	**Richard-Duane Chambers** Director, Policy and Integration CHIPS R&D Office
10:00AM – 10:30AM	Networking/Break	
10:30AM – 10:45AM	Research Security	**Greg Strouse** NIST Safeguarding Science Research Security Director
10:45AM – 11:00PM	Application Preparation and Submission	**Shanell Williams** Other Transaction Agreements Officer
11:00AM – 12:00PM	Question and Answer Panel	**Panel:** Dev Palmer, Richard-Duane Chambers, Greg Strouse, Shanell Williams

Afternoon Agenda (PM ET)

Time	Session	Speaker
12:00PM – 1:30PM	Networking and Lunch (on own)	
1:30PM– 1:40PM	Afternoon Instructions	
	Research and Development Areas (RDAs)	
1:40PM – 1:50PM	Equipment, Tools, Processes, and Process Integration	**Bob Soave** Program Manager
1:50PM – 2:10PM	Facilitated Feedback	
2:10PM – 2:20PM	Power Delivery and Thermal Management	**David LaVan** Program Manager
2:20PM – 2:40PM	Facilitated Feedback	
2:40PM – 2:50PM	Connectors (Photonics & RF)	**Chris Myatt** Program Manager
2:50PM – 3:10PM	Facilitated Feedback	
3:10PM – 3:40PM	Networking/Break	
3:40PM – 3:50PM	Chiplets Ecosystem	**Bapi Vinnakota** Program Manager
3:50PM – 4:10PM	Facilitated Feedback	
4:10PM – 4:20PM	Co-design/Electronic Design Automation (EDA)	**Rob Aitken** Program Manager
4:20PM – 4:40PM	Facilitated Feedback	
4:40PM – 4:50PM	NAPMP Next Steps	**Dev Palmer** Director, CHIPS NAPMP
4:50PM – 5:10PM	Facilitated Feedback	
5:10PM – 5:15PM	Closing	