IAC R&D Gaps Working Group

June 6, 2023 Update to IAC

Industrial Advisory Committee (IAC) – R&D Gaps Working Group

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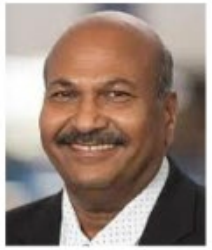

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Global-Foundries

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Intel Corporation

Charles Gray
Ford Motor Company

Todd Younkin
SRC

WG member only

Supporting: Ben Davis, David LaVan

New WG charge: Advanced Packaging

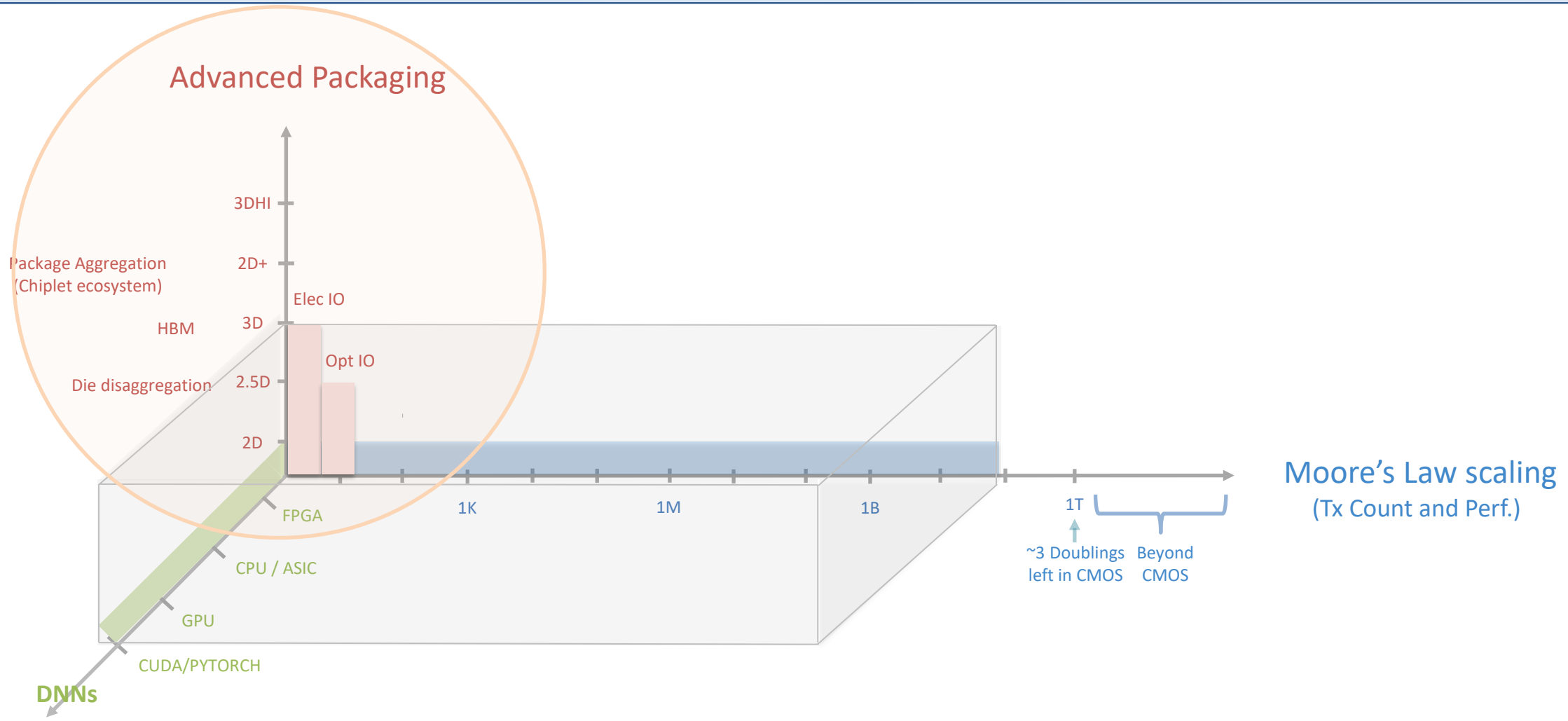
Provide recommendations for strategies and investments for the long-term research needs for advanced packaging that will help establish and sustain a viable domestic advanced packaging ecosystem in the US.

The working group could:

- review the advanced packaging needs of the U.S. and ecosystem gaps suggest focus area priorities
- outline best opportunities to develop and sustain US leadership in semiconductor advanced packaging
- suggest mechanisms for ecosystem development

Co-leads: Ann Kelleher, Carol Handwerker

Moore’s Law economics will be driven by chips, advanced packaging and architectures



Application driven systems with specialized architectures/algorithms
w/ software stack

R&D Gaps Working Group recommendations – Feb 7 IAC Meeting

Recommendation 1:

Establish a set of five key capabilities aimed to lower the barriers to entry and success for innovators. These capabilities will rely on a network of physical and virtual facilities with a digital backbone to reduce design and experimentation cycle time. These capabilities should benefit the *entire community of stakeholders and it should be of primary importance to increase access to and reduce the effective cost of accessing these capabilities over time.*

1) Establish easily accessible prototyping capabilities in multiple facilities and enact the ability to rapidly try out CMOS+X at a scale that is relevant to industry

2) Create a semiverse digital twin

3) Establish chiplets ecosystem and 3D heterogeneous integration platform for chiplet innovation and advanced packaging

4) Build an accessible platform for chip design and enable new EDA tools that treat 3D (monolithic or stacked) as an intrinsic assumption

5) Create a nurturing ecosystem for promising startups

Relevant to Advanced Packaging

Schedule for Advanced Packaging sprint

Mar 14,21,28	Key documents, Homework: Top 5 focus areas, Grouping of team inputs (Part 1)
Apr 4,11,18	Grouping of team inputs (Part 2), Speaker selection
May 2	Settle on essential questions Any modifications or new issues from DOC white paper?
May 9	SRC presentation, 1/2-day session prep
May 15	*½-day session (Monday AM) to make recommendations* - Speaker summary: lessons learned from 3 subgroups - Sub-groups to propose recommendations, alternative, and rationale
May 23	Refine recommendations
May 30	Refine recommendations, review draft of Jun 6 presentation
Jun 6	IAC public meeting in Wash DC

Summary of R&D Gaps WG progress

Focus of 90-day sprint:

- Reviewed 16 relevant R&D, roadmap, and ecosystem landscape reports
- Rolled up “Top 5 focus areas” from each working group member
- Identified key R&D gaps categories to be addressed
- Recorded perspectives from 22 experts relevant to these categories
- Prepared 10 recommendations for Jun 6 IAC meeting

Sources for Advanced Packaging materials

SRC	Jan ‘21	Decadal Plan for Semiconductors (Grand challenges)
	Apr ‘23	MAPT: Advanced Packaging and Heterogeneous Integration (Chapter 9, interim)
MITRE	Nov ’21	American Innovation, American Growth: A Vision for the NSTC
	Mar ’22	NSTC RFI Response
	Feb ‘23	Creating an Enduring National Resource: A Blueprint for NSTC and NAPMP
ASIC	Feb ’22	Accelerating Semiconductor Research, Accelerating America
	Mar ’22	NSTC RFI Response
	Mar ’23	Recommendations for revitalizing semiconductors through NAPMP
NIST	Sep ’22	Incentives, Infrastructure, and R&D Needs for Semiconductor Industry
	Apr ’23	A Vision and Strategy for the NSTC
PCAST	Sep ’22	Revitalizing the U.S. Semiconductor Ecosystem
M&M	May ‘22	3DIC and 2.5D IC Packaging Market (2022 edition)
YOLE	May ‘22	Status of the Advanced IC Substrate Industry (2022 edition)
IPC	Nov ’21	North American Advanced Packaging Ecosystem Gap Assessment
	Dec ’22	Towards a Robust Advanced Packaging Ecosystem
HIR	Mar ‘23	Heterogeneous Integration Roadmap (2021-2023 editions, 24 chapters

High level topics of interest

Groupings of “Top 5” homework

Analog/Mixed signal
Economics
Ecosystem
EDA
Equipment and Materials
Defense
Manufacturing
Memory
MEMS/Sensors/Actuators
Photonics
Standards
Startups
Substrates

Invited Speakers for IAC R&D Gaps working group

Guest Speaker	Title	Affiliation
John Allgair Jim Vandevere	CTO President	BRIDG – Florida BRIDG – Florida
Hamid Azimi	CVP – Substrate Pkg. Tech.	Intel
Bob Brennan	GM – Customer Solutions Eng	Intel Foundry Services
Richard Gottscho	EVP, Strategic Advisor to CEO	Lam Research
Steve Kosier	COO & CTO	Skywater
Kangwook Lee	SVP/GM Packaging Dev. Div.	SK Hynix
Seokhee Lee	Technology Advisor	SOLIDIGM/SK Hynix
Vidya Natarajan Sundar Ramamurthy Sarah Wozny	Dir. Mkt. Products Group VP & GM Epi, Pkg. &ICAPS BU Director – Adv. Pkg. BU	Applied Materials
Tom Rucker	VP – Technology Dev.	Intel
Willy Shih	Faculty, Business School	Harvard

Guest Speaker	Title	Affiliation
Muhannad Bakir	Faculty, ECE	Georgia Tech
Subu Iyer	Faculty, ECE & MSE	UCLA
David Harame	COO and Associate VP	AIM Photonics
Alissa M. Fitzgerald	Founder and CEO	A.M. Fitzgerald
Steven Pawlowski	CVP Advanced Memory	Micron
Kevin Engel	EVP Business Units	Amkor
Brett Robinson Ted Tessier	CEO CTO, Advanced Packaging	Integra
Madhavan Swaminathan	Faculty, EE	Penn State Univ.
Kenneth Larsen	Dir. 3DHI Product/Market	Synopsys
Frederick Miller	VP Electronics	PsiQuantum
Ian Melville	Director Technology Dev	Globalfoundries
Matt Kelly	CTO and VP Tech Solutions	IPC

Speaker sub-groups

SG #1	SG #2	SG #3	
Applications	Manufacturing	EDA / General	
Analog/Mixed signal	Equip and Materials	Ecosystem	
Defense	Manufacturing	EDA	
Memory	Startups	Standards	
MEMS/Sensors/Act.	Substrates	+	
Photonics	+	Economics	
+	Economics	+	
Economics	+	Best of SG #1 & 2	
+	Best of SG #1 & 3		
Best of SG #2 & 3			
James	Ken	Todd	Team Leads
Ahmad	Ann	Dan	
Chuck	Carol	Mukesh	
Gregg	Dan	Philip	
Raj	Debo	Susie	
	Om		

Essential Advanced Packaging questions

What are the essential features of the NAPMP organization, leadership, operating model and funding – that is not specified in the DOC white paper?

What is the appropriate integration and prototyping strategy (over time) that leads to US manufacturing?

What is missing in the roadmap development efforts and how can they be improved?

How can accelerated development of digital twin and EDA capabilities for advanced packaging lead to innovation?

What is winning and how would you measure success in 1, 3, 5, and 10 years?

What goals are appropriate for energy efficiency and sustainability with respect to economics, environmental impact, and climate change?

How do you foster global collaboration in R&D while achieving the overall CHIPS Act domestic goals?

What is Advanced Packaging?

Technologies and capabilities that allow the **combination of multiple chips and other components to form a highly integrated, multi-functional sub-system which can then be assembled onto laminates, panels, or circuit boards** to pass signals and power to the external environment – by packaging semiconductor **chips** in very close proximity to each other **side-by-side (2.5D) with a silicon bridge or interposer** as well **as stacked on top of each other without an intermediary layer such as die-to-die, die-to-wafer, or wafer-to-wafer (3D)** allowing very high-speed and high-integrity signal transmission.

Increasingly resemble wafer fab processes in terms of feature sizes (sub-micron) and the methods needed to produce them

In contrast, typical packaging is focused on single die or few die mounted to a laminate substrate with larger feature size wire bond connections to interface with the external environment.

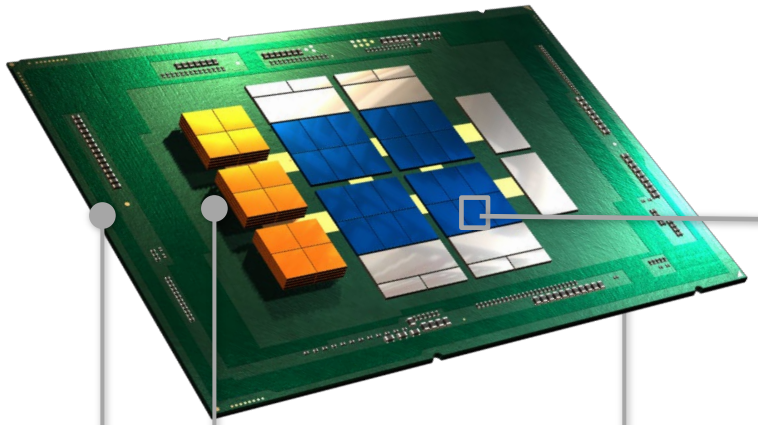
Where does packaging begin? Packaging starts at the silicon metallization layer used to connect the die to another die or a substrate.

Where does packaging end? System integration and Testing: Advanced Packaging involves considerations beyond the chip level and encompasses system in a package (SIP) level integration and testing. This includes techniques like system-on-chip (SoC) packaging, where multiple functions and components are integrated onto a single chip, and system level testing to insure the overall functionality, reliability and performance of the packaged device or system. For devices with processors/programmable logic, system level test and evaluation of the tightly integrated multi-functional sub-system includes functionality and product performance of the co-designed hardware *and software*.

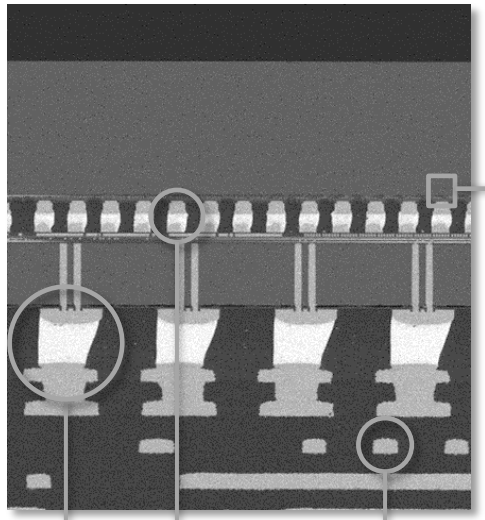
What are the enabling processes and capabilities? TSVs, bumping, bonding and hybrid bonding, silicon and glass interposers, silicon bridges, RDL on substrate structures, chiplets, laser and fiber attach, metrology, failure analysis, product and reliability test

Dimensional scaling from packaging to semiconductors (>6 orders of magnitude)

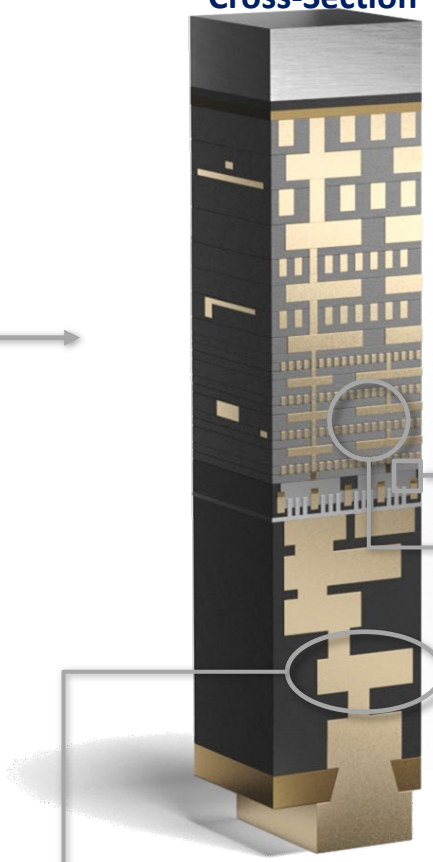
System in a Package



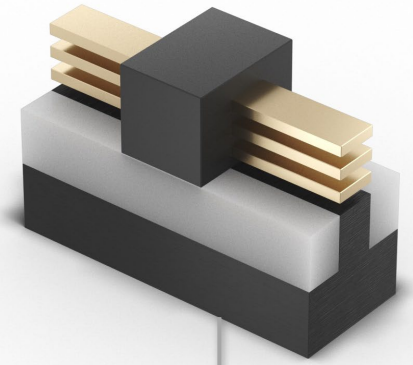
Package Cross-Section



Active Die Cross-Section



RibbonFET



10 mm | 1 mm | 100 µm | 10 µm | 1 µm | 100 nm | 10 nm | 1 nm

Package Edge

Die Edge

Package-to-Board Interconnect Pitch

Die-to-package Interconnect Pitch

Die-to-die Interconnect Pitch

Package Routing

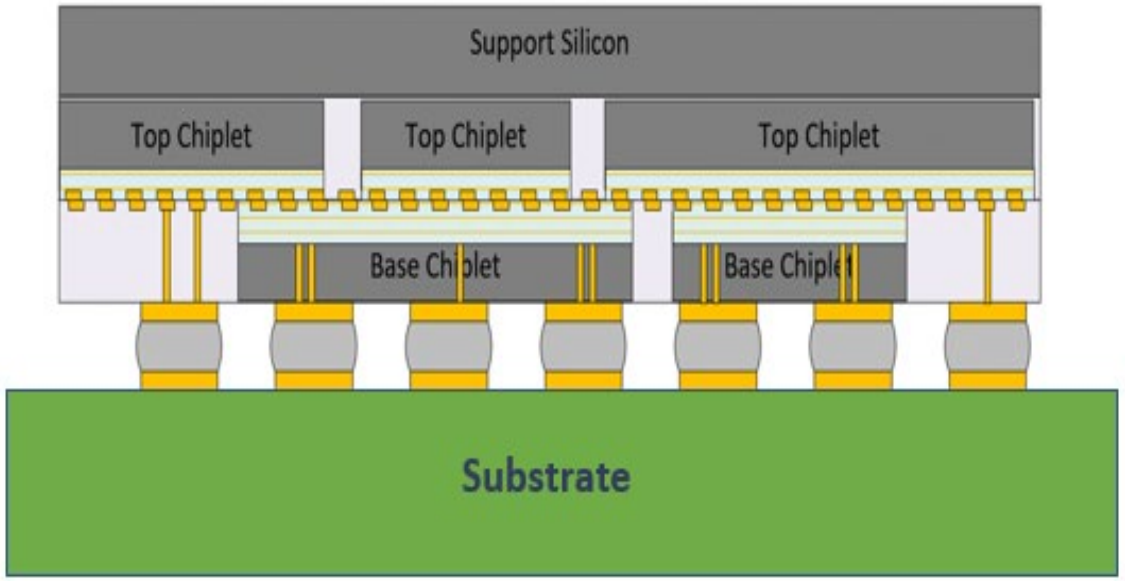
Die Power Routing

Local Interconnect Routing

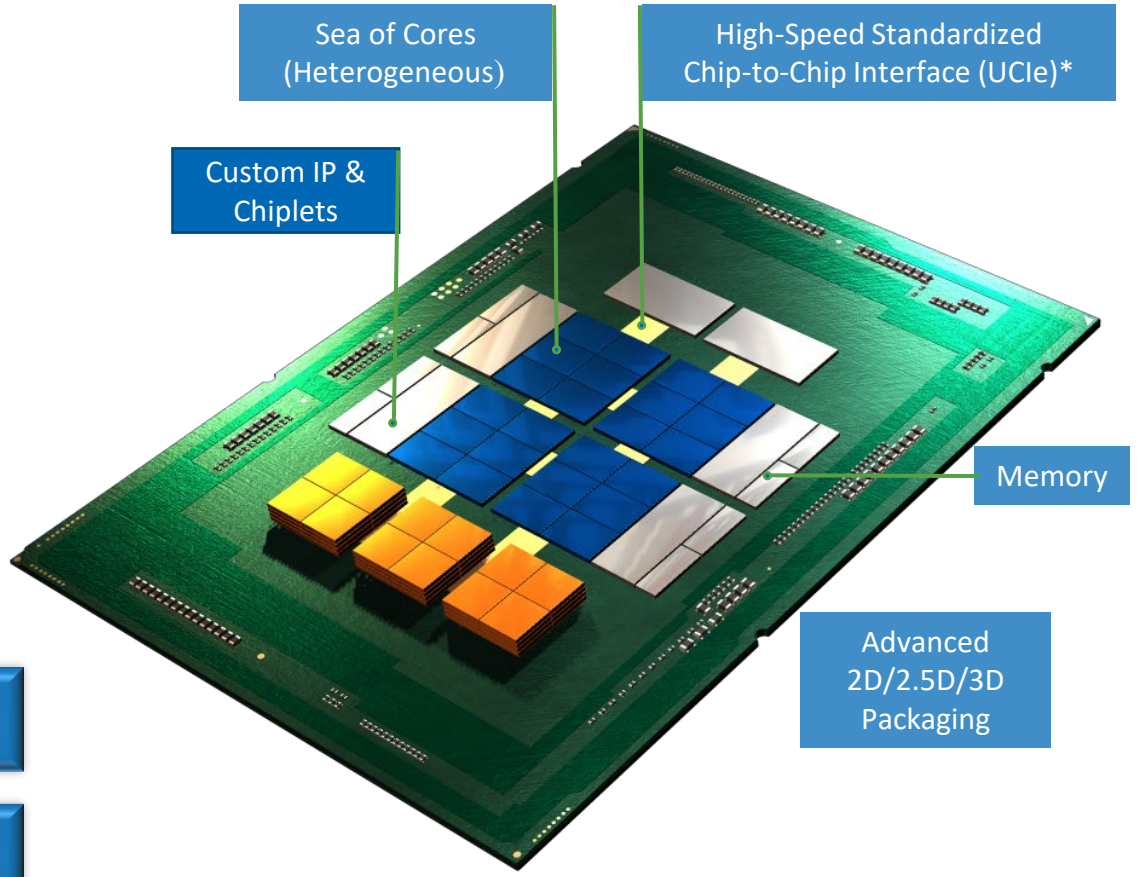
Transistor

Schematic of Advanced Packaging (cross sections)

Cross-Section of Advanced Package



System in a Package



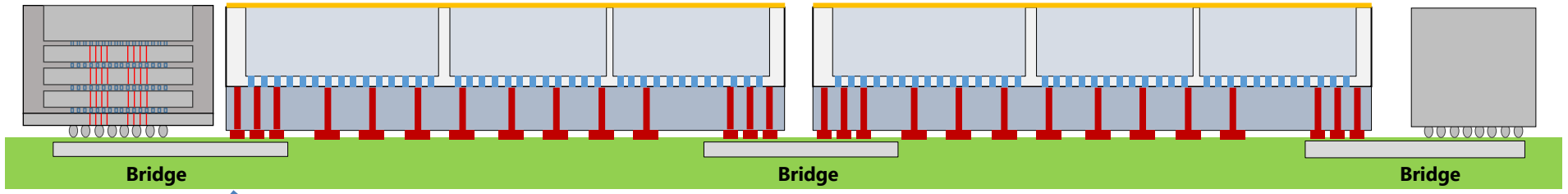
- Enables construction of SIP exceeding max reticle size
- Mix-and-match chiplets from different process nodes
- Faster Time to Market and reduced portfolio cost

The package is a complex composite: Compute

Material
- UF/mold: Flow, Reliability, Warpage
- Fluxes: joint quality/cleanability
- Thermal interface materials

Electrical
- Bump Current carrying capability
- HSIO and Power Delivery
- Design co-optimization

Fine pitch interconnect
- Die-Die, Die-Wafer, Die- Substrate
- Improved alignment/ bump Coplanarity
- Stacked die coplanarity



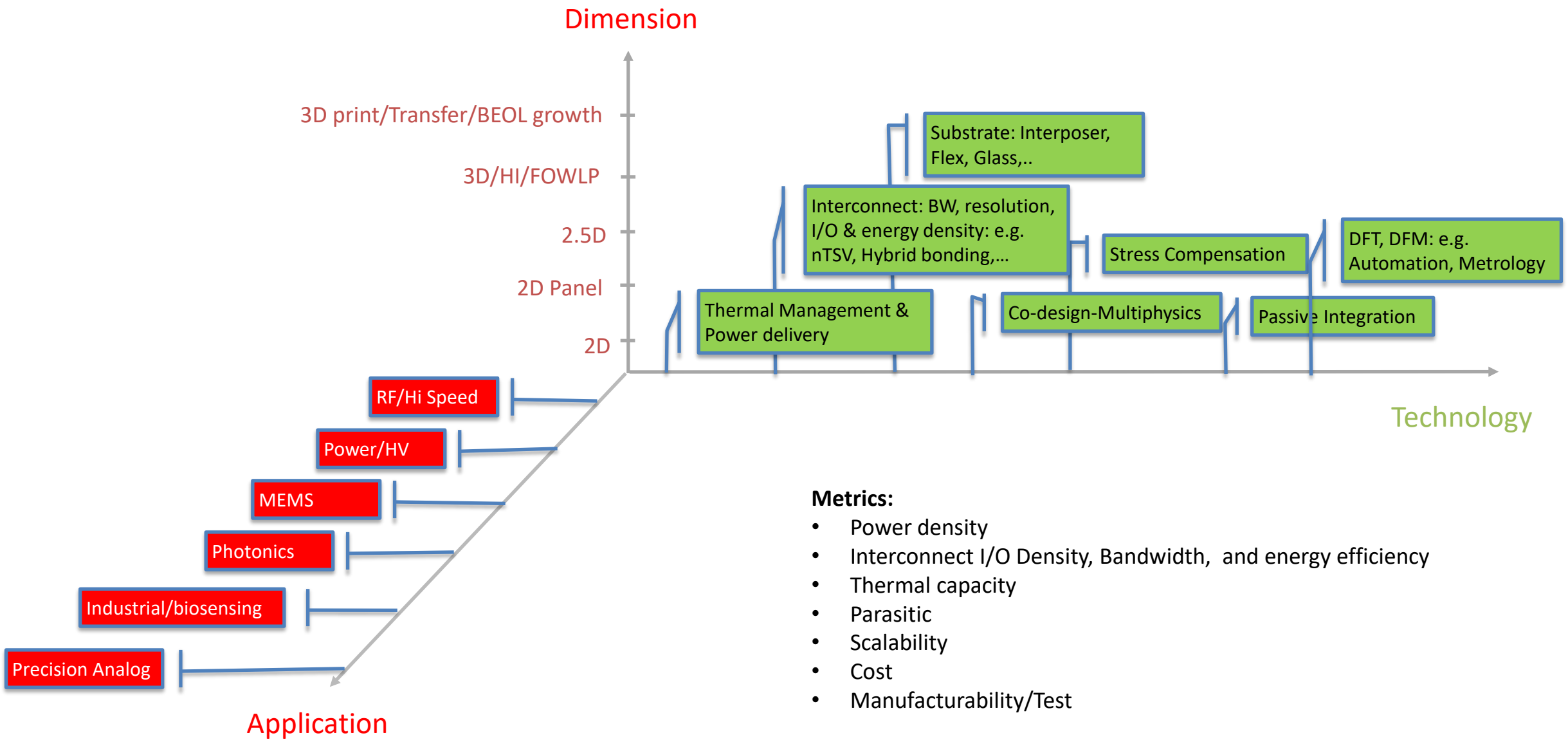
External IP/die/pkg integration
- Passivation/bump compatibility
- Design rule/ Design co-optimization

Advanced substrates
- Improved bump coplanarity
- Fine pitch/ Multi diameter bumping
- High density routing

Acceptable Reliability
- Temperature cycling
- Thermo-mechanical cycling
- Electromigration
- Temperature/humidity/Bias

Equipment/ Material/Process/ Design Co-optimization/Test are key to Heterogenous Integration

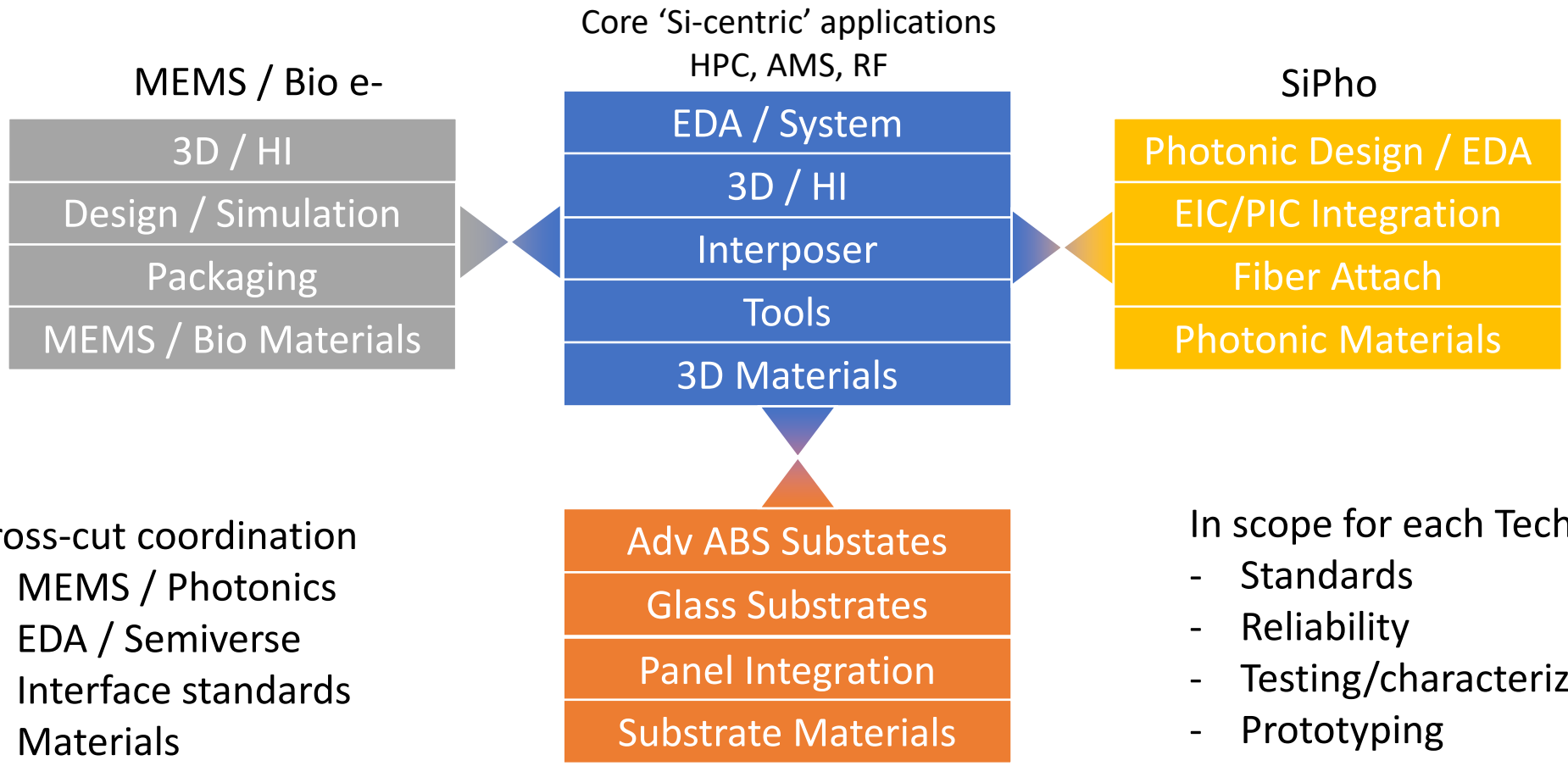
The package in a complex landscape: Analog/Mixed signal



Metrics:

- Power density
- Interconnect I/O Density, Bandwidth, and energy efficiency
- Thermal capacity
- Parasitic
- Scalability
- Cost
- Manufacturability/Test

NAPMP Tech Centers Concept Recommendation



Cross-cut coordination

- MEMS / Photonics
- EDA / Semiverse
- Interface standards
- Materials
- Reliability / testing
- WFD

In scope for each Tech Center

- Standards
- Reliability
- Testing/characterization
- Prototyping
- Economics
- Sustainability

High level observations from documents and speakers

- Packaging is a vast space with significant differences based upon cost, performance and application requirements
- Packaging decisions have historically been based upon **cost** (especially labor driven) and **proximity to SE Asia ecosystem**
- US has nearly **no presence in substrates, minimal OSAT capabilities**
- US has **strengths in EDA, equipment, and product/system design**
- A packaging process baseline requires a useful full flow manufacturing process, which requires incentives for industry leader(s) to locate in the US – therefore it is critical to link to the DOC CHIPS Act manufacturing incentives program (9902)
- Without a packaging process baseline, it will be hard to prototype and evaluate process, equipment, and metrology improvements and there needs to a significant commitment to test, yield, and characterization for all NAPMP efforts
- Urged to consider demand-side incentives to motivate capacity installs and to create virtuous cycles of learning
- The boundary between wafer and packaging facility is blurring and there are opportunities (logistics, cycle time, cost, automation) that would benefit from adjacency
- Increased automation for advanced packaging will be required to on-shore manufacturing, while workforce development is especially acute for the US with a changing mix of technicians and engineers as the level of automation changes

Recommendations

Recommendation 1

Ensure an **independent budget and a dedicated executive leader** for NAPMP, reporting to NSTC CEO and NSTC fiduciary board

Considerations:

- Advanced packaging R&D needs dedicated focus and financial independence to ensure that the intentions of the CHIPS Act are not overwhelmed by the large investments required for semiconductor front-end activities
- At the same time, the distinction between wafer fab integration flows and unit processes continues to blur as the feature size and performance requirements converge
- Most of the capabilities and grand challenges require an integration of chip and packaging (co-design): they are not independent

Recommendations (pg 2)

Recommendations 2 and 3

Incentivize (9902) an existing **wafer- and panel-based manufacturer** to **create prototyping capabilities** in the US by establishing a pilot and initial manufacturing line, including expansion capabilities (annex) for R&D

Incentivize (9902) at least one existing **substrate manufacturer** to create a US pilot and initial manufacturing line and with a R&D annex to **explore advance substrate options** (including glass)

Considerations:

- Wafer and panel packaging are state-of-the-art fundamental capabilities are currently not available in the US, and are inherently less dependent on labor intensive manufacturing of traditional packaging
- Unit based packaging manufacturing is more fragmented, and should be a lesser priority than wafer and panel
- Without a competitive cycle time and yield process baseline, assessing potential improvements from the R&D programs will be greatly impeded, and barriers to achieving future US manufacturing outcomes will remain – likely resulting in CHIPS Act investments mostly benefiting existing non-US stakeholders
- Co-location reduces the risk in transitioning from prototyping to manufacturing
- A competitive process baseline is crucial for achieving digital twins, prototyping and workforce development

Recommendations (pg 3)

Recommendation 4

Ensure a robust set of programs that **establish and extend enabling processes and capabilities** such as bump and line pitches sub-5 um line/space, processing for TSVs (silicon and substrate), hybrid bonding (Wf-Wf, Die-Wf, Die-Die), etc. across multiple technologies and materials (i.e., not just silicon)

Considerations:

- Advances in enabling materials, processes, equipment, metrology, failure analysis and test are critical to US leadership and for following an aggressive roadmap

Recommendations (pg 4)

Recommendations 5 and 6

Identify **EDA** advanced packaging and system gaps and create pathfinding and ultimately EDA tools that can effectively co-design and system optimize all elements of **2.5 and 3D heterogeneous integration** (especially photonics, memory, RF, power, etc.) **including multi-physics capabilities**

Create a community of stakeholders to **build a digital twin capability from the R&D stage through manufacturing** with a **tight integration to EDA/simulation** as well as for **workforce development support and training**

Considerations:

- Substantial gaps exist in the ability to simulate and co-design system level solutions implemented as advanced packaging, and especially to do pathfinding exploration for optimization. This will require long term investment before the market may be ready to support the level of investment required
- The software and modelling capability needs to be enhanced to enable a faster learn rate during research and development.
- These capabilities can be the vehicles for both increased automation and more effective workforce training especially where access to physical infrastructure and the costs/time for prototyping may prove prohibitive
- Build out of these capabilities supports collateral, essential tool development, including enabling PDKs, ADKs, design services, and shuttles
- Leverage inter-agency coordination opportunity to provide demand-side system/application co-design drivers

Recommendations (pg 5)

Recommendation 7

Set grand challenges of **achieving 10x increase in productivity and 10x decrease in environmental/energy footprint** for mainstream advanced packaging capabilities, including eco-benign semiconductor manufacturing

Considerations:

- Numerous speakers called out the need to improve automation and reduce the environmental footprint of today's and tomorrow's packaging technologies
- As with highly automated semiconductor fabs, this will significantly reduce the obstacles for US-based locations for future packaging centers
- These goals are aggressive but obtainable if roadmapped and funded over a 10-year time horizon similar to what was accomplished with the 300mm wafer size conversion. International cooperation across the R&D and manufacturing supply chains is essential.
- Initial work in this area can coordinate with the DARPA ERI NGMM 3D HI program that has already started.

Recommendations (pg 6)

Recommendation 8

Double the **U.S. advanced packaging university footprint** (from ~5 to ~10) and faculty, expand existing advanced packaging university programs by at least 50%, and build a virtual university-wide curriculum with increased funding for research and education

Considerations:

- Analogous to the early days of computing, initial investments to build world class university-based faculty to teach the next generation of students and conduct pathfinding research are crucial
- There are only a handful of universities that have anything approaching a critical mass of advanced packaging faculty and programs today
- We need to expand those programs, hire the next generation of faculty educators and researchers, and initiate new programs in partnership with willing universities. This will take time to recruit and build.

Recommendations (pg 7)

Recommendation 9

If the IAC were to call out one emerging technology to receive special attention, we believe **silicon photonics** is a rare general-purpose technology that should merit CHIPS Act investments in R&D, prototyping, and manufacturing

Considerations:

- Silicon photonics, integrated with electronics, represents a fundamental leadership play if manufacturing and scaling issues can be resolved such as laser/fiber attach, electronics/photonics testing, packaging, chiplets
- Basic photonics technology can scale out across many application domains, starting first in HPC/data centers and in life sciences, and expanding to industrial, automotive, RF, computing, and quantum
- Photonics is on the cusp of achieving significant manufacturing volumes; it mostly unoccupied territory and the advent of CXL and UCIe chip interconnect standards paves the way for nearer-in photonics co-packaged solutions
- The US has significant R&D capabilities, lots of startups, and investments in a photonics ecosystem and prototyping via the AIMS Photonics Mfg. USA Institute (NY), as well as commercial facilities such as Global Foundries (NY) and Intel (AZ)
- Silicon photonics is one of the technologies that can address sustainability and environmental issues (energy and power reduction) across several critical applications

Recommendations (pg 8)

Recommendation 10

Complete a **landscape survey and gap analysis of the advanced packaging** of both supply and demand in the US (and North America) leveraging recent reports including prototyping gaps in key specialty packaging capabilities - including MEMS, photonics, power electronics, analog, and RF.

Considerations:

- The CHIPS Act NSTC and NAPMP need a clearer more detailed survey of existing capabilities and the gaps compared to state of the art global capabilities
- This needs to be completed as soon as possible to inform priorities and investment decisions, and necessarily overlaps incentives provided in the CHIPS Act 9902
- As part of the gap analysis, include international corporations (equipment and material suppliers, substrate providers, etc.) and relevant **international consortia** such as imec, LETI, Fraunhofer, IME, ITRI, METI (Japan) to ensure duplication of effort is minimized and the best is obtained from the rest of world.

Measures of Success

After 1 year:

- Standup NAPMP with meaningful and collaborative demonstrators that attack industry wide grand challenges
- Select sites for advanced packaging of wafer-based, panel based, and substrate prototyping and production
- Solid plan established for digital twins, simulation, EDA and demonstration vehicles to support prototyping centers
- R&D funding contests to advance unit processes and awards beginning to be disbursed

After 3 years:

- New packaging centers operational with 2.5D and 3DHI capabilities,
- Through commercial incentives in 9902, create a demand for substrates, package assembly and test to ensure new US production lines are populated — explicitly connecting the manufacturing and R&D provisions of the CHIPS Act
- A vibrant startup community and workforce pipeline is supported for NAPMP
- Workforce development programs producing first trained engineers and technicians

After 5 years, and beyond:

- Packaging R&D centers are fully operational
- Through R&D, address labor and productivity considerations by improving automation to drive innovation and mostly level the cost of domestic vs. international facilities
- Domestic capabilities that came online in early years are now moving R&D results into the commercial domain

Recommendation Summary

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5) Identify **EDA** advanced packaging and system gaps and create pathfinding and ultimately EDA tools that can effectively co-design and system optimize all elements of **2.5 and 3D heterogeneous integration** (especially photonics, memory, RF, power, etc.) **including multi-physics capabilities**

6) Create a community of stakeholders to **build a digital twin capability from the R&D stage through manufacturing** with a **tight integration to EDA/simulation** as well as for **workforce development support and training**

7) Set grand challenges of **achieving 10x increase in productivity and 10x decrease in environmental/energy footprint** for mainstream advanced packaging capabilities, including eco-benign semiconductor manufacturing

8) Double the **U.S. advanced packaging university footprint** (from ~5 to ~10) and faculty, expand existing advanced packaging university programs by at least 50%, and build a virtual university-wide curriculum with increased funding for research and education

9) If the IAC were to call out one emerging technology to receive special attention, we believe **silicon photonics** is a rare general-purpose technology that should merit CHIPS Act investments in R&D, prototyping, and manufacturing

10) Complete a **landscape survey and gap analysis of the advanced packaging** of both supply and demand in the US (and North America) leveraging recent reports including prototyping gaps in key specialty packaging capabilities - including MEMS, photonics, power electronics, analog, and RF.