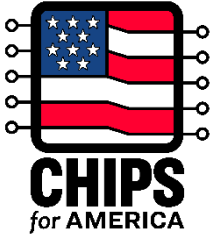


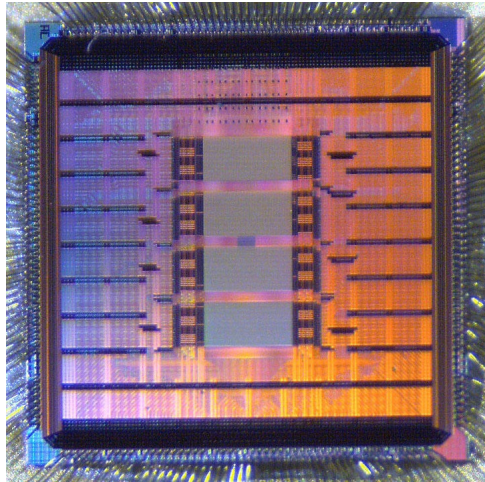
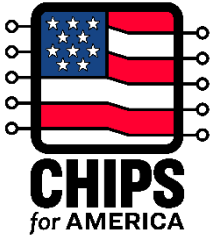
# CHIPS for America Research and Development Update



June 6, 2023



# CHIPS R&D Vision



## U.S. Technology Leadership

The U.S. invents, develops, and deploys the foundational semiconductor technology of the future.



## Accelerate Ideas to Market

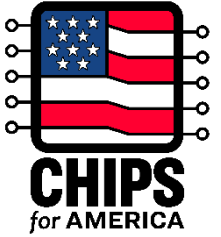
A thriving ecosystem that is focused on getting the best ideas to commercial scale as quickly and cost effectively as possible.



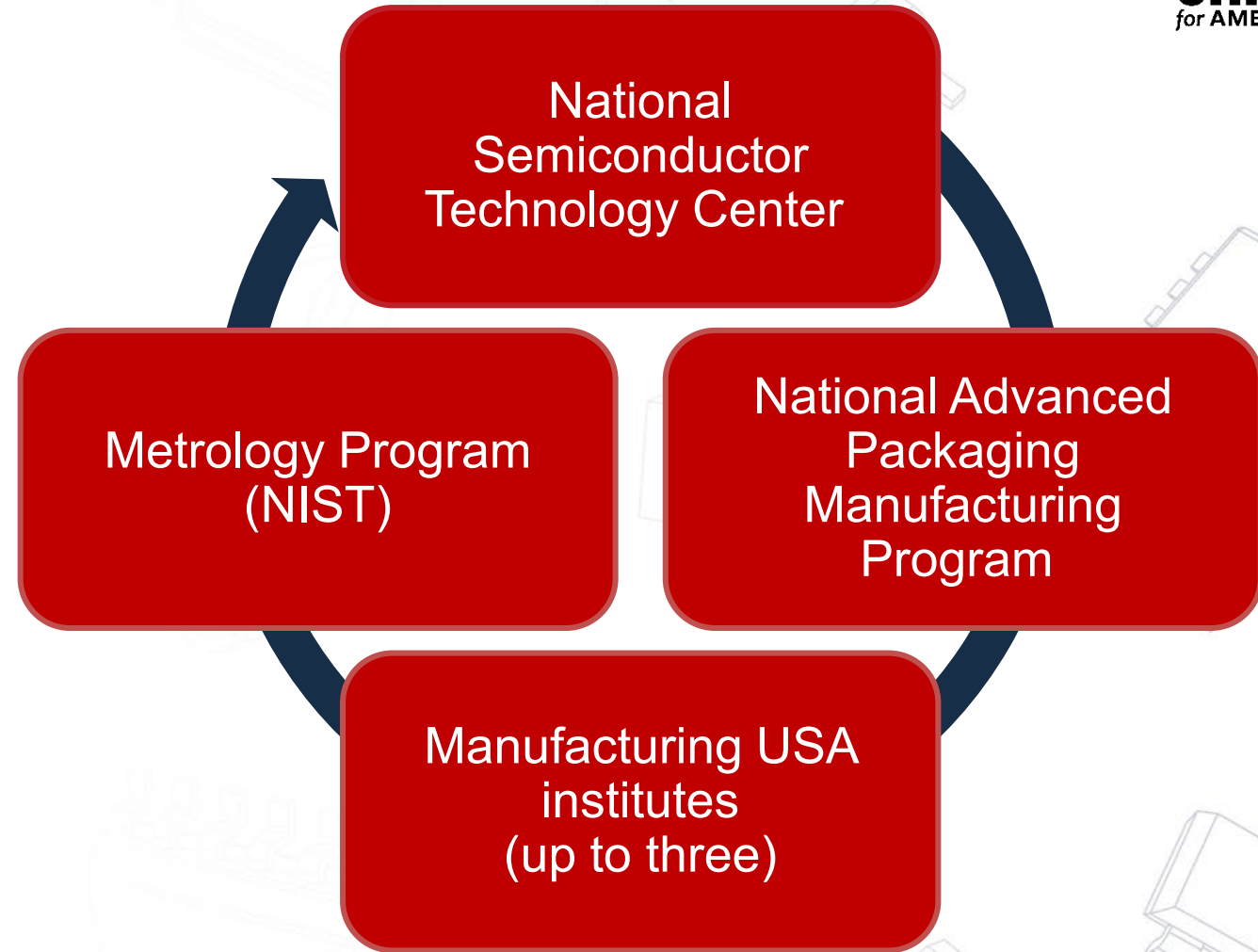
## Talent

A new generation of skilled workers, inventors, designers, researchers, technicians, and others able to build and sustain semiconductor manufacturing in the U.S.

# CHIPS for America R&D

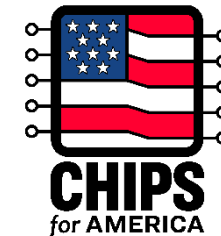


- To strengthen and advance **U.S. leadership** in R&D
- An **integrated ecosystem** that drives innovation
- In **partnership** with industry, academia, government, and allies
- A strategic view of R&D infrastructure, **participant value-proposition**, and technology focus areas
- Informed by the **Industrial Advisory Committee**





# Program Development Timeline



SUMMER 2023

FALL 2023

WINTER 2023

National Semiconductor Technology Center

Selection Committee identifies Board of Trustees

Establish NSTC

National Advanced Packaging Manufacturing Program

NAPMP vision and strategy paper

Manufacturing USA institute(s)

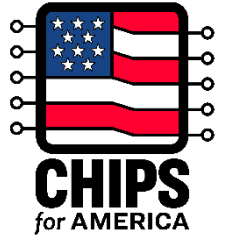
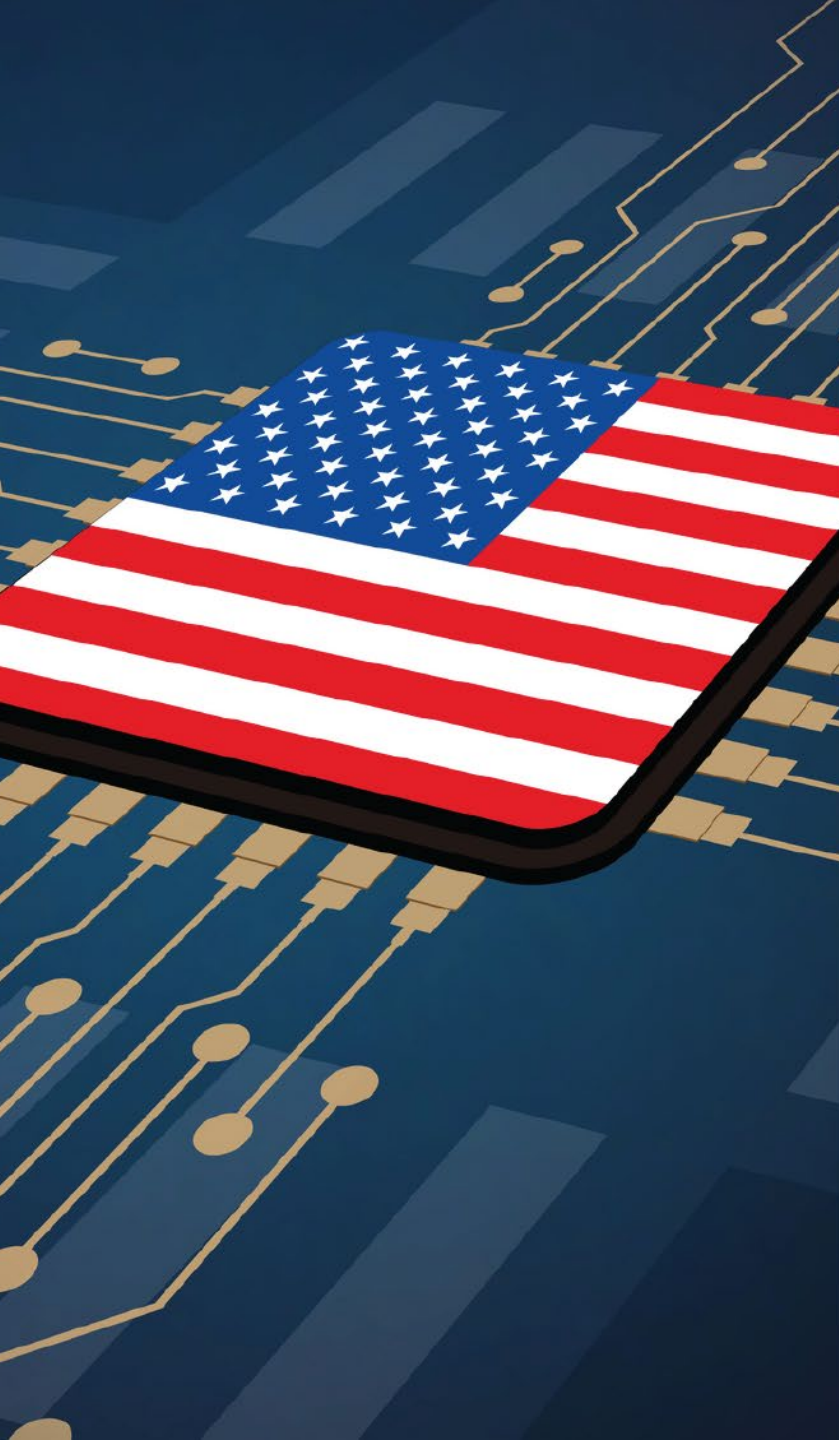
RFI Summary Published

Select topic(s); begin proposal process

Metrology Program (NIST)

Metrology Gaps Report Published

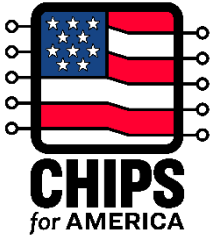
Select programs to begin



# NSTC Vision

By the decade's end, the NSTC should be viewed throughout the world as an **essential resource** within the broad semiconductor ecosystem with a network of respected scientists and engineers, state-of-the-art facilities, effective programs, and demonstrated technical achievements.

# Programs



Technology leadership

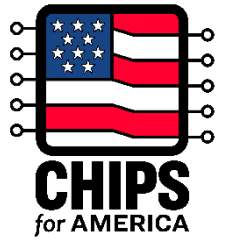


Community assets



Workforce

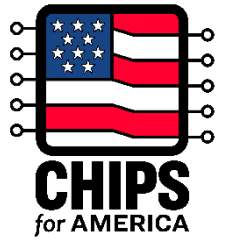




# Technology Leadership

- In-house and funded research
- Grand challenges and road maps
- Standards and protocols
- Technical exchanges
- Security

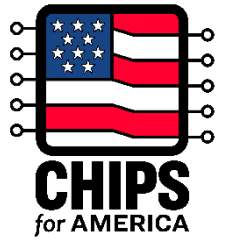




# Community Assets

- Chiplets
- Design Enablement Gateway
- Data sets
- Patents
- Technical centers for prototyping, research, and experimentation



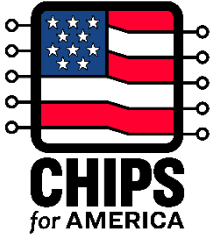


# Workforce Programs

FOR SCIENTISTS, ENGINEERS, AND  
TECHNICIANS

- Outreach to groups traditionally underrepresented
- Support scale-up of existing quality programs
- Develop novel approaches to training

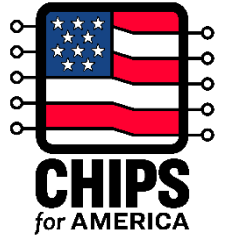
# Membership



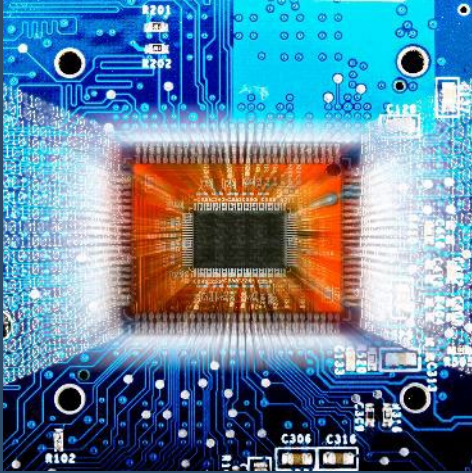
- Businesses of all sizes and at all stages
  - Fabless companies
  - Foundries
  - Integrated device manufacturers
  - Equipment vendors
  - Materials suppliers
- Research institutions, including minority serving institutions
  - Community colleges
  - State and local governments
  - National labs
  - Labor unions
  - Sector investors







# National Advanced Packaging Manufacturing Program



- Strengthen semiconductor advanced test, assembly, and packaging capability in the domestic ecosystem
- Leverage public-private partnerships, that can include support for facilities managed by the NSTC and MUSA
- Broad range of technologies:
  - Heterogeneous integration
  - Wafer and panel-based approaches
  - Tooling and automation
  - Substrate technology

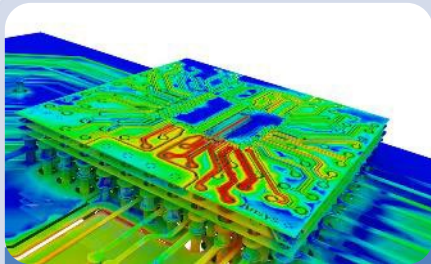
# NAPMP Approach

Technology innovation

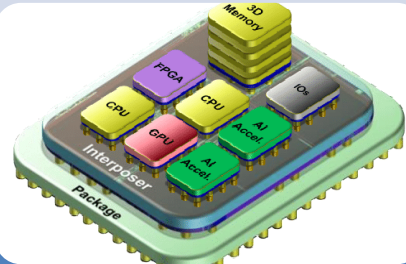
Create an R&D environment advancing the state-of-the art in advanced packaging.

Ecosystem support

Investments to bolster the growth in domestic capacity and enhance capabilities for competitive edge.



Co-design and simulation



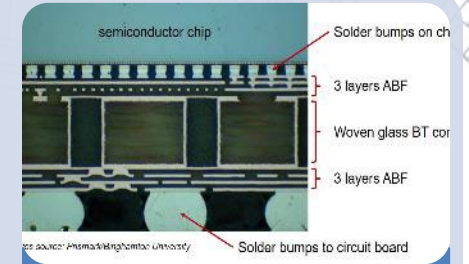
Chiplets



Pilot packaging facilities



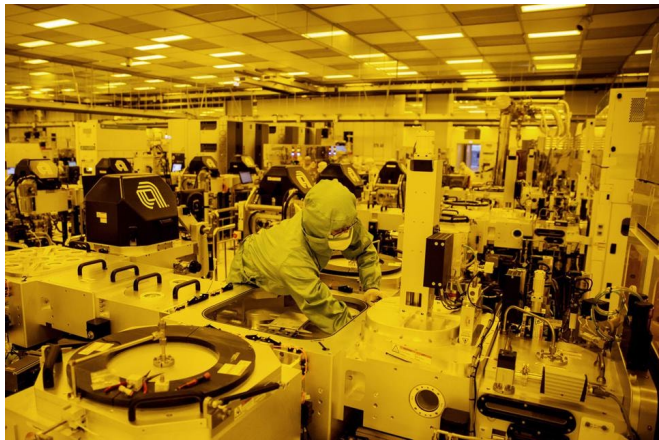
Tooling and automation



Materials and substrates

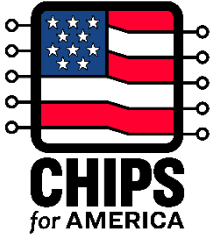


# Pilot Packaging Facility(ies)



- The NAPMP will utilize the NSTC to support (a) packaging facility(ies) that enables R&D efforts.
- Prototype and pilot scale integration of components fabricated in NSTC facilities or 3<sup>rd</sup> party sources.
- Baseline packaging flows to support a goal of established package-proven IP.
- The facility should have sufficient tool redundancy to allow groundbreaking research on new materials and processes while still maintaining baseline capacity.
- Partnerships with domestic OSATs and electronics manufacturing services (EMS) to facilitate migration of successful prototypes to a production manufacturing environment.

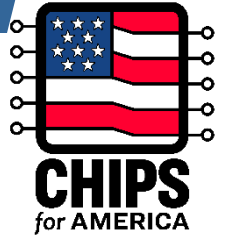
# Manufacturing USA Institute(s)



- Up to three new public-private partnership institutes in the Manufacturing USA network
- To advance research and commercialization of semiconductor manufacturing technologies
- Pre-competitive collaboration among researchers and manufacturers
- Workforce training
- RFI Summary Report Published



# Manufacturing USA Network



- Electronics
- Materials
- Energy/Environment
- Digital /Automation
- Bio-Manufacturing

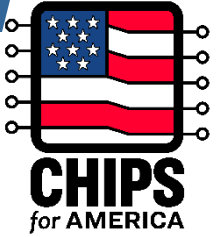
 Integrated Photonics Albany, NY Rochester, NY	 Advanced Functional Fabrics of America Advanced Fibers and Textiles Cambridge, MA	 Transforming Process Industries Modular Chemical Process Intensification New York, NY	 Additive Manufacturing Youngstown, OH El Paso, TX	 Regenerative Manufacturing Manchester, NH
 Flexible Hybrid Electronics San Jose, CA	 Advanced Composites Knoxville, TN Detroit, MI	 Sustainable Manufacturing Rochester, NY	 Robotics & AI Pittsburgh, PA	 Biopharmaceutical Manufacturing Newark, DE
 Wide Bandgap Semiconductors Raleigh, NC	 Where Manufacturing Technology and Talent Matter Lightweight Materials Detroit, MI	 Smart Manufacturing Los Angeles, CA	 The Digital Manufacturing & Cybersecurity Institute Digital Manufacturing & Cybersecurity Chicago, IL	 Bioindustrial Manufacturing St. Paul, MN
NEW— Electrified Processes for Industry without Carbon (EPIXC) Phoenix, AZ			 the cybersecurity manufacturing innovation institute Cybersecurity in Manufacturing San Antonio, TX	



**16 institutes**  
 Members in every state  
 9 partner federal agencies

**DOC sponsors 1 institute + serves as the overall Program Office**  
 DOD sponsors 9 institutes; DOE sponsors 6 institutes

# Semiconductor Institute RFI Key Points



## 1 Institute Scope and Scale

- Several potential topic areas suggested
- No consensus on a single 'super-sized' all-topic institute vs. multiple focused institutes

## 2 Structure and Governance

- Consensus that the design framework for Manufacturing USA is sound, with exception of larger scale needed for impact in semiconductor space
- Consensus for tiered membership structures

## 3 Coordination

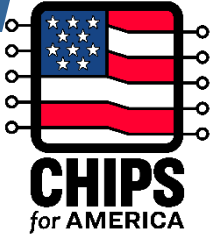
- Consensus that coordination with other CHIPS initiatives and with existing Manufacturing USA institutes in related sectors is critical

## 4 Sustainability

- Consensus that institutes are likely to need federal funding beyond 5 years
- Consensus that in longer-term, institutes achieve sustainability if focused on industry priorities



# Semiconductor Institute Topic Examples

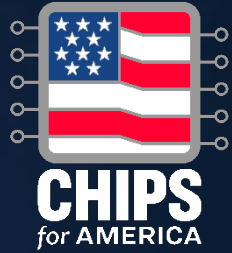


## Cross-cutting technology topics

- Productivity enhancement via early design including co-design, digital twins, and artificial intelligence
- Smart manufacturing and automation
- New and advanced materials
- Metrology and testing

## Focused institute topics

- Substrate manufacturing for advanced packaging
- Sensors and microelectromechanical systems
- Infrastructure to support technology transition to manufacturing

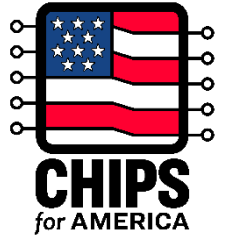


# CHIPS R&D Metrology Program

Marla Dowell, Ph.D.  
Director, CHIPS R&D Metrology Program

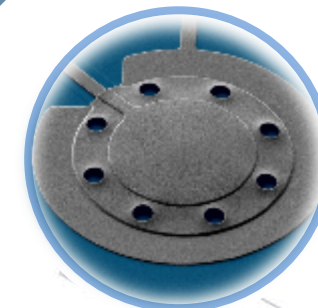
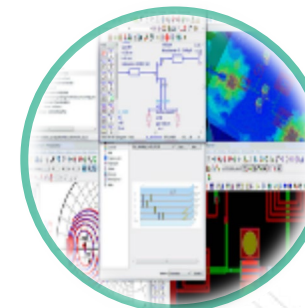
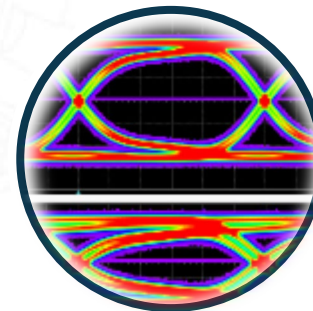
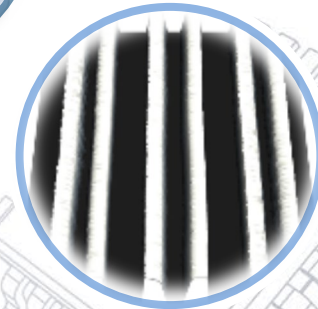
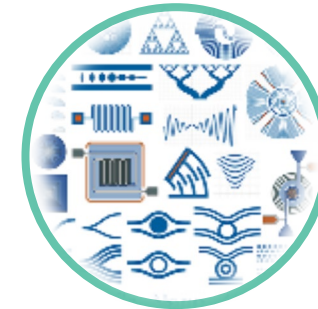
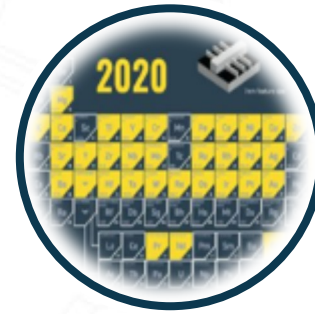


# NIST and Advanced Microelectronics

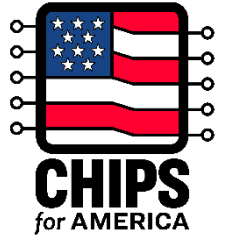


**NIST has a long history and broad portfolio of targeted investments in microelectronics spanning the following areas:**

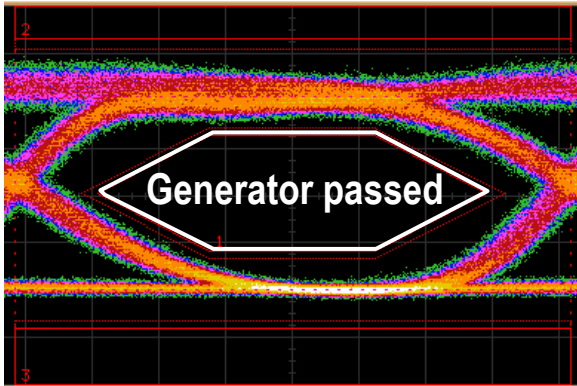
- Materials and chemistry
- Devices and interconnects
- Circuit design and computer automated design tools
- Fabrication/Manufacturing
- Packaging and test
- Computing architectures
- Software, modeling, simulation
- Beyond digital CMOS technologies
- RF electronics



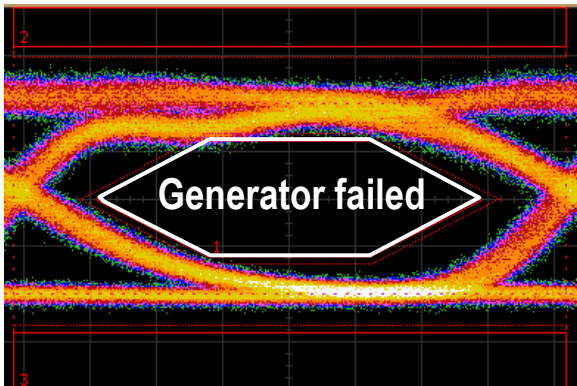
# Metrology Importance



## Reduce Cost



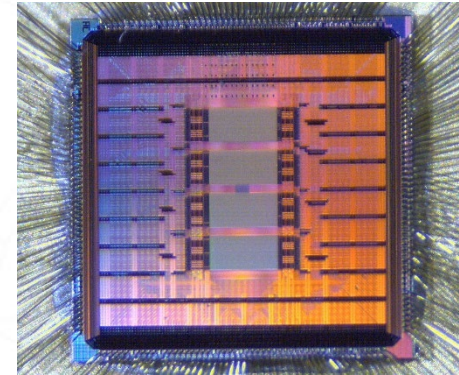
Same transceiver  
measured on two  
different  
oscilloscopes



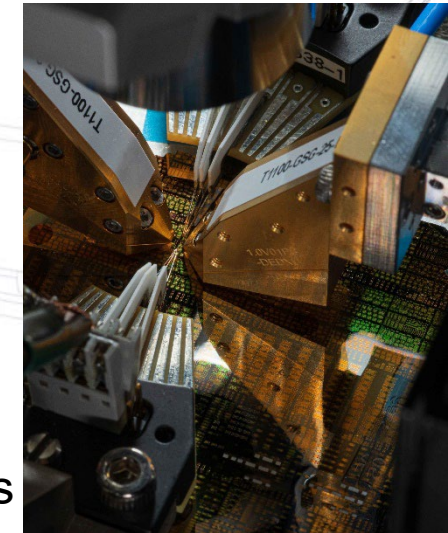
10 Gb/s Ethernet  
Transceivers  
False rejects cost:  
\$200M/yr

Measurements to test 6G technologies do not exist

## Catalyze Innovation



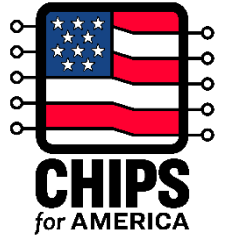
NIST/Google  
Open Source  
Chip designs



NIST/DARPA  
On-chip  
Calibration Kits

Measurement designs so that industry and academia can  
evaluate their technology





# Metrology Program



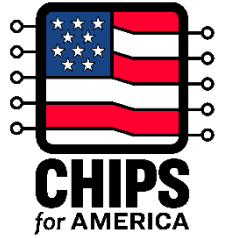
NIST Nanofabrication Facility

**VISION:** CHIPS R&D Metrology catalyzes innovation with emphasis on measurements that are accurate, precise, and fit-for-purpose for the production of microelectronic materials, devices, circuits, and systems.

**MISSION:** Measure, innovate, lead to enhance a vibrant U.S. ecosystem for semiconductor manufacturing and to promote U.S. innovation and industrial competitiveness.

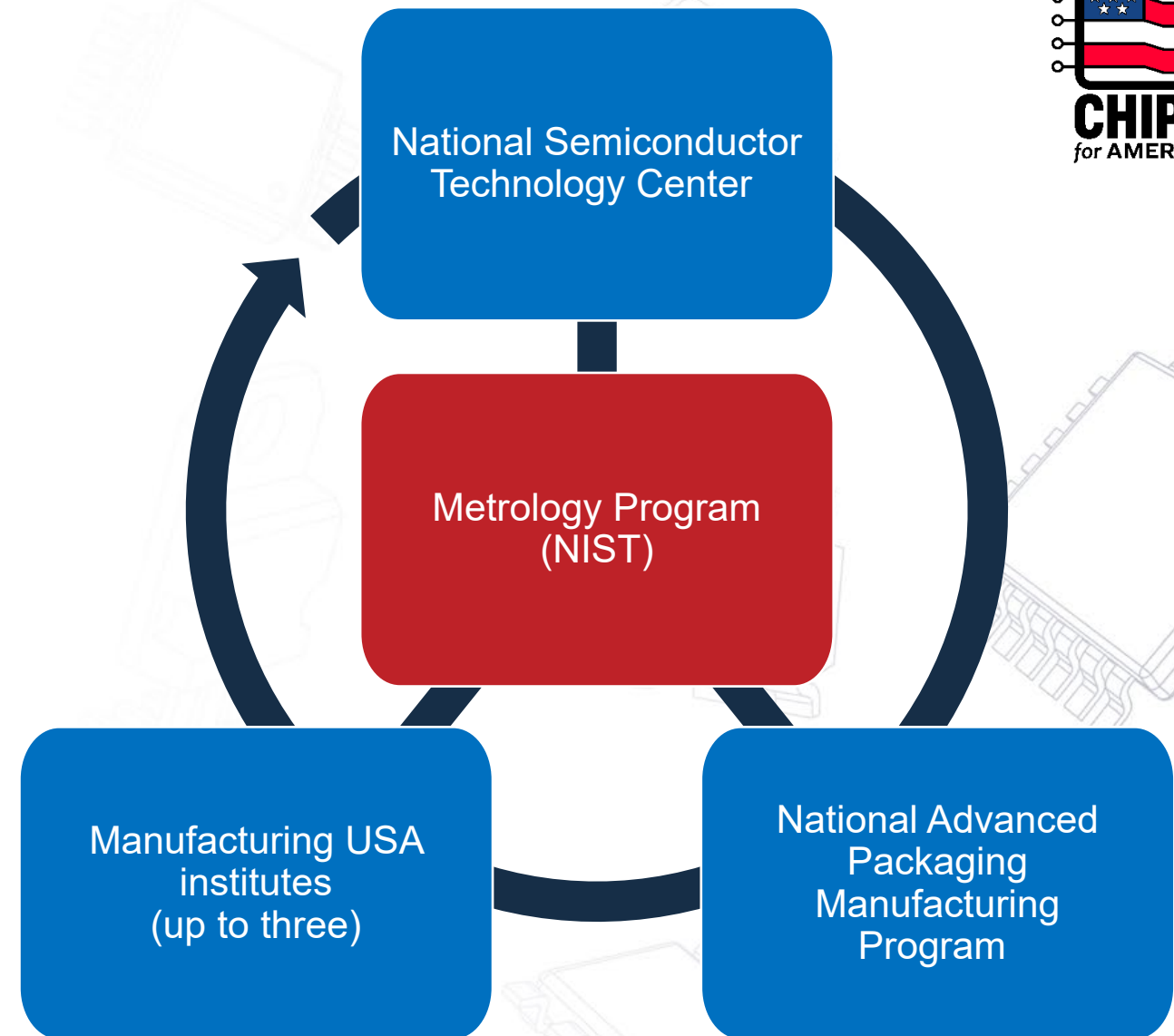
## GOALS:

1. Expanding measurement solutions for the semiconductor ecosystem.
2. Increase the number of solvers by harnessing the diversity of people and ideas, inside and outside of NIST.
3. Expand education and workforce development opportunities that inspire excitement about manufacturing careers and expand career pathways.



# Maximize Speed and Impact

- Metrology is **foundational** and **fundamental** for all R&D programming
- Metrology **tools are delivered** to other CHIPS R&D programs;
- High impact research areas **sourced from industry**
- Metrology technologies should reach **commercial scale**







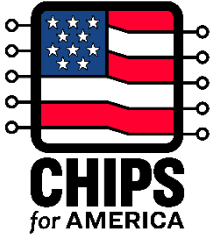
# Industry Input is Key

- Measurement science for new materials and packaging
- Physical metrology for next-generation microelectronics
- Computation and data
- Virtualization and automation
- Reference materials and data, and calibrations
- Standards for processes, cybersecurity, and test methods



[https://nvlpubs.nist.gov/nistpubs/  
CHIPS/NIST.CHIPS.1000.pdf](https://nvlpubs.nist.gov/nistpubs/CHIPS/NIST.CHIPS.1000.pdf)

# Strategic Opportunities



← Extensive feedback from stakeholders across industry, academia, and government →

Metrology for materials purity, properties, and provenance

Advanced metrology for future microelectronics manufacturing

Enabling metrology for integrating components in advanced packaging

Modeling/ simulating semiconductor materials, designs, and components

Modeling/ simulating semiconductor manufacturing processes

Standardizing new materials, processes and equipment for microelectronics

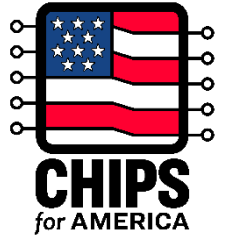
Metrology to enhance security and provenance of micro-electronic based components and products



<https://nvlpubs.nist.gov/nistpubs/CHIPS/NIST.CHIPS.1000.pdf>



# Example: SRMs for 5G materials



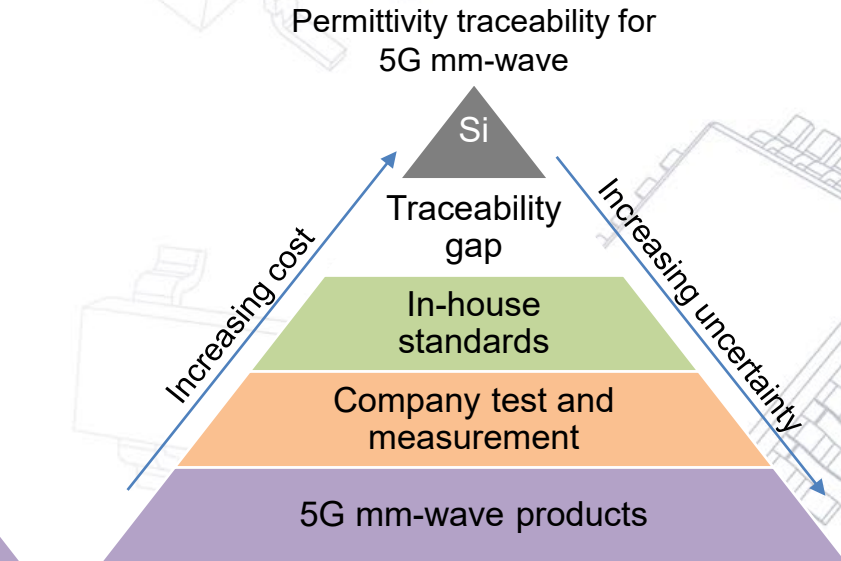
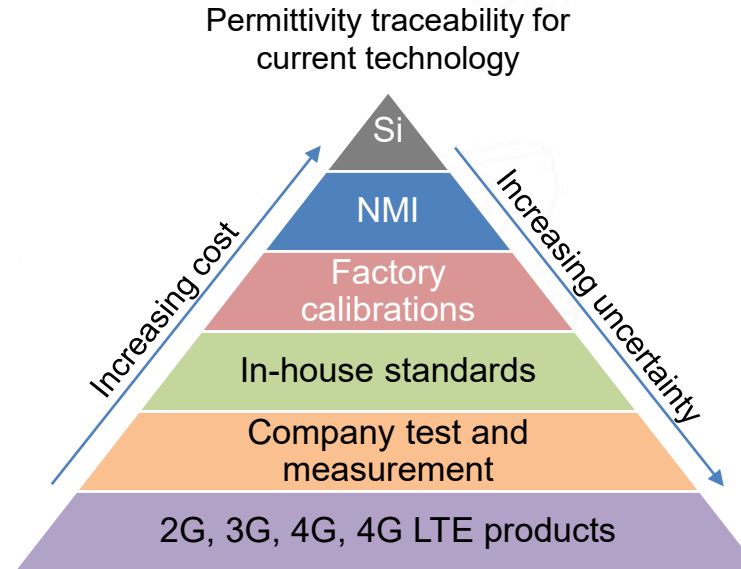
## International Manufacturing Initiative (iNEMI)

“The lack of traceable reference material for mmWaves is a very serious problem. This lack makes verification of measurement methods and laboratory techniques impossible in an industry setting.” - *5G Materials Characterization Project Report I*

## Semiconductor Research Corporation

“Dielectric characterization up to 500 GHz and beyond. Scope includes anisotropic and inhomogeneous materials ... High-frequency and high-temperature dielectric characterization of low-loss materials (encapsulants, mold compounds, substrates, etc.).” - *Research Needs: Packaging*

‘5G’ extends beyond wireless applications, including wired applications with needs for material characterization to 100+ GHz



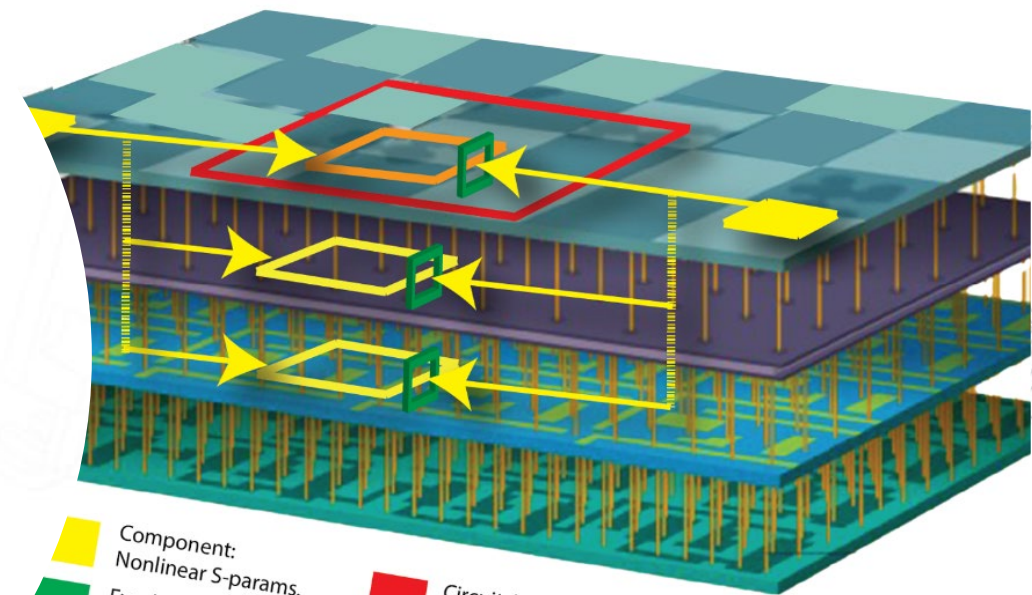
# Example: Metrology for Increasing Circuit Complexity

## Why?

- Increased integration density & functionality
- Add new materials & functionality
- Reduce power, cost, & latency

## What's needed?

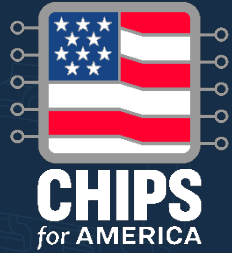
- Evaluate chips, interfaces, and materials buried in multilayer stacks
- New models to evaluate dynamic 3D systems
- Electromagnetic, thermal, & mechanical properties of constituent materials
- Broadband/dynamic material properties



- Component: Nonlinear S-params.
- Fundamental Interfaces: Metal-Semiconductor
- Circuit, board-level imaging: Temp, Efield
- Local Scanned-Probe: Imaging.



# Research Infrastructure



- Support metrology R&D
- Reduce technical risk for emerging technologies

WORLD-CLASS FACILITIES



- Ensure CHIPS R&D is available & useful for stakeholders
- Accelerating data ecosystem by leveraging existing resources

## METIS

Metrology Exchange to Innovate In Semiconductors