CHIPS *for* AMERICA

Manufacturing USA Semiconductor Institute(s)

Summary of Responses to Request for Information

June 1, 2023

Manufacturing USA®

CHIPS *for* AMERICA

NIST NATIONAL INSTITUTE OF STANDARDS AND TECHNOLOGY
U.S. DEPARTMENT OF COMMERCE

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ORGANIZATION OF THE REPORT

This document provides an overview of the stakeholder responses, consensus, and an overarching summary of some of the thematic areas that emerged from the Manufacturing USA Request for Information (RFI).

NIST's approach to summarizing the comments received in the RFI was to capture the range and breadth of public input, including common themes and points of divergence. NIST appreciates the richness of the input received and recognizes that detailed specific comments may not be included in this summary. Readers who would like to see the comments in their entirety can find those at regulations.gov.[1]

The RFI analysis and high-level summary was performed by the NIST team (named below) by categorizing responses by the five RFI topic areas, individual questions and corresponding responses when applicable, and respondent and organization type. Where applicable, the NIST team also appropriately mapped comments from the text of the general responses to specific RFI questions. Where applicable, specific suggestions from the responses were reproduced as part of the high-level summary.

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I. EXECUTIVE SUMMARY

In a Request for Information (RFI) that was published in the Federal Register on October 13, 2022, the National Institute of Standards and Technology (NIST) Office of Advanced Manufacturing requested public input to inform the design of, and requirements for, potential Manufacturing USA institute(s) that would strengthen the semiconductor and microelectronics innovation ecosystem in such areas as design, fabrication, advanced test, assembly, and packaging capabilities.[2] The RFI was open from October 13, 2022 to December 12, 2022. Information was requested in five areas:

1. Institute scope
2. Institute structure and governance
3. Strategies for driving co-investment and engagement
4. Education and workforce development
5. Metrics and success

There were more than 90 responses[3] to the solicitation, with the majority of responses submitted by semiconductor-related industries.

Institute Scope. Responders suggested that the new institutes should be transformational, tackling challenging problems that bridge the gaps from research and development (R&D) to full-scale manufacturing. Several responders suggested focus areas or themes for the new institutes, such as smart manufacturing and packaging, advanced packaging substrate technology, substrate manufacturing, design for manufacturing, and infrastructure to support technology transition to commercial and defense applications. Responders did not reject any of the topics listed in the RFI questions as inappropriate, but also did not indicate a clear consensus for potential topics for a new Manufacturing USA institute or institutes. While no clear consensus emerged from responses with respect to the question of "one super-sized" institute versus two-three smaller institutes, responders agreed that the size of the institute(s) funded should flow from the footprint needed to achieve impact in the chosen technology space. There was an absolute consensus expressed for the need to carefully coordinate the activities and scopes for any new semiconductor Manufacturing USA institutes with those of semiconductor-related R&D investments, including the National Advanced Packaging Manufacturing Program (NAPMP), national semiconductor technology center (NSTC), and existing Manufacturing USA institutes in related spaces.

Institute Structure and Governance. Responders agreed that the original 2013 design framework[4] for Manufacturing USA may still be relevant for informing the design of new Manufacturing USA semiconductor institute(s). Responders also agreed that some of the existing institutes may present a good model for the new institutes. However, responders agreed that the typical scale of the existing institutes is insufficient to have a measurable impact on the capital-intensive semiconductor manufacturing ecosystem.

Strategies for Driving Co-Investment. Responders generally agreed that co-investment[5] by all members in the Manufacturing USA semiconductor institute(s) is important in creating shared value and impact in each institute's mission space. Responders were also in agreement that the co-investment strategy for each institute should be structured to encourage and enable robust participation across the full diversity of stakeholders. Many responders pointed to the need for shared access to capital-intensive equipment, fabrication facilities, and novel materials as essential to success, although there were diverse opinions expressed on how to best achieve that goal. Estimates for the scale of the federal investment needed ranged from $150 million over five years to $1 billion over five years. Most responders noted that federal funding was likely to be needed beyond five years to secure a cohesive partnership, but that, ultimately, the institute(s) could be self-sustainable if properly focused on industry needs.

Education and Workforce Development. Responders generally agreed that the Manufacturing USA semiconductor institute(s) could play a role in supporting experiential learning opportunities for all educational levels, including primary/secondary students through university and postgraduate students along with incumbent workers. The responders suggested that programming will need to include awareness-building, recruitment, training, and upskilling for both technician and engineering levels. Responders further agreed that the new institute(s) should leverage the existing Manufacturing USA education and workforce development (EWD) network other workforce programs, work closely with the existing

institutes in adjacent fields, establish connections with new networks anticipated under NSTC and NAPMP, and engage with universities, trade schools, and community colleges that have diverse education and vocational training. Responders stressed that having a strong partnership with industry members is imperative to ensure that advanced manufacturing workforce development activities effectively address industry priorities. Responders also suggested the institute(s) work closely with industry to ensure a broad talent base is captured, and all community groups, especially those that have been under represented, are given the opportunity for successful careers.

Metrics and Success. Responders agreed on the need to track measures to demonstrate the impact of the Manufacturing USA semiconductor institute(s) on U.S. semiconductor manufacturing ecosystems. Several responders suggested performance metrics aligned with institute objectives to measure both operational and technical progress that can be indicators for innovation and economic competitiveness of the domestic semiconductor industry. Responders also suggested leveraging the best practices of the existing Manufacturing USA institutes and their federal agency sponsors to develop and implement metrics.

II. INTRODUCTION AND BACKGROUND

Semiconductors are fundamental to nearly all modern industrial and national security activities, and are essential building blocks of critical and emerging technologies, such as artificial intelligence (AI), autonomous systems, next-generation communications, and quantum computing.

The U.S. semiconductor industry has historically led in many parts of the semiconductor supply chain, such as R&D, chip design, and manufacturing. Over the past couple of decades, the U.S. position in the global semiconductor industry has dramatically declined. In 2019, the United States accounted for 11 percent of global semiconductor fabrication capacity, down from 13 percent in 2015 and continuing a long-term decline from around 37 percent in 1990.[8] Semiconductor packaging also presents a critical supply chain challenge since less than 3% of global packaging capacity is in North America.[6] Much of the overseas semiconductor manufacturing capacity today is in Taiwan, South Korea, and, increasingly, China.[7]

The fragility of the current global semiconductor supply chain was put squarely on display in 2020. The industry faced significant disruptions as a result of the coronavirus pandemic, a fire affecting a major supplier in Japan, and a severe winter storm that disabled production in facilities in Texas for several days. These events, together with other factors, including pandemic-induced shifts in consumer demand, contributed to a global semiconductor shortage that affected multiple manufacturing sectors that rely on semiconductors as critical components for their finished products. Especially severely hit was the automotive industry, which saw plants idled for months.[9]

The Department of Commerce published an RFI in September of 2021 on the semiconductor supply chain (86 FR 53031, September 24, 2021).[10] More than 150

responses were received from commenters including from nearly every major semiconductor producer as well as representative companies that consume these products across multiple industry sectors. These responses provided new insights into the complex and global semiconductor supply chain.[11]

To strengthen the U.S. position in semiconductor R&D and manufacturing, Congress authorized a set of programs in Title XCIX of the William M. (Mac) Thornberry National Defense Authorization Act for Fiscal Year 2021, Public Law 116-283, as amended by sections 103 and 105 of the Creating Helpful Incentives to Produce Semiconductors for America Act (CHIPS Act) of 2022 (Pub. L. 117-167, Division A), codified at 15 U.S.C. 4651 et seq. (hereinafter, CHIPS for America Act).

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In 2021, President Biden's American Jobs Plan[12] called for at least $50 billion to fund this set of programs. As funded by Section 102 of the CHIPS Act of 2022:

• $39 billion is available for a program to incentivize investment in facilities and equipment in the United States for the fabrication, assembly, testing, advanced packaging, production, or R&D of semiconductors, materials used to manufacture semiconductors, or semiconductor manufacturing equipment.

• $11 billion is available to support several R&D and infrastructure investments including the establishment of an NSTC and NAPMP, the creation of up to three Manufacturing USA institutes targeting semiconductors, and expansion of NIST's metrology R&D in support of semiconductor and microelectronics R&D.

Under Section 9906(f) of the CHIPS for America Act, the Director of NIST may establish up to three Manufacturing USA institutes[13] that are focused on semiconductor manufacturing. In addition, the Secretary of Commerce may award financial assistance or other transactions to any Manufacturing USA institute for work relating to semiconductor manufacturing. Such institutes may emphasize the following:[14]

• Research to support the virtualization and automation of maintenance of semiconductor machinery

• Development of new advanced test, assembly, and packaging capabilities

• Developing and deploying educational and skills training curricula needed to support the industry sector and ensure the United States can build and maintain a trusted and predictable talent pipeline.

Request for Information

The intent of this RFI was to inform the development of up to three Manufacturing USA semiconductor institutes that will strengthen leadership and national resilience of the U.S. semiconductor and microelectronics industry and other industries that rely on microelectronics, through R&D of manufacturing technology, and enhanced EWD.

RFI questions covered major areas about which NIST was seeking comments. They were not intended to limit the topics that may be addressed. Responders were allowed to include any topic believed to have implications for the development of Manufacturing USA semiconductor institute(s), regardless of whether the topic was included in the RFI. In addition, when addressing those topics, responders could choose to address the practices of their organization or a group of organizations with which they are familiar. As desired, responders could also choose to provide information about the type, size, and location of the organization(s). Provision of such information was completely optional and did not affect NIST's consideration.

III. RFI RESPONSE OVERVIEW

NIST requested public input to inform the design of, and requirements for, potential Manufacturing USA institutes to strengthen the semiconductor and microelectronics innovation ecosystem, including design, fabrication, advanced test, assembly, and packaging capability. These Manufacturing USA institutes are authorized in the CHIPS for America Act to support

efforts in R&D as well as EWD. That act also provides for the NSTC, the NAPMP, and NIST Metrology R&D supporting measurement science and standards, all of which are to work together in a complementary fashion. Responses to this RFI may inform NIST's development of funding opportunities for federal assistance or other transactions to establish Manufacturing USA semiconductor institute(s).

The RFI was open from October 13, 2022 to December 12, 2022.

RFI Statistics

The 28 questions of the RFI addressed five areas: Institute scope; institute structure and governance; strategies for driving co-investment and engagement; education and workforce development; and metrics and success (See Table 1). Figures 1 and 2 provide a snapshot of the number of responses received per question and responses by organization type respectively.

Key themes across RFI topics

Institute Scope

Institute coordination: Responders generally viewed the new Manufacturing USA semiconductor institute(s) as complementary to existing ones along with the new R&D investments, and remain aligned with the programmatic purposes of Manufacturing USA. Responders suggested that the new institutes should be transformational, tackling hard problems that bridge the gaps from R&D to full-scale manufacturing. Several responders suggested focus areas or

Table 1. RFI topic areas and focus

		RFI Areas		
Institute Scope	**Institute Structure and Governance**	**Strategies for Driving Co-Investment and Engagement**	**Education and Workforce Development**	**Metrics and Success**
1. Coordination with other CHIPS Act-funded R&D efforts	6. Unique considerations for semiconductor/ microelectronics technology sector	9. Investment tax credit (ITC) for industry	16. Supporting workforce and awareness at all educational levels	25. Sector-specific economic competitiveness, national security, technology innovation
2. Complementarity with and non-duplication of existing MFG USA institutes	7. Risks and benefits of "up to three" semiconductor institutes	10. Factors influencing non-federal co-investment	17. Engaging full diversity of education and vocational training organizations	26. Semiconductor institute-specific education and workforce development
3. Role for existing MFG USA institutes in semiconductor R&D	8. Ensuring stakeholder participation	11. Sustaining institute operations in the absence of continued federal support	18. Ensuring focus and industry priorities	27. Semiconductor manufacturing ecosystem development
4. Scale needed for impact on semiconductor manufacturing innovation		12. Foreign entities	19. Leveraging existing workforce programs	28. First year considerations
5. Appropriate technical scope for impact without duplication		13. Other federally funded programs	20. Success measures	
		14. Interaction with state and local economic development entities	21. Integration of R&D with workforce	
		15. Standards development bodies	22. Building a steady pipeline of skilled workers	
			23. Broadening talent base	
			24. Education and workforce development mechanisms	

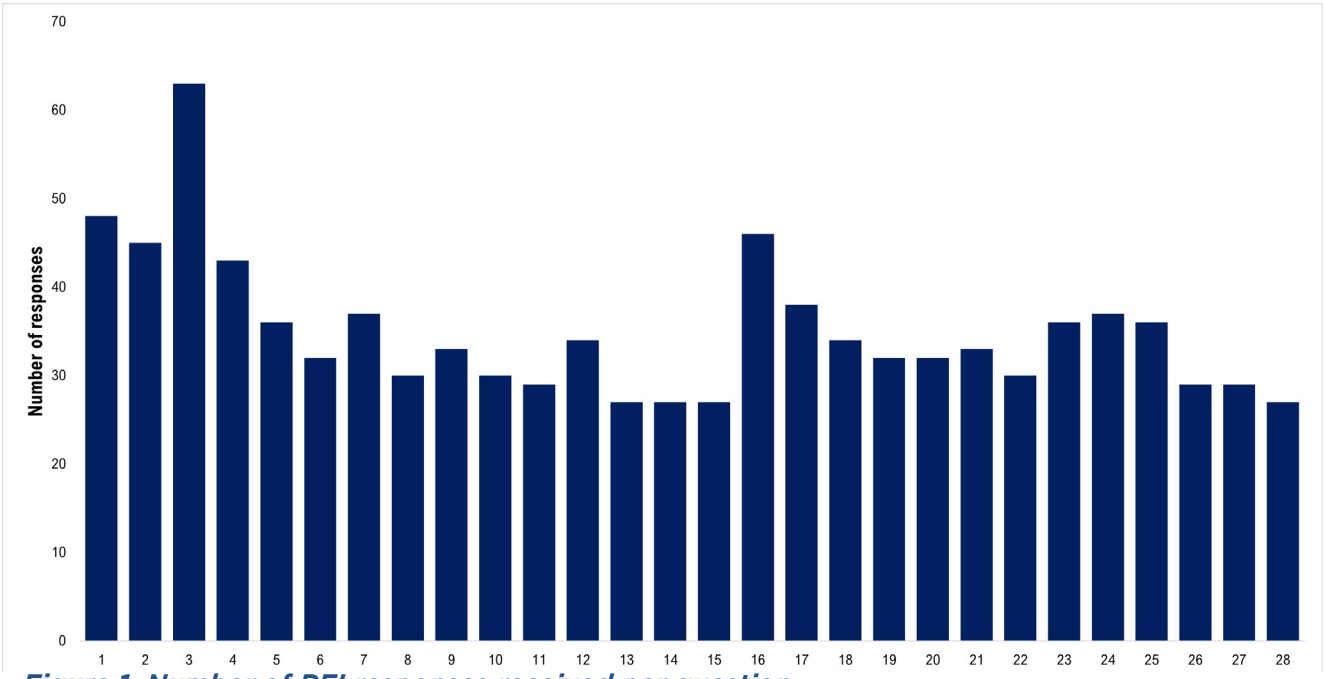

Figure 1. Number of RFI responses received per question

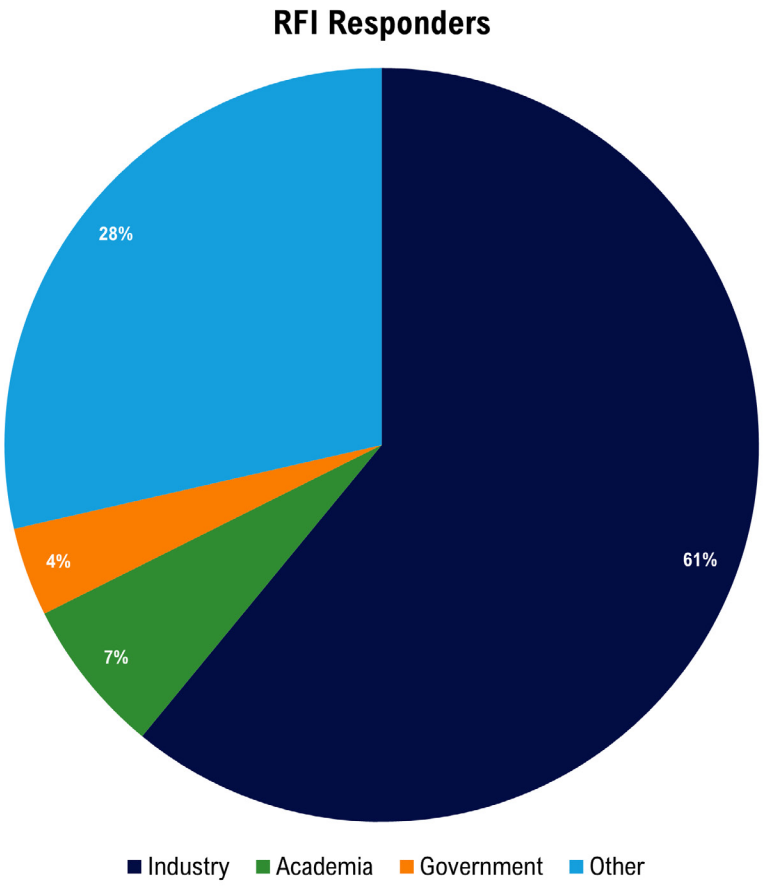

Figure 2. RFI responders by organization type. The government responders included both state and federal. The "Other" category includes responders from Manufacturing USA institutes, non-profits, individuals and all responders who choose to remain anonymous.

themes for the new institutes, such as smart manufacturing and packaging, advanced packaging substrate technology and manufacturing, manufacturing design, and infrastructure to support technology transition to commercial and defense applications. In terms of R&D investments, responders emphasized the importance of non-duplication and complementing existing investments, especially when considering the needs and costs for building additional infrastructure for new semiconductor institutes. It should be noted that this input aligns with the Manufacturing USA authorizing statute,[14] which specifies that new institutes must not substantially duplicate the technology focus of any other Manufacturing USA institute. Responders also stressed relevant collaboration with existing institutes, especially institutes with infrastructure or experience in cross-cutting areas critical to semiconductor manufacturing such as power electronics, flexible electronics, integrated photonics, robotics, and smart manufacturing.

Scope considerations: Responders generally agreed that scoping was key to ensure the impact and success of each new institute and avoid duplication of efforts with existing programs. Responders noted the need for close collaboration and cooperation related to semiconductor R&D initiatives such as the NSTC, NAPMP, and the Department of Defense (DOD) Microelectronics Commons, as well as defining an institute-specific focus that supports the objectives of the CHIPS Act to create impactful ecosystems. In addition to scope-related suggestions, responders also suggested understanding and utilizing synergies with existing and relevant Manufacturing USA institutes and understanding the commonality that exists between defense and commercial industries. They also reiterated the importance of convening industry, small-to-medium enterprises (SMEs), government, and academia to collectively work on the needed innovation, competitiveness, and workforce strategies in the semiconductor and microelectronics space.

Federal and non-federal investment: Several responders suggested a range from $150 million to $250 million in federal funding for new semiconductor institutes over five years, with a few responders further suggesting federal operational funding should be sustained throughout the lifetime of the institute. A few responders noted, in alignment with requirements in the Manufacturing USA authorizing statute,[6] that co-investment should be at least 1:1 for the federal dollar match. A few other responders suggested $250 million per year, with $125 million per year federal funding and $125 million per year non-federal cost share and $600 million over five-years at minimum, and funding levels approaching $1 billion over five-years. Other responses suggested the creation of one large public-private partnership that integrates both microelectronics and advanced packaging technology at a much higher investment level as compared to typical Manufacturing USA institutes, with regional centers established under the Manufacturing USA semiconductor institute(s) in the west, midwest, south, and northeast.

Potential technology focus areas: Several responders favored the RFI-listed potential technology areas of focus and a few others suggested new or alternative topic areas in the scope of an institute. Responders suggested strong partnership and coordination between NSTC and NAPMP on the proposed RFI topic areas to avoid duplication. In terms of coordination with existing Manufacturing USA institutes, responders reiterated the need for relevant collaboration with existing institutes, especially those with infrastructure or experience in cross-cutting areas critical to semiconductor manufacturing. A few responders cautioned relevance of the suggested topic areas to pursue given that the technical objectives of the NSTC and NAPMP have not been established. Related suggestions were to pursue topics broad enough to provide flexibility to the institutes and allow them to align and complement the other Manufacturing USA institutes, NSTC, and NAPMP. Table 2 captures the feedback on the appropriateness of RFI listed scope of work.

Table 2. Feedback on the appropriateness of RFI listed scope of work

Chip-package architectures and co-design of integrated circuits and advanced packaging. May include AI, security, and test methodologies	General agreement, additional sub-topics or emphasis suggested; strong partnership and coordination between NSTC and NAPMP emphasized for this topic and addressing co-design, for example an electronic design automation (EDA) coalition of excellence partnering with device designers and package designers
Technologies to increase the microelectronics manufacturing productivity of American workers, lower costs, and offset the drastic shortfall of skilled workers	General agreement, additional sub-topics or emphasis suggested; suggestion that this topic must be a part of any initiative whether it is part of the NSTC, NAPMP, or a semiconductor institute and not necessarily a standalone effort; suggestion to leverage workforce development programs in NSTC and NAPMP, to modernize curricula and build awareness of the semiconductor industry
Assembly and test metrologies to develop new analytical equipment and analysis capabilities based upon standards	General agreement, additional sub-topics or emphasis suggested; consensus to enable interoperability and traceability of fabrication, packaging, and test data from development to manufacturing phases in support of automation; suggestion for NIST metrology efforts to provide advice, guidance, expertise, and coordination in this topic to enable NSTC, NAPMP, and existing Manufacturing USA programs to achieve their respective goals
Coding and system software with novel computing paradigms and architectures, including chiplet compatibility with earlier generations	Mixed responses, with some sub-topics or emphasis suggested; suggestion that the topic was out-of-scope for semiconductor Manufacturing USA institutes, but within the scope of the NSTC
Integration of security into packaging, interposers, and/or substrates	Mixed responses, with some sub-topics or emphasis suggested; suggestion that this topic be an important component of the overall advanced packaging initiatives or be within the scope of NAPMP coalitions of excellence but not as a standalone topic for an institute
High density interposers and substrates, incorporating new materials and designs	General agreement, additional sub-topics or emphasis suggested; suggestion that the topic should be an important part of the NSTC and Advanced Packaging Institute that is partnered with relevant Manufacturing USA institutes
Chiplet-enabled trusted packaging facilities that obviate the need for trusted foundries	Mixed responses, with some sub-topics or emphasis suggested; responses either suggesting out-of-scope or should collaborate with NAPMP and NSTC; suggestions include lack of clarity that chiplet-enabled trusted packaging can obviate the need for trusted foundries and more research is warranted
New materials, such as glass for substrates, or compound semiconductors	General agreement, additional sub-topics or emphasis suggested. A few suggested that this topic be part of the scope of NSTC and NAPMP
Environmental sustainability for semiconductor manufacturing	General agreement, additional sub-topics or emphasis suggested; suggestions that this topic be part of an overall semiconductor manufacturing mission, not necessarily for a specific institute directive
Analog and gigahertz technology materials and metrology, enabling beyond 5G, the Industrial Internet of Things and Industry 4.0	General agreement, additional sub-topics or emphasis suggested; suggestion to include this topic in both the NSTC and NAPMP goals
Performance and process modeling and metrology	General agreement, additional sub-topics or emphasis suggested; suggestion also included that this topic be part of the advanced packaging ecosystem but not necessarily as a theme for a new institute

Criteria for selection: Responders indicated that the impact on U.S. manufacturing was a key criterion in evaluating a chosen focus area, including how an institute in that focus area would address technology gaps, create a runway to launch novel "leapfrog" technologies and grow a domestic ecosystem and economy. There was broad emphasis on advanced packaging or assembly, test, and packaging as having the most disruptive potential and opportunity for renewed U.S technological leadership since integration of various types of chips has become so complex. Responders indicated that the new institutes focused on semiconductor manufacturing innovation should complement existing Manufacturing USA institutes and the NSTC and NAPMP, while cautioning about the lack of scope clarity of the NSTC and NAPMP. Responders also recommended a focus on productivity while reducing the cost of manufacturing semiconductors, with efforts on EWD and underrepresented minorities.

Technical scope for impact: Responders' interests fell into six categories, predominantly in advanced packaging and smart manufacturing enabled by AI and new materials. Cross-cutting issues of environmental impact, energy efficiency, and especially EWD were included in several categories, namely: advanced packaging, heterogeneous integration (HI), and substrates; design and simulation, often AI-driven; productivity enhancement and smart manufacturing via early design/digital twins and AI; advanced materials; and metrology and testing.

Institute Structure and Governance

Alignment with design principles: Responders agreed that the original national network for manufacturing innovation design principles are aligned with the needs of the semiconductor innovation ecosystems, including the appropriate role for government as a catalyst, not primary stakeholder, and the institutes as hubs connecting innovation ecosystems. However, the responders noted the complexity of the existing relationships and intensity of R&D investments in the mature global ecosystem as unique factors that must be considered in designing the new Manufacturing USA institutes focused on semiconductor manufacturing. Responders also highlighted the importance of plans for sustaining and upgrading any specialized equipment or pilot lines within institutes, given the high capital costs associated with these assets.

Scale of proposed institute(s): The responders had diverse perspectives on the question of how many semiconductor institutes should be established, given that legislation authorizes up to three institutes. However, responders agreed that the typical scale of the existing Manufacturing USA institutes is insufficient to have measurable impact on the capital-intensive semiconductor manufacturing ecosystem. Responders noted that there were benefits to increased geographic coverage with multiple institutes, but also that careful coordination and complementarity of scope was critical to achieving those benefits. Responders also noted that stakeholders may be challenged to navigate membership in multiple institutes and suggested that one "supersized" institute with multiple regional hubs is worth consideration.

Structures to secure stakeholder participation: Most responders agreed that the governance and membership structures for new Manufacturing USA semiconductor institute(s) could largely be modeled on those for existing institutes. Responders agreed that the institute(s) must be industry-led and be inclusive of the broader ecosystem, with low barrier to entry for participation by organizations that serve underrepresented groups. Also noted was the need for easily navigable, multi-year membership agreements with balanced intellectual property (IP) rights consistent with a precompetitive R&D focus.

Fostering technology transitions: Responders pointed to the need for close collaboration

within the ecosystem, including with the NSTC, NAPMP, and existing Manufacturing USA institutes to access fabrication facilities, cross-cutting capabilities, and link access to commercialization partners across application areas. Responders also mentioned that the institutes will need to measure more than just advancement of technology readiness, but also the investment and adoption readiness to succeed in transitioning technology.

Strategies for Driving Co-Investment and Engagement

Co-investment value: Responders generally agree that co-investment by all members in the Manufacturing USA semiconductor institute(s) is important for creating shared value and impact. Responders agreed that cash was the most useful and flexible form of co-investment and should be encouraged. Many responders cited shared access to capital-intensive equipment, fabrication facilities, and novel materials as essential to success, although there were diverse opinions expressed on how to best establish that.

Co-investment strategy: Responders were also in agreement that the co-investment strategy for each institute should be structured to encourage and enable robust participation across all stakeholders. Many responders suggested scaling required co-investment based on member type and anticipated commercial benefit, through tiered membership models with different requirements for cash vs. in-kind commitments, as well as distinct IP rights.

Sustainability: Many responders noted that a thoughtful co-investment strategy coupled with a solid industry-focused business model should support sustainability. However, responders noted that the institute is likely to need federal support beyond five years, given the long timelines often needed before a return on investment (ROI) is tangible to industry.

Investment tax credit impact: Responders were in general agreement that the impact of the investment tax credit for driving industry co-investment in the Manufacturing USA semiconductor institute(s) was promising, yet uncertain at this early stage of enactment.

Education and Workforce Development

Advanced manufacturing workforce development: Responders generally agreed that the Manufacturing USA semiconductor institute(s) should invest in and support experiential learning opportunities for all educational levels, from primary/secondary students through university and postgraduate students, along with incumbent workers. The responders suggested that the programming will need to include awareness-building, recruitment, training, and upskilling for both technician and engineering levels. The majority of responses also stressed the importance of outreach at an early stage. The institute(s) must partner with academia and industry stakeholders to revise the curricula and provide hands-on training, build interest in job opportunities in the field, and recruit a pipeline of candidates.

Diversity of education and vocational training: Responders were generally in agreement that the semiconductor institute(s) should forge a variety of relationships with educational and training organizations to ensure there are sufficient students in the talent pipeline to meet workforce demands. The consensus was that the institute(s) should leverage the existing Manufacturing USA EWD network and work closely with the existing institutes in adjacent fields, establish networks and partnerships via NSTC and NAPMP, and engage with universities, trade schools, and community colleges that have diverse education and vocational training. The responders also emphasized the importance of curriculum updates through co-op and intern programs to provide on-the-job

training that would meet the needs of the industry. Development of a toolkit that addresses educational, certification, and career pathways to close the skills gap in manufacturing was also suggested.

Addressing industry priorities: The responders stressed that strong partnerships with industry members are essential to ensure advanced manufacturing workforce development activities effectively address industry priorities. Suggestions included aligning regional workforce development programs with organizations that already have deep EWD penetration in industry, or rotating industry professionals into community colleges and universities to teach specific classes and courses. A few responses suggested that workforce development activities should correlate with industry roadmapping activities to address skill gaps and competencies needed for advanced manufacturing.

Complementary partnerships: Responders suggested institute(s) partner with organizations that have access to existing training facilities and resources as they customize EWD programs for optimal support of their membership and the nation at large. Collaboration with National Science Foundation (NSF) and regional/state programs to leverage existing programs was also suggested.

Measure of Success: Responders suggested that the determination of appropriate metrics will largely depend on the specific programs and projects that the institute chooses to implement. Generally, responders agreed that institutes and NIST as the sponsoring agency of the semiconductor manufacturing institute(s) could assess successful recruitment and retention of a well-trained, diverse workforce. Responders suggested quantitative metrics could capture elements such as diversity statistics on race and gender, number of internship/apprenticeships, and enrollment in university science, technology, engineering and mathematics (STEM) majors, and in vocational training. Many responders also suggested that quantitative metrics could be developed for the number of partnerships with universities, industry markets served by institute-developed programs, the number of relevant degrees and certificates awarded, workers placed in semiconductor manufacturing jobs, and the growth of regional job fairs.

R&D integration with workforce: Responders suggested strengthening industry and academic partnerships in part through demonstrations of state-of-the-art technology. Suggestions included addressing a need for increased R&D in STEM majors and careers, innovative new graduate curricula and team science training, work-based learning opportunities such as learn and earn programs, internships, and apprenticeships with R&D departments, and integration of R&D activities with education utilizing local leading Manufacturing Extension Partnership (MEP) centers.

Pipeline of skilled workers: Responders suggested several mechanisms to achieve a steady pipeline of skilled workers by assessing industry needs and growing the talent pipeline while also promoting diversity, equity, and inclusion. Suggestions included forming strong partnerships with government, industry, non-profits, and academic stakeholders to develop kindergarten to 12th grade (K-12) or post-secondary educational training programs. Responders also suggested cross-promoting professional and multidisciplinary technical knowledge, skills, and abilities that are needed to revitalize the nation's semiconductor manufacturing. It was noted that these skills are currently held by workers in several different manufacturing and STEM fields, including automotive, aerospace, and transportation. In addition, some responders listed specific job titles and occupations that could transition workers to semiconductor manufacturing.

Broadening the talent base: Responders suggested partnering and tailoring activities with community groups, professional associations, and affinity organizations that have been underrepresented in semiconductor manufacturing. Reaching women and minorities was reiterated as important for the current manufacturing culture. Responders also suggested the institute(s) work closely with industry to ensure a broad talent base is captured, and all community groups, especially those that have been under represented, are empowered and given the opportunity for successful careers. Lastly, outreach in coordination with NSTC and NAPMP was highlighted to effectively leverage federal resources to ensure greatest impact.

Education and workforce development activities: Responders proposed several types of EWD activities to target specific audiences for different training functions. Suggestions included hybrid curricula, hands-on engagement, experiential learning programs, mobile learning lab, accessible job outlook pathways, short courses and certifications, mentor training, and train-the-trainer programs. Most responders agreed that partnerships with other government, academic, and private organizations will help expand outreach, accessibility, and impact of EWD activities. Responders, once again, also mentioned the importance of diversity, equity, and inclusion in all education and workforce training activities.

Metrics and Success

Performance metrics: Responders agreed on the need to track measures to demonstrate impact of the Manufacturing USA semiconductor institute(s) on U.S. semiconductor manufacturing ecosystems. Several responders suggested aligning metrics with institute objectives, to measure both operational and technical progress and impact on innovation, economic competitiveness, and national security. There were also a few responses suggesting sector-specific metrics like decreased imports of foreign components, raw materials, and services.

Education and workforce development metrics: Responders suggested that impact should be measured across the entire supply chain from component production to finished products for manufacturers involved in the institute. Related metrics potentially include time needed to train workers to achieve proficiency, productivity, gauge training effectiveness, number of internships, technician/trade certificates awarded, degrees awarded, and number of hires by the semiconductor industry and its supporting ecosystem.

Metrics supporting U.S. semiconductor manufacturing ecosystem: Responders generally favored impact metrics measured by commercial activities such as number of startups in the institute field, jobs added per year in the related industrial sector, number of new products introduced with semiconductor technology, sales volume related to technology development facilitated by the institute, patents and patent-protected sales for technology generated by the institute, commercial viability and institute facilitated deployment of technologies, and expansion of domestic manufacturing capacity. Several responders also suggested technology-specific output metrics such as wafers per month or number of new chips built that use advanced substrates developed and used at the new institute. For broader impact, responders suggested surveying semiconductor companies and members of the institutes while simultaneously considering other global semiconductor institution metrics to best evaluate the performance and impact in establishing and expanding the ecosystem related to knowledge transfer, collaboration, pipeline and job creation, safety, quality, delivery, and growth.

First-year success metrics: Several responders suggested year-one success metrics such as institute bylaws established with initial member participation, paid company

membership dues that represent at least a 50% market share in the markets the institute aims to influence, second-year dues payments received from at least 90% of first-year members, committed state funding for over five years, and member input significantly guiding institute value proposition, technology roadmap, and business plan and budget. Responders also suggested key considerations while setting up the new institutes such as defining clear scope and mission, capitalizing on existing industry and public and private partnerships, and finalizing key institute operational documents.

Forms of support: Responders suggested establishing clear governance and interactions with NSTC and NAPMP and partnership with existing Manufacturing USA institutes. Support from NIST, the NAPMP and NSTC (including governance structures for those programs), and partnership with existing Manufacturing USA institutes are essential for early success. Other suggestions addressed developing a strategic plan and framework in alignment with Manufacturing USA and Department of Commerce strategic goals and leveraging other federal agencies and state and local government interests.

IV. RFI CATEGORIAL RESPONSES

Institute Scope

1. Coordination with other CHIPS-Act-funded R&D efforts

RFI Question 1: The Manufacturing USA semiconductor institute program is one component of an $11 billion R&D effort that includes the National Advanced Packaging Manufacturing Program, the National Semiconductor Technology Center and the NIST Metrology R&D. The entire R&D program is intended to be interconnected and comprehensive, with no gaps and minimal redundancy, to position the United States for technology and workforce leadership in the semiconductor and microelectronics sector for the long-term prosperity of the nation. Additionally, the Manufacturing USA authorizing statute specifies that new institutes must not substantially duplicate the technology focus of any other Manufacturing USA institute. From your perspective, what role do you envision for new Manufacturing USA semiconductor institutes that will best complement the other R&D investments and remain consistent with the programmatic purposes of Manufacturing USA? Since the Secretary of Commerce may award financial assistance to any existing Manufacturing USA institutes for work relating to semiconductor manufacturing, what role do you envision for existing, federally sponsored Manufacturing USA institutes with respect to semiconductor manufacturing?

RFI Question 1 Response Summary:

The majorityof the responders for this question viewed the new Manufacturing USA semiconductor institute(s) to complement existing and new R&D investments and remain aligned with the programmatic purposes of Manufacturing USA. Many responses specifically suggested potential focus areas and priorities for the new institutes, related R&D investments, and coordination aspects to consider alongside already-existing Manufacturing USA institutes.

In terms of priorities, multiple responses suggested that the new institutes should be transformational, tackling hard problems that bridge the gaps from R&D to full-scale manufacturing. The new institutes should grow domestic capabilities for semiconductors, thus reducing dependence on the global supply chain, and focus on next-generation manufacturing technology. Several responses reiterated the specific objectives of the CHIPS Act itself as central to the mission of the new institutes, such as reshoring semiconductor manufacturing, focusing on workforce development, and establishing leadership in the security of

the semiconductor supply chain. Several responses also suggested potential focus areas or themes for the new institutes such as advanced smart manufacturing and packaging, advanced packaging substrate technology and manufacturing, and infrastructure to support technology transition to commercial and defense applications. In addition, a few responses generally agreed to the possible themes as listed in the RFI as scope for each of the new Manufacturing USA institutes with a priority to improve domestic microelectronics manufacturing productivity and America's economic competitiveness overall. Several responses especially emphasized specific capabilities for the new institutes such as: wafer level HI, innovative interconnects, nanoscale metrology, intelligent design, assembly, packaging and test methodologies, standards, cyber security, certification, workforce development, networking and streamlined contracting, semiconductor chip manufacturing lifecycle, supply chain gaps, end-to-end digital thread across semiconductor and microelectronics design and AI-enabled advanced digital simulation.

In terms of semiconductor related R&D investments, several responses emphasized not duplicating but instead complementing existing investments and building additional infrastructure for the new semiconductor Institutes. There were suggestions that the new institute(s) should consider the activities of other existing Manufacturing USA institutes as well as other initiatives funded by DOD and other federal agencies. In relation to coordination with existing Manufacturing USA institutes, several responses repeated the need for meaningful collaboration with existing institutes, especially those with infrastructure or experience in cross-cutting areas in semiconductor manufacturing such as advanced packaging, power electronics, flexible electronics, integrated photonics, robotics, and smart manufacturing.

2. Complementarity with and non-duplication of existing Manufacturing USA institutes

RFI Question 2: The technological breadth of innovation in semiconductors and microelectronics is likely larger than can be served by any single Manufacturing USA institute. Therefore, each Manufacturing USA semiconductor institute should have an appropriate scope to ensure that each institute is impactful and does not duplicate efforts of other programs. Historically, institutes in the current network of existing Manufacturing USA institutes have generally been funded for an initial 5 years at $150 million to $600 million, including federal funding and cost-sharing (co-investment) from non-federal partners. What would be the ideal scope and corresponding financial investment from federal and non-federal partners, for a Manufacturing USA semiconductor institute to achieve the needed impact on competitiveness?

RFI Question 2 Response Summary:

The consensus from the responders to this question was that, given the technological breadth of innovation in semiconductors and microelectronics, appropriate scoping (and avoiding duplication of efforts with existing programs) was key to ensuring the impact and success of each new institute. Several responses suggested the ideal scope and focus for new semiconductor institutes. Suggestions included advanced packaging and smart manufacturing, substrate technology development, design virtualization and visualization, hardware design simplification, materials and wafer processing, three-dimensional heterogeneous integration (3DHI) analog semiconductors, wide and ultra-wide bandgap semiconductor fabrication, semiconductor workforce development, metrology focus, scalable assembly tools, etc. A few responses also noted the need for close collaboration and cooperation related to R&D initiatives such as the NSTC, NAPMP, and DOD Microelectronics Commons,

and defined an institute-specific focus to address the objectives of the CHIPS Act and create impactful ecosystems. Several responses also suggested understanding and utilizing synergies with existing and relevant Manufacturing USA institutes, understanding the commonality that exists between defense and commercial industries, and reiterated the importance to convene industry, SMEs, government, and academia to collectively work on the needed innovation, competitiveness, and workforce strategies in the semiconductor and microelectronics space.

Other relevant scope-related coordination comments included leveraging existing semiconductor facilities and equipment, generating open source technology within the industry, building prototype hardware or strongly support building hardware with cost-effective end-to-end prototyping to manufacturing, investigating new methods to form reliable interconnects, establishing an open/neutral semiconductor and microelectronics marketplace to expedite and reduce cost for hardware/prototype production and services across the end-to-end digital thread to facilitate commercialization, emphasizing hands-on techniques and expertise for semiconductor workforce training and creating a national network of pilot line resources.

In terms of corresponding federal investments, several responses ranged from $150 to $250 million for new semiconductor institutes over five years, with a few responses suggesting federal operational funding should be sustained throughout the lifetime of the institute. A few responses noted that the federal cost share should be at least 1:1. Other responses suggested $250 million annually, comprising half from federal funding and the other half from non-federal cost share and $600 million over five-years at minimum and funding levels approaching $1 billion over five-years. There were also responses suggesting the creation of one large public-private partnership that integrates both microelectronics and advanced packaging technology at a much higher investment level as compared to typical Manufacturing USA institutes, and establishing four regional centers under the Manufacturing USA semiconductor institute(s) in the west, midwest, south, and northeast of the country. Another suggestion proposed a $250 million federal investment over five years to expand existing Manufacturing USA efforts in smart manufacturing, cybersecurity, robotics, and digital transformation within semiconductor manufacturing. There was a suggestion for institute cost to be one-third from federal funding, one-third from state funding and one-third from industrial and academic institutions.

3. Role for existing Manufacturing USA institutes in semiconductor R&D

RFI Question 3: Potential technology areas of focus that could be addressed by the Manufacturing USA semiconductor institutes to complement the National Advanced Packaging Manufacturing Program and the National Semiconductor Technology Center in Question 1 are listed below. What are your thoughts on the appropriateness of each for the scope of work for a Manufacturing USA semiconductor institute? What other topics should be included in the scope of an institute?

- Chip-package architectures and co-design of integrated circuits and advanced packaging. May include AI, security, test methodologies, etc.
- Technologies to increase the microelectronics manufacturing productivity of American workers, lower costs and offset the drastic shortfall of skilled workers
- Assembly and test metrologies to develop new analytical equipment and analysis capabilities based upon standards
- Coding and system software with novel computing paradigms and

architectures, including chiplet compatibility with earlier generations

- Integration of security into packaging, interposers and/or substrates
- High density interposers and substrates, incorporating new materials and designs
- Chiplet-enabled trusted packaging facilities that obviate the need for trusted foundries
- New materials, such as glass for substrates, or compound semiconductors
- Environmental sustainability for semiconductor manufacturing
- Analog and gigahertz technology materials and metrology, enabling beyond 5G, the Industrial Internet of Things and Industry 4.0
- Performance and process modeling and metrology

RFI Question 3 Response Summary:

The majority of the responders to this question were in favor of the potential technology areas of focus proposed in the RFI. Of those responses, more than 40 came from industry and included specific recommendations on the focus and scope of these technology areas. There were also several responses that suggested new or alternative topic areas.

a. Chip-package architectures and co-design of integrated circuits and advanced packaging. May include artificial intelligence, security, test methodologies, etc.

There was general agreement for an institute to support a diverse set of AI, communications, sensing, and networking applications. Suggested sub-topics included: architectures for security-confidential computing, data integrity, privacy, and data attestation; thermal management based on materials and electrical conductivity; package manufacturing including particle defect inspection and three-dimensional (3D) packaging; computational lithography and process-informed lithography; AI for lithography, tools for design productivity, virtual fabrication-tools for manufacturing productivity; architectures optimized for quantum materials and devices, photonic integrated circuits, and radio frequency (RF) and higher frequency applications; harsh environment hardening via novel packaging and hetero-integration driven by AI-enhanced system partitioning; advancing and coordinating hetrogenerous intergration capabilities in the areas of standards, verification, packaging, and validation capabilities; co-design coupled with accurate chip-package interactions through modeling and simulation of 3DHI architectures for harsh environments; co-designed integrated circuits for signal integrity, thermal, optical, and mechanical properties; post-assembly and post-packaging repair and reconfiguration to support defect and variation tolerance; heterogeneous processing near memory and storage architectures for data/media analytics applications; reconfigurable fabrics for hardware obfuscation and secure split manufacturing; carbon nanotubes; and high-performance computing.

A few comments suggested addressing co-design by an EDA coalition of excellence partnering with device designers and package designers alongside strong partnership and coordination between NSTC and NAPMP.

b. Technologies to increase the microelectronics manufacturing productivity of American workers, lower costs and offset the drastic shortfall of skilled workers

Several comments supported increasing American microelectronics manufacturing productivity, lowering costs, and addressing the drastic shortfall of skilled workers. Suggested sub-topics included: digital twins focusing on big data analytics for manufacturing; testing including virtualization and maintenance automation for productivity; multi-project wafers to

provide access to high-quality materials and devices; leveraging co-design of automated manufacturing equipment within the prototype; AI-enhanced co-design for microelectronics; front-end fabrication and back-end advanced packaging technology to develop tools and techniques that improve efficiency and maximize ROI, lower costs, and maximize American worker efficiency; online training classes and industry-supported certifications to include additive, digital twins, automation, cyber security, AI, augmented reality (AR), virtual reality (VR), advanced analytics, sensors, machine learning, robotics, computing, and communications; and automation of the entire end-to-end process including design, manufacturing, testing, and packaging.

A few responses suggested that while productivity, automation, and smart manufacturing methods must be a part of any initiative (whether part of NSTC, NAPMP or Manufacturing USA network), the topic addressing the shortfall of skilled workers should not be a standalone effort for a semiconductor institute. Leveraging workforce development programs in NSTC and NAPMP were also suggested to modernize curricula and build awareness of the semiconductor industry.

c. *Assembly and test metrologies to develop new analytical equipment and analysis capabilities based upon standards*

There was general agreement for this topic to enable interoperability and traceability of fabrication, packaging, and test data from development to manufacturing phases through automation. Suggested sub-topics included: novel assembly and test metrologies, automated testing of advanced microelectronic packaging, infrastructure for flexible, comprehensive, automatic post-assembly and in-field testing and characterization, user-friendly interface, data analysis, and visualization tools; new advanced packaging technology approaches for wafer stacking and die-on-die or die-on-wafer assembly and new approaches to maintaining signal integrity while connecting heterogeneous devices; in-line and final test methodologies and equipment; new metrologies to maximize yield and binning; screening 3DHI analog semiconductors; non-contact and non-destructive test metrologies; advanced testing capability that matches feature scaling; and automated testing of advanced microelectronic packaging.

A few responses suggested the NIST metrology program provide advice, guidance, expertise, and coordination in this area to enable NSTC, NAPMP, and existing Manufacturing USA programs to achieve their respective goals.

d. *Coding and system software with novel computing paradigms and architectures, including chiplet compatibility with earlier generations*

This topic generated mixed responses. Responses in favor included the following: relevant significance in advancing 5G and successor wireless technologies; software and novel computing paradigms and architectures for 3DHI analog semiconductors; expand the availability of design and enablement tools; develop chiplet or 3DHI modeling methodology to optimize across electrical, thermal, electromagnetics, and related areas; development of prognostics and health management capabilities down to the chip level; and an open chiplet ecosystem to drive to a standardized open chiplet architecture and fabrication, etc.

A few responses suggested that the topic was out-of-scope for semiconductor Manufacturing USA institutes, but within the scope of the NSTC.

e. *Integration of security into packaging, interposers and/or substrates*

Several responses agreed with integration of security into packaging, interposers and/or substrates. Suggested sub-topics included: anti-tamper enclosures to secure multiple-chip modules, modular and composable

security solutions; trusted anchors, novel chiplet design and partitioning, and novel packaging processes; embedded security features in 3DHI analog semiconductors; advancements in lithography capability critical for substrates to address next generation high-density and device integration requirements; and physical product protections, anti-tamper, secure packaging, anti-reverse engineering, hardware locking self-destruction, digital thread, cyber resiliency, in-field reconfigurability and edge processing.

A few responses noted that while this topic is an important component of overall advanced packaging initiatives and should be within the scope of NAPMP coalitions of excellence, it should not serve as a standalone topic for an institute.

f. High density interposers and substrates, incorporating new materials and designs

There were several responses in favor of this topic. Suggested sub-topics included: reconfigurable interposers for reusability, defect/variation tolerance, and isolation; monolithic 3D heterogeneous architectures; new rigid 3D substrate technologies to provide a significant edge in terms of reduced loss, improved performance, increased reliability, thermal management, and cost; new advanced test, assembly, and packaging capabilities for HI; interposer developments to leverage existing and future small pitch die with higher power requirements; reference design libraries for interposer design; development of novel interconnect methodologies that are equal to or better than bump technologies and wire bond capabilities; and manufacturing-focused hardware effort to support bringing substrates and laminates in domestic manufacturing.

A few responses suggested that the topic should be an important part of NAPMP as part of an Advanced Packaging Institute that would partner with any relevant Manufacturing USA institutes.

g. Chiplet-enabled trusted packaging facilities that obviate the need for trusted foundries

This topic generated mixed responses. Suggested sub-topics included: a need to add and upgrade trusted power semiconductor packaging facilities for military applications; the value in embedding security features in 3DHI analog semiconductors which are tightly integrated with and supply communications and power to digital chiplets such that the digital chiplets do not need to be fabricated in trusted foundries; chiplet architectures can be more prone to security threats from side channel attacks due to signals exiting the chiplets; focus on establishing the facility first, then establish trusted accreditation; focus on non-silicon compound semiconductor materials; the importance of compound semiconductors critical for defense and commercial applications, including gallium nitride (GaN), gallium arsenide (GaAs), indium phosphide (InP), silicon–germanium (SiGe), and others emerging aluminum gallium nitride (AlGaN), scandium-doped aluminum nitride (ScAlN), indium gallium arsenide (InGaAs), and gallium oxide compounds; development of high thermal conductivity materials to be used internally and externally to the device; multi-material additive manufacturing envisioned to create all levels of packaging; new dielectric and thin film tools and processes; glass as a critical area for low-loss RF systems, and the desire for additional onshore manufacturing for glass substrates; investment in reliable and sustainable sourcing for critical materials; enabling low-cost equipment to meet environmental regulations for air, water, and solid waste treatment; and chiplet standards such as Universal Chiplet Interconnect Express (UCIe) offer an opportunity for standardized packaging and trusted packaging facilities.

A few responses either suggested this topic was out of scope for Manufacturing USA institutes and they should, instead, collaborate with relevant centers of excellence in the NAPMP and NSTC. There was a suggestion that the chiplet-enabled trusted packaging facilities is best integrated into manufacturing lines but the associated costs with setting up and operating such a facility are beyond the budget for a Manufacturing USA institute. A few responses suggested that chiplet-enabled trusted packaging may not obviate the need for trusted foundries and more research is warranted.

h. New materials, such as glass for substrates, or compound semiconductors

The majority of responses were in favor of this topic. Suggested sub-topics included: raw materials and crystal growth to support the supply chain; materials for optoelectronics and photonic integrated circuits; two-dimensional materials for integration with Si, ferroelectric materials, nanoscale magnetic materials; materials and device design with prototyping for power electronics (e.g., Silicon carbide (SiC), GaN, Gallium(III) oxide (Ga2O3); specialty glasses and ceramics, materials for displays (inorganic and organic); new polymers and polymer composites for high-frequency packages, high voltage, and harsh environments; need for incubator for emerging technologies that utilize emerging materials for semiconductor manufacturing and new insulating materials for power semiconductor modules such as diamond to improve high-voltage insulation and thermal conductivity; glass substrates, compound semiconductors, and thin-film capacitors, inductors and diamond heat spreaders are required for 3DHI analog semiconductors and carbon nanotubes; new growth and synthesis processes and methods are needed to permit growth and development of novel material devices and device architectures; low-cost 3D wafer-level hermetic heterogeneous packaging and packaging methodologies for systems that combine digital and analog (RF and optical) signals; and new materials, such as glass for substrates can offer low-parasitic, scalable (beyond 300 mm wafer size), and relatively low-cost platforms.

A few responses suggested the topic was within the scope of NSTC/NAPMP but outside the scope of the new institutes.

i. Environmental sustainability for semiconductor manufacturing

Multiple responses were in favor of this topic. Comments and suggestions included: advances in semiconductor device technologies that have less switching energy and less leakage power; signaling circuits that enable high-speed data transmission using less energy; architectures that match the demands of data-intensive applications; programming systems that reduce software bloat while also enabling productive development of high-performance applications; manufacturing materials and processes compatible with world standards of sustainable development; high-volume, low-mix fabrication facilities with a higher likelihood for environmental sustainability; internal rate of return and economic rate of return payoffs; maximizing equipment and process efficiency while minimizing power, chemicals, water, and waste; multi-disciplinary research agenda including socio-technical factors; explore digital twins to drive higher productivity and reduce resources requirements; explore 3DHI analog semiconductors to improve semiconductor manufacturing environmental sustainability; and explore carbon nanotube microchip manufacture.

A few responses suggested that while this is a very important part of the overall mission, it should be a part of the overall semiconductor manufacturing institute scope, not a specific institute directive.

j. Analog and gigahertz technology materials and metrology, enabling beyond 5G, the Industrial Internet of Things and Industry 4.0

Most responses were in favor of this topic. Suggestions, comments, and subtopics raised included: explore analog, RF and 5G transmission and reception potential; millimeter wave and sub-terahertz (mmWave/sub-THz) advanced RF systems in a package for 6G communications and advanced sensing; 3DHI significantly reduces parasitics enabling a significant increase in analog semiconductors operating frequency which, in turn, requires new materials and metrology to support this higher performance operating regime and to provide better signal shielding for low voltage analog circuitry; development of critical RF materials sourcing including materials like benzocyclobutene, liquid crystal polymer, polyimide and polytetrafluoroethylene materials; enable remote sensing and diagnostics for support and maintenance of the machinery; digital twin and digital thread technology; and full-spectrum electronic warfaretechnology.

There was also a suggestion to include this topic in NSTC and NAPMP goals.

k. Performance and process modeling and metrology

Most responses were in favor of this topic. Suggested sub-topics included: virtual models to understand the dynamics of the growth of unconventional materials to characterize defects and increase yield, EDA software for design and simulation of system-in-package architectures, tools for design and simulation of system-in-package architectures, and screening metrology methods and models to identify production reliability weak links in process and device design; development of hardware and software to design, fabricate, package, and deploy computing technology; metrology and test tools, techniques, and data management critical to data acquisition and insights derived from that data without which an AI-driven smart fabrication or advanced packaging line would not be possible; holistic co-design and optimization of 3DHI analog semiconductors and their manufacturing and testing/binning from wafer fabrication; and advanced modeling capabilities for complex microsystems (e.g., 3DHI, 2.5D packaging, etc.) to enable automated design optimization.

One responder suggested that this topic be part of the advanced packaging ecosystem but not as a theme for a new institute. A few responses cautioning relevance of the suggested topic areas include: difficulty to select specific topic areas for the Manufacturing USA institutes to pursue since technical objectives of NSTC and NAPMP have not yet been established; topics selected should be broad enough to provide flexibility to the institutes and allow them to align and complement the other Manufacturing USA institutes, NSTC, and NAPMP; a clear mission statement for the NSTC, NAPMP and Manufacturing USA programs should be one of the first deliverables of the CHIPS Program Office to better guide scope considerations, with appropriate care taken that to avoid duplication and clearly articulate inputs and outputs of each.

Some suggested that the proposed RFI topics were not exactly appropriate for Manufacturing USA institutes and recommended consolidation of several topic areas in conjunction with NAPMP programs and projects. For example, one suggestion was to incorporate the following topics into NAPMP programs and projects, in conjunction with NIST, to ensure focus and eliminate duplication: assembly and test metrologies to develop new analytical equipment and analysis capabilities based upon standards; integration of security into packaging, interposers, and/or substrates; high density interposers and substrates, incorporating new materials and designs; Industry 4.0; performance and process modeling and metrology; new materials, such as glass for substrates, or compound semiconductors; and environmental sustainability for semiconductor manufacturing. Yet another response

suggested combining topics "technologies to increase the microelectronics manufacturing productivity of American workers, lower costs and offset the drastic shortfall of skilled workers," "new materials, such as glass for substrates, or compound semiconductors," "analog and gigahertz technology materials and metrology, enabling beyond 5G, the industrial internet of things and industry 4.0," and "performance and process modeling and metrology" to be combined under a single institute to save cost and drive synergies.

Other related topic suggestions included: design for longer product life, reducing electro magnetic pulse susceptibility; focus on "applications," such as an automotive and smart machines, tools to automate the chip design from code to transistors; low-volume, high-mix leapfrog technology manufacturing; periodic certification of entities to check compliance with CHIPS Act criteria; emerging memory technologies such as spin-transfer torque magnetoresistive random access memory; widely applicable manufacturing process for piezoelectric nano systems; in-situ physics-of-failure analysis capabilities; advanced glass packaging for high-frequency applications can immediately impact the emerging field of room-temperature quantum transducers; micro electro mechanical systems (MEMS); complementary metal-oxide-semiconductor image sensor chips; high-temperature furnace elements; mining and purification of raw materials; recycling waste streams; specialized equipment that could reduce consumption of materials in chip manufacturing, transitioning and adopting green manufacturing processes; advanced products based on unique in-space produced materials (novel materials grown in microgravity); improve plasma power metrology; producing and updating/upgrading technology roadmaps and environmental analysis; thermal management across all levels in the hierarchy; advanced packaging planning software tools; high-temperature and radiation-hardened semiconductor devices; smart machinery control systems for modernized semiconductor technology and modernization of infrastructure; semiconductor/microelectronic supplier diversity index for tiers, different industries or applications; and secure blockchain networks and standards for the semiconductor and microelectronic ecosystems.

4. Scale needed for impact on semiconductor manufacturing innovation

RFI Question 4: What criteria should be used to select technology focus areas in delineating the scope for a Manufacturing USA institute focused on semiconductor manufacturing?

RFI Question 4 Response Summary:

There was consensus that institute focus should be based fundamentally on making the largest possible impact on U.S. manufacturing. Specifically, responders suggested posing the question, "does the focus area create a runway to launch novel, leapfrog technologies and grow the U.S.-based ecosystem/ economy?" There was broad emphasis on advanced packaging as having the most disruptive potential and opportunity for renewed U.S technological leadership since integration of various types of chips has become so complex. Packaging was stated by several as an enabler of the next microelectronic revolution, even by silicon chip-focused organizations.

Widespread recommendations were made that the new institute(s) complement existing Manufacturing USA institutes and the NSTC and NAPMP. However, there was an array of responses with respect to how the relationships would best be structured, especially given the as-yet undefined scope of the NSTC and NAPMP. Some responders recommended that the new semiconductor Manufacturing USA institutes develop manufacturing processes for NSTC/NAPMP output, while others conversely suggested

the institutes act as early technology readiness level (TRL) feeders for the NSTC and NAPMP. Also recommended was to have the institutes support cross-cutting technologies that may enhance the efforts of NSTC or NAPMP, without clearly falling into a single topic area.

Several responders recommended a focus on reducing the cost of manufacturing semiconductors, with additional efforts on promoting the impact of technology through EWD and recruitment and training of underrepresented communities.

There was widespread recommendation to address gaps, including holes in the current manufacturing ecosystem (particularly in segments of the ecosystem that are vulnerable to facility access disruption in South East Asia) and to make the U.S. more competitive.

In the former category, several responders stated that without developing technology to support a self-sustaining substrate industry, the U.S. will remain dependent on Asia for a critical piece in the semiconductor supply chain. The U.S. should focus on leapfrogging technologies for making differentiated substrates. Fabrication tools and assembly, testing, and packaging improvements were often recommended. A novel concept suggested that the institutes focus on critical technology that already has been identified and controlled against exportation under U.S. export laws.

To increase U.S. competitiveness, responders suggested the U.S. could ideally create something that cannot be easily replicated in existing facilities in other countries, making it harder for competitor nations to catch up to U.S. capabilities. Examples provided by the responders included novel core materials in substrates, glass or silicon, large panel cores, GaN laser diode technology, emerging technologies, and potential breakthrough areas (e.g., quantum, materials).

Responders also suggested that the proposed institutes be selected for potential impacts on energy efficiency, productivity, chemical budget, and reuse to push U.S. industry towards a circular economy.

5. Appropriate technical scope for impact without duplication

RFI Question 5: What technology focus areas that meet the criteria suggested in Question 4 above would you be willing to co-invest in?

RFI Question 5 Response Summary:

Responders' interests fell into six categories, predominantly in advanced packaging and smart manufacturing enabled by AI and new materials. Cross-cutting issues of environmental impact, energy efficiency, and especially EWD were included in several categories. Responses related to advanced packaging and HI included:

- Design, verification, and AI co-design of chips/chiplets and new chip-package architectures, which may include AI, security, and test methodologies, all to accelerate Industry 4.0
- HI for analog semiconductors, which would expand the field to many more companies than digital and would complement the focus of NSTC
- Design integrated workflow that is predictive for multi-domains (electrical, thermo-mechanical), secure, and provides trusted traceability ("secure advanced package design")
- Increased bandwidth for chip-to-chip communications on a substrate, and low power chip-to-chip communication and power delivery thermal management of high-power chips
- Applications for reliability and harsh environments

Responses related to substrates included:

- Advanced substrates, interposers, and laminates (glass, SiC, GaN) for RF communications and power control technologies, including MEMS switches, sensors, and HI
- Include non-captive prototyping and production cleanroom space focused for advanced substrates
- Substrates enabling greater electrification, communication, and Industry 4.0

Responses related to design and simulation, often AI-driven included:

- Design and simulation for advanced packaging, including AI co-design and verification, next-generation predictive electronic design, and HI
- AI methods for system verification, quality assurance, error detection and identification of optimal architecture for classes of circuit design and packaging
- Hardware design simplification to enable engineers with moderate software coding capability to design a leading-edge processor

Responses related to productivity enhancement and smart manufacturing via early design/digital twins and AI included:

- Technologies to increase productivity of American workers, lower costs, and address the drastic shortfall of skilled workers
- Industry 4.0 technologies to lead to autonomous smart factories
- True Industry 4.0 built into design from ground up, including AI and digital twins for initial design, construction, and operation of facilities, including systems and equipment
- Standards in data, equipment interfaces, facilities, and tools to reduce facilities cost
- "Smart Manufacturing Experience Center" to simulate production in an interactive environment

Responses related to advanced materials included:

- Energy efficient and green processes for high-performance semiconductor materials
- Advanced materials enabled by in-space production
- Next generation materials, including superconductorsarbon nanotubes, STT magnetic RAM, analog RF transistor technologies, materials for advanced substrates/interposers, and power electronics
- Electro-optical/infrared detectors, materials, and devices

Responses related to metrology and test included:

- Improved, faster, more accurate metrology of processes, such as high performing device and wafer test, measurement, and metrology instrumentation, enabling 1 trillion transistor mixed-node testing
- Packaging and assembly processes that support performance metrology of mixed-die packaging
- Standardization for design-for-test, self-test, and test ports, easily integrated into product design for faster time-to-data and less expensive automated test equipment
- Metrology for new materials for analog RF transistor technologies

Institute Structure and Governance

6. Unique considerations for semiconductor/ microelectronics technology sector

RFI Question 6: Existing Manufacturing USA institutes were launched and operate in alignment with the design principles published in 2013 as the National Network for Manufacturing Innovation: A Preliminary Design (https://www.manufacturingusa.com/reports/national-network-manufacturing-innovation-preliminary-design). Are there any unique considerations for the semiconductor and microelectronics sector that may require modifications to the conventional design for any Manufacturing USA semiconductor institutes under consideration?

RFI Question 6 Response Summary:

Responders generally agreed that the design principles articulated in 2013 are still appropriate, although responders also pointed to other unique considerations for design of Manufacturing USA semiconductor institute(s). Responders agree that the institutes should be sustainable hubs focused on precompetitive manufacturing innovation and should focus on the gap between laboratory capabilities and scalable technologies proven in industrially relevant environments ready for commercialization.

Responders also felt that accessibility to shared infrastructure is critical, even as they expressed different perspectives on whether the infrastructure access should be through a virtual network or centralized physical headquarters with specialized facilities. Responders shared the perspective that the role of the institute is to serve as a hub to link innovation ecosystems for semiconductor manufacturing and should both provide benefit to and learn from various national assets, including other Manufacturing USA institutes and other CHIPS R&D federal investments.

The principle guiding roles for stakeholders were also noted as still relevant. Namely, government should serve as a catalyst to convene the ecosystem around challenges too large for any one entity to solve alone, but should not be the primary sustainer of the ecosystem at maturity. However, several responders noted that the institute may not be fully mature within the initial five-to-seven years envisioned within the design document. Industry members should set the technical direction of the institute to ensure there is a path to scale-up and market support, and that previous failures in R&D that happened within proprietary settings may be considered in determining investments. Academic members can be key to the innovation pipeline and ecosystem by creating and testing new technologies, especially those that would not typically be supported within industry due to less certain ROI.

Responders generally felt that the lead organization for an institute should be an independent non-profit to ensure trust in safeguarding member IP. However, that perspective was not universal, with at least one respondent suggesting that a for-profit entity could make an effective lead for the institute.

Many responders offered additional design considerations for Manufacturing USA semiconductor institute(s) based on unique aspects of the semiconductor sectors. Specifically, the new institute(s) will not need to build a new advanced manufacturing industry around emerging capabilities as there is already a mature global semiconductor industry. Instead, the new institute(s) can focus on increasing the cost-competitiveness of the U.S. industry and leverage existing capabilities and infrastructure. However, given that much of the mature manufacturing expertise is largely overseas, the institutes may need to learn from foreign collaboration and foreign researchers to build U.S. capabilities.

Furthermore, responders noted that the original framework document did not address a few realities of the semiconductor

sector: the various critical stakeholders are already connected through existing collaborations and industry services that must be navigated carefully to establish a unique and compelling value proposition for the new institute(s); and institutes should bring together and work with direct competitors who would otherwise blur the lines of precompetitive research and limit the scope of what could be accomplished through collaboration. At least one responder noted that the design framework emphasis on engaging SMEs may need to be re-examined, as the rapid scale-up capabilities needed for success in this sector are generally only within reach of large industry.

Many responders pointed to the high capital costs and operating expenses for fabrication facilities and suggested that the institute(s) may need to consider alternatives to owning such facilities, including by co-locating new institutes at locations with existing infrastructure or focusing on areas where periodic access to member infrastructure is sufficient. Divergent perspectives among responders were noted on the value of co-located R&D facilities compared to a virtual network of infrastructure that can be shared. However, responders pointed to the Fraunhofer IIS institute in Germany as an example of an accessible state-of-the-art modern fabrication facility to support collaboration that would be useful domestically. Responders were also in agreement that governance structures and leadership within the institute(s) must actively promote member access to any shared facilities to offer real value.

Several responders questioned the impact of potential Manufacturing USA institutes to accelerate innovation for this sector if funded at the typical scale represented by the existing Manufacturing USA model. Responders noted the need for a significantly scaled institute model if the institute is expected to mature technologies from laboratory to industrial readiness and remain relevant as the highly capital-intensive industry evolves. To this point, responders noted that any planning for high-cost facilities or pilot lines should include plans for sustaining and upgrading as technologies and markets evolve.

Responders agreed that it is critical to cultivate collaboration both among the new semiconductor institutes and externally with other Manufacturing USA institutes to speed learning. Responders agreed that any new institutes should not be competitors to existing institutes but should establish relationships that leverage expertise from adjacent industries and multiple manufacturing sectors. Several responders pointed to a need for increased investment in existing Manufacturing USA institutes in relevant spaces to provide resources to engage with and help guide start-up of the new semiconductor institutes to ensure collaborative relationships are in place at launch.

Responders also pointed to a need for robust governance structures for the institutes to provide representation for all stakeholders, given the broad application space for semiconductors and the likelihood that the new institutes will need to serve many different applications and sub-sectors. Responders highlighted that institute leadership and governance should encompass the full spectrum of expertise needed, including business expertise in market drivers, global trends, and transitioning technology, not just technical expertise. Responders also noted that small and medium-sized manufacturers (SMMs) providing innovative advanced components for defense applications need to be integrated into new institutes to encourage U.S. competitiveness and leadership and to sustain the SMMs as they build new industrial base capabilities.

Other considerations that were noted by responders that impact the design principles for Manufacturing USA semiconductor institutes include the need to address

supply chain risks that flow from the current clustering of specialized capabilities in foreign regions. Several responders pointed to the need to ensure some domestic capability for every step of the supply chain, and a role for the proposed institute(s) to create supply chain redundancies. Responders noted that repurposing technologies from adjacent industries could be an effective strategy to meet this need. Responders also noted that close coupling of the NAPMP R&D infrastructure within the proposed institute(s) would promote co-design between chips and packaging technologies.

Another consideration noted by responders is that the intensity of R&D within the semiconductor sector places heavy demands on the innovation ecosystem. Responders suggested that the institute(s) will need to navigate different risk management stances of universities and other stakeholders regarding IP to speed project agreement negotiations.

7. Risks and benefits of "up to three" semiconductor institutes

RFI Question 7: Semiconductor R&D and manufacturing cover substantial technical breadth. What business models or best practices should be employed by a Manufacturing USA semiconductor institute to support U.S. leadership and effectively manage emerging technologies to support commercialization? What advantages or disadvantages would there be to one "super-sized" Manufacturing USA semiconductor institute that would cover the technology sector broadly? Since Congress authorized the NIST Director to establish up to three institutes, what advantages or disadvantages would there be for multiple Manufacturing USA semiconductor institutes each with a smaller scope focused on a specific technology area? How would one Manufacturing USA semiconductor institute or multiple institutes structure relationships with other significant partners to spur collaborative work?

RFI Question 7 Response Summary:

Responders expressed that the institute(s) must be a non-profit, independent facilitator of innovation within its field of specialization. Responders stressed that the new institute(s) should enable collaborative technology maturation, with the focus on technologies, processes, and tools best aligned to facilitate transition to commercial production.

Suggestions for business models and best practices that would support U.S. leadership in emerging semiconductor technology leading to commercialization included:

- Defining avenues for transitioning institute-developed technology such as: (1) direct transfer to member companies, (2) transfer to the NSTC or NAPMP, and (3) hand-offs to a startup to further refine the business case
- Partnering with equipment and services providers, and creating member incentives to share expertise and transfer processes to commercial manufacturing partners
- Adopting the advanced product quality planning framework of procedures and techniques used to develop products in industry and ensure compatibility with Good Manufacturing Practices
- Applying venture capital-style due diligence assessments to investment and adoption readiness levels in addition to technical readiness assessments
- Creating regional centers for specialized one-on-one support to firms of all sizes
- Establishing testing and certification resources for industry firms as fee-for-service capabilities
- Building a multi-faceted business model to include developing cutting-edge innovative technologies for products and services for

manufacturing, addressing supply chain gaps, and providing training initiatives to meet current and future manufacturing needs

- Ensuring balance between government IP rights and needs of industry to meet business drivers for commercialization

In considering the pros and cons of the number and size of semiconductor institute(s), responders were split between the creation of one "super-sized" or multiple institutes. However, there was agreement that the size of a new institute should follow from its technology focus and the degree to which existing infrastructure for that technology area is present within the U.S. or would need to be substantially established. Responders also acknowledged that it is unlikely that a single entity could manage the diversity of manufacturing technology innovation needs for such a broad sector within the available budget. Several responders did favor the single-institute model, citing benefits such as improved decision-making, scalability, lower operational costs, faster time to service, and greater resilience. Those in favor of a single institute also noted the greater ease of managing material compatibility. A few responders suggested that a central hub with regional centers might allow a more cohesive mission and reduce the risk of bifurcating industry members among competing institutes.

Many responders felt that two to three new Manufacturing USA semiconductor institutes with appropriate specialization would have the greatest impact within the existing network, but also pointed to the need to avoid duplication of efforts with each other, and with the NSTC and NAPMP. The responders in favor of multiple institutes noted that creating more than one institute would increase the geographic diversity and would potentially strengthen the ability of the institutes to attract top talent in a more specialized subject matter expertise. Responders also noted that aligning institute(s) scopes with regional assets including existing workforce training may help define scope and result in a higher utilization of tools and facilities. However, responders noted that multiple institutes across geographies would inherently require a degree of duplication of overhead and administrative functions and would make it more difficult to develop a unified mission and culture.

Responders offered general suggestions to create inclusive and collaborative cultures within all established institutes. Some suggested that NIST encourage collaborative projects and ensure that budgets include funding for travel between institutes. Responders also suggested allocating some portion of funding for the new semiconductor institute(s) to existing Manufacturing USA institutes in related technology spaces to support collaboration and knowledge sharing. Responders also suggested that the leadership of each of the NSTC, NAPMP, and Manufacturing USA semiconductor institute(s) should participate in a leadership council to direct and coordinate the activities of each to make them cohesive and avoid duplication.

Responders also suggested potential mechanisms to encourage a diversity of ideas within the institute(s); for example, institutes could host faculty researchers as joint appointments with universities outside the region to increase the reach of the institute(s) and promote partnerships. Responders also suggested rotating institute(s) leadership.

8. Ensuring stakeholder participation

RFI Question 8: What membership and participation structure for a Manufacturing USA semiconductor institute would be most effective for ensuring participation by industry, academia, and other critical stakeholders, particularly with respect to financial and intellectual property obligations, access, and licensing? Based on your knowledge of current Manufacturing

USA institute practices, are the needs of potential semiconductor institutes different than for other institutes?

RFI Question 8 Response Summary:

Most responders agree that the membership and participation structures of a Manufacturing USA semiconductor institute(s) should mirror those of the existing institutes to create a pre-competitive environment that is highly inclusive of the broad ecosystem. Responders agreed that a tiered membership structure with different requirements and benefits is the approach most likely to drive participation. The majority also agreed that the institute(s) should be industry-led and that the leadership should attract members from all sectors and include companies of all sizes. Responders also noted that the institute(s) should include meaningful incentives to attract underrepresented communities, including minorities, women, and veterans. The responders suggested that organized outreach by the new semiconductor institute(s) will help shape new coalitions, academic partnerships, mentor-protégé relations, and durable consortia.

Responders noted the importance of balancing the interests of different stakeholders with different missions in designing membership structures. Ideas suggested include tiered access to IP, project funding opportunities, and licensing rights for institute-developed technology, as well as scaled fee structures and priority access to specialized facilities and equipment. Other ideas include a multi-year commitment and flexibility to allow members to shift from one type of membership to another. Responders agreed that barriers to participation should be kept as low as possible to avoid excluding key stakeholders, but also that active participation in the activities of the institute(s) should be a requirement of membership. Responders suggested the institute(s) create a common base non-disclosure agreement (NDA) for all participants and allow access to a common set of base licenses for domestic process design kits (PDKs) for learning and development. Responders also recommended that membership agreements include clear statements of fees, benefits, timeframes, and IP property policies that promote technology transfer.

One respondent outlined a tiered model for participation where the lowest access would be limited to written information about basic R&D outcomes within an NDA. The next level of access would allow contributions to research projects as well as information on outcomes of key research initiatives. The highest access would allow participation in technology development, with access to facilities and equipment following site-specific training and certification. A few responders suggested that segmenting the work of the institute(s) by technologies for different types of devices could allow containment of confidential information and IP rights within those segments and facilitate the development of pre-defined commercialization plans structured to benefit all.

Multiple responders emphasized the need to share information among the Manufacturing USA semiconductor institute(s), the NAPMP, and NSTC, while also engaging with existing institutes to seek advice and accelerate collaboration and technology transition. Many responders suggested that U.S.-based manufacturers and institutions should have priority access to member benefits, but multiple responders also pointed to the need for participation by international members aligned with U.S. interests.

Strategies for Driving Co-Investment and Engagement

9. Investment Tax Credit for industry

RFI Question 9: The authorizing statute for Manufacturing USA requires at least an equal non-federal co-investment in Manufacturing USA institutes to match

the federal investment. From your perspective, what are the most significant considerations to garner support for the required co-investment for a Manufacturing USA semiconductor institute? What is the anticipated impact of the new Investment Tax Credit (ITC) for industry established in the CHIPS Act on the level of investment in the new Manufacturing USA semiconductor institute(s), in facilities, including for manufacturing equipment and construction? How might a Manufacturing USA semiconductor institute be set up to best leverage the Investment Tax Credit?

RFI Question 9 Response Summary:

Significant considerations to garner industry support for the required co-investment. Responders generally agree that co-investment is important to validate the institute(s) goals and programs. Many responders noted that the existing Manufacturing USA institutes have converged on co-investment models based on three types of co-investments that should work for the new semiconductor institute(s):

- Contribution of funding for institute(s) capital (including facility build-out)
- Investment of industry and academic labor for institute(s) technical leadership (e.g., roadmap development, steering, technical events) and governance
- In-kind cost-share on member projects

Responders generally agreed that a good business plan and co-investment strategy is key to a clear pathway to institute(s) sustainability, significant job creation, and promising technology of strategic value for national priorities. One responder noted that co-investments should not be considered simply financial risk-sharing or measured solely on immediate financial return.

Responders agreed that a co-investment strategy should be structured to encourage and enable a range of inputs (e.g., cash, labor, equipment, facility access), as these contributions reduce the total investment burden on private equity-backed firms and encourage investment. Responders also emphasized that co-investments should come from all groups that participate or receive benefit and mentioned that the strength of co-investment from state and local governments should be considered when considering a site for a new institute. Mechanisms to drive co-investment by venture capital funds were also noted as a potential asset for sustained operations.

Many responders advised against a "one-size-fits-all" approach in recognition of different stakeholder realities. Several responders noted that academic members find it difficult to provide cash cost-share and stressed allowing, instead, in-kind contributions such as use of equipment, tools, and facilities. A few responders suggested rebalancing required co-investment expectations to shift more of the required 50% match to large industry, lessening the match required from pre-revenue SMMs or non-profits. Others suggested that co-investment requirements be linked to the market size of participating companies, and/or the expected economic benefit to the member.

Responders were uncertain about the value of the new ITC. Some responders were skeptical it would encourage industry contributions to the new institute(s), while others believe it will provide incentives for private firm participation. Many responders would like to see the terms broadened to include transitioning costs of moving business from non-U.S. based suppliers to domestic suppliers. A few responders suggested ideas for how the ITC might be leveraged within the Manufacturing USA semiconductor institute(s), including:

- Establishing a commercial entity to support institute(s) activities
- Offering a "co-working manufacturing space" business model that addresses manufacturing readiness from 3 -10

to encourage an entrepreneurial environment and mindset while using different financial metrics than traditional venture capital-based startups and cash flow

10. Factors influencing non-federal co-investment

RFI Question 10: For the required non-federal co-investment for a Manufacturing USA semiconductor institute, with respect to the different types of co-investment (e.g., cash, equipment donations, facilities access, etc.), are there factors unique to the semiconductor industry that would impact how the co-investment could be structured to best support the institute?

RFI Question 10 Response Summary:

Responders differed in their perspectives but generally agreed that the high cost of specialized facilities means that member access to specialized equipment and facilities is a form of cost-share that is useful for many institute(s) partners. Responders also agreed that cash contributions were inherently most flexible and should be encouraged but also noted that co-investment needs will evolve as the institute(s) matures from start-up (estimated to be initial three to five years) to a fully operational state.

Responders pointed to various forms of possible and useful co-investment, including:

- Cash contributions in the form of membership fees
- In-kind time and materials for project support
- Free or discounted electronic photonic design automation licenses to support greater member access to PDKs built on different platforms
- Semiconductor tooling and expertise
- Priority access to multi-product wafer services for domestic companies
- Equipment loans or discounts
- Cleanroom floorspace to demonstrate equipment
- Access to specialized equipment or facilities
- Salary support for institute(s) leaders

Responders agreed that co-investment should be aligned with institute(s) values as well as the resources available to different stakeholders. Several responders noted that not all members (for example, pre-revenue companies and community colleges) can offer cash cost-share. Different stakeholder communities can contribute different types of in-kind cost-share, such as:

- Foundries can provide access to fabrication facilities and commercial equipment
- Equipment manufacturers can provide discounts and equipment loans
- Design companies can provide software and/or design expertise
- Materials developers can provide access to emerging materials in limited volumes
- Large industry can offer R&D resources in support of specific institute(s) projects
- Academics members can lead roadmapping efforts, help with operational costs of convening members, and provide access to specialized instrumentation and equipment for characterizing properties of new materials not typically found within companies

Responders agreed that access to IP was of great value to the community, especially to academics, start-up companies and other SMEs. However, all responders noted that access to IP as cost-share can be problematic and must be navigated with exceptional care.

Responders offered several recommendations for Manufacturing USA semiconductor institute(s) to promote

co-investment, including:

- Development of tiered membership models with different requirements for cash or in-kind contributions, with distinct IP rights for different tiers
- Reduction of cost-share requirements for universities, community colleges, or other non-profit organizations leading or participating in EWD programs, particularly for training programs serving underrepresented minorities
- Building incentives for service providers to give priority for domestic industry needs as a form of cost share

11. Sustaining institute operations in the absence of continued federal support

RFI Question 11: What arrangements for co-investment proportions and types could help a Manufacturing USA semiconductor institute sustain operations in the absence of continued federal support?

RFI Question 11 Response Summary:

Responders commented that this important question does not have a simple or universal answer. Ultimately, sustainability will be an outcome of the positive value proposition for members. Commenters noted that there will be a long lead time before return on investment for industry participation is realized, creating a need for federal support beyond five years. Responders also stressed the importance of securing federal funding for the full award period to attract long-term industry engagement.

Responders pointed to forms of revenue and offsets of operating costs that can be cultivated for long-term sustainability, including:

- Establishing cost-share structures that encourage co-investment to offset operational costs, such as leadership of roadmapping and technology workshops and dedicated personnel for developing and managing institute-led programs
- Developing revenue streams by providing fee-based access to pilot lines and specialized equipment, prototyping services, use of meeting spaces, and assistance with proprietary projects, including transitioning technology at higher TRL/manufacturing readiness level (MRL) into commercialization

Responders also noted that different forms of co-investment to sustain the institute(s) can be provided by leveraging resources appropriate to different types of stakeholders:

- Industry co-investment is likely to sustain the institute(s) through membership fees, in-kind project support, and access to facilities and equipment, provided the collaborative R&D programs remain industrially relevant
- Physical infrastructure and capital costs could be covered by state and local governments to support regional ecosystem development around institute(s) hubs
- Equipment costs can be supported through federal funding (for large capital costs) and/or in-kind contributions from vendors and other industry members
- Salaries of institute(s) leadership can be supported by co-investment from states
- Project-directed federal funding can support R&D aligned with mission needs
- EWD activities such as apprenticeships, paid internships, bootcamps, and online learning resources for underrepresented communities can be supported through funding from non-sponsoring federal agencies

Responders also noted that the scale of the Manufacturing USA semiconductor institute(s) may need to be greater than

is typical for institutes in other sectors, due to the high costs of semiconductor R&D and manufacturing. For example, one responder suggested that an institute focused on advanced packaging might require a federal investment of $250 million per year to have impact on domestic competitiveness. Others noted that although some technology focus areas for a potential institute are less capital intensive, the need for sustained partnerships to provide access to capital-intensive specialized facilities and industrially relevant equipment will be critical.

Risks noted by responders to the long-term value proposition, sustainability, and mission of the institute(s) include:

- Shifting to reliance on foreign support in the absence of continued federal funding
- Straying from a focus on industry needs
- Governance and cost-share structures that do not promote sustained access to high-cost facilities and equipment for academic and SME members
- Uncertainty in the level and timing of federal support to offset costs of non-revenue generating activities of the institute(s) with long timelines, such as those to grow workforce pipelines

Responders noted that many of these risks can be mitigated by having sustained base federal funding for operating costs of convening the institute(s), including outreach to SMEs and EWD activities that support national needs, with private-sector co-investment expected to support technical projects.

Responders highlighted considerations for long-term sustainability and mission success for the Manufacturing USA semiconductor institute(s), including:

- Designing co-investment structures with incentives for industry to prioritize capacity to meet domestic needs
- Being inclusive of the unique needs of a potential workforce-development-focused institute design and sustainability
- Incentivizing different forms of co-investment needed for start-up years versus long-term sustainability phases, including through tiered membership structures that scale member benefits to sustain long-term engagement
- Including development of a sustainable, integrated domestic supply chain to ensure the long-term mission success of the institute(s) and overall CHIPS R&D program

12. Foreign entities

RFI Question 12: A Manufacturing USA semiconductor institute should support domestic competitiveness. How should relationships with foreign entities be structured or constrained to support domestic manufacturing priorities while maximizing the opportunities to leverage international expertise and resources? In what circumstances should the Manufacturing USA Semiconductor institutes and NIST as the federal sponsor consider membership requests from foreign-owned businesses?

RFI Question 12 Response Summary:

Responses to this question were received from Manufacturing USA institutes, academic institutions, societies, and organizations, and companies involved with semiconductors.

The Manufacturing USA institute responses noted expertise outside of the U.S., and advised that collaborations with international partners can be valuable. They also noted that participating in international organizations can provide new insights. However, they indicated that NIST/Manufacturing USA should focus on technology development and IP within the U.S. A few responders also commented that some foreign suppliers are far more

cost-effective than U.S. counterparts, and they would like consideration for their members to use more affordable options. The institutes also submitted that some foreign companies are making large investments in U.S. semiconductor manufacturing, and they should get special consideration in the foreign membership approval process.

Academic institutions were consistent in supporting collaboration with foreign entities noting the need for international supply chains and partnerships. The academic institutions believe that collaborations and partnerships will lead to more technology being developed in the U.S. and growth of the U.S. semiconductor ecosystem.

Societies and organizations echo the call for international collaboration and access to cheaper supplies. Some concerns were raised regarding issues around national security and the need to move beyond dependence on foreign suppliers, but there was a great deal of support for foreign entities that have a strong U.S. manufacturing presence.

Overall, companies that responded were the most in favor of focusing and supporting domestic production and domestic supplies. They were highly supportive of very clear articulation of the need for and contributions by a foreign entity that cannot be addressed by a domestic entity before it could participate in a Manufacturing USA institute's programming.

13. Other federally funded programs

RFI Question 13: How should a new Manufacturing USA semiconductor institute engage other existing Manufacturing USA institutes (**https://www.manufacturingusa.com/institutes**), including those awarded funds for work related to semiconductor manufacturing, and other manufacturing related programs and networks such as the Manufacturing Extension Partnership (**https://www.nist.gov/mep**) and the U.S. Department of Energy's Next Generation Power Electronics National Manufacturing Innovation Institute ("Power America")?

RFI Question 13 Response Summary:

Responders agreed that the new semiconductor institute(s) should formally engage with existing institutes, especially those currently in the semiconductor space, to augment the activities and capabilities of the existing institutes. Responders suggested that the benefits of such engagement would be to learn the best operational framework, identify technology gaps in existing institutes to reduce duplication, optimize new technology development and utilize learnings from successful workforce programs. Furthermore, responders noted that engagement between the up to three new Manufacturing USA semiconductor institutes and existing Manufacturing USA institutes to best coordinate facilities and equipment within multi-institute projects. Responders also stated that institute(s) should have organizational "dotted lines" to NSTC and NAPMP to learn from and contribute to those efforts.

Responders agreed the Manufacturing USA semiconductor institute(s) should develop partnerships with economic development organizations, the MEP and universities to achieve greater outreach to their regional communities, including to SMMs. It was suggested that these relationships and responsibilities should vary based on the stage of the semiconductor value-chain to support technology transition and EWD goals. Responders also recommended that semiconductor institute(s) work with MEPs to assist with SMM adoption of the institute-developed technology via such activities as consulting services and designing support resources to align and support MEP methods and strategies for smart manufacturing adoption in fabrication facilities or back-end lines.

14. Interaction with state and local economic development entities

RFI Question 14: How should a Manufacturing USA semiconductor institute interact with State and local economic development entities?

RFI Question 14 Response Summary:

Within the 28 responses to this question, there was overwhelming support for the Manufacturing USA semiconductor institute(s) to work closely with state and local economic development entities. (One contrary response worried that collaboration with state and local economic development entities could lead to politization of ideas.) Collaboration opportunities that responders indicated were important between state and local entities and the institute(s) ranged from skilled workforce development, access to shared pilot line facilities, business recruitment to the area, job creation, connections with ecosystem partners, and institute(s) funding. Two specific grant programs to leverage were suggested: a homeland security grant program, and a state and local cybersecurity grant program.

Responders suggested that allowing tax credits and state and local funding to be captured as cost-share would incentivize relationships between the institute(s) and state and local economic development entities. One responder suggested an economic development advisory board for the institute(s) to include members from Economic Development Administration-designated districts to ensure broader national reach. The inclusion of economic development entities beyond the regions in which the institute(s) are physically located could create nodes that can scale impacts.

Several examples cited organizations and other members in the ecosystem, including existing semiconductor-related Manufacturing USA institutes such as NextFlex, AIM Photonics, and PowerAmerica, that have built strong connections with state and local economic development partners and already invested in new chip-related factories and production. Responders strongly encourage leveraging these existing connections with the work of the new institute(s). However, responders also noted the tension between driving regional economic impact and serving national needs.

Several responses indicated that an expected outcome of the institute(s) should be creation of highly skilled jobs—either directly at the institute(s) or via partnerships that provide support for start-ups and regional co-location. Furthermore, one respondent indicated that job creation is critical to engaging economic development entities.

15. Standards development bodies

RFI Question 15: How should a Manufacturing USA semiconductor institute coordinate with and inform standards development bodies on the need to modify existing or develop new standards as a result of this initiative?

RFI Question 15 Response Summary:

The overwhelming majority of responders to this question suggested that the Manufacturing USA semiconductor institute(s) should coordinate and inform standards development bodies in three ways: role and coordination, focus areas, and standards organizations and engagement. For role and coordination, there was consensus that the semiconductor institute(s) should play a pivotal role to strategically participate, engage, and convene members particularly from industry to develop and promote standards that reflect technology advances in the semiconductor industry. Responses related to focus areas included design, manufacturing, testing, and packaging standards; equipment compatibility standards; supply chain diversity standards; quality standards; interoperability standard and HI using advanced packaging. Several responses suggested engagement with

standards organizations, namely Joint Electron Device Engineering Council, Institute of Electrical and Electronics Engineers Standards Association, Semiconductor Equipment and Materials International, Telecommunications Industry Association, UCIe, Semiconductor Industry Association, NIST, and International Electrotechnical Commission.

Education and Workforce Development

16. Supporting workforce and awareness at all educational levels

RFI Question 16: How could a Manufacturing USA semiconductor institute best support advanced manufacturing workforce development and/or awareness at all educational levels (e.g., for K-12 through post-graduate students)?

RFI Question 16 Response Summary:

Most responders agreed that the semiconductor institute should invest in and support experiential learning opportunities for all educational levels, from primary and secondary students through to university and postgraduate students. Responders noted that programming must include awareness-building, recruitment, training, and upskilling at technician as well as engineering levels. The majority also stressed that early engagement is critical to build and sustain a pipeline of skilled workers. Responders commented that access to EWD initiatives needs to be strengthened by expanding to other geographical regions and suggested regional hubs for hands-on learning and training on specialized equipment.

Responders also agreed that the institute(s) should partner with state and local educational systems, and academic and industry stakeholders to develop and disseminate industry-relevant curricula targeted at all levels of the pipeline, from K-12 students through postgraduate professional programs. Such programs should provide skill-specific hands-on training and create career interest and pathways for semiconductor manufacturing. Responders emphasized that any new institute(s) must also leverage and complement existing Manufacturing USA institutes' EWD programs and avoid duplication with EWD efforts under adjacent CHIPS Act activities.

Responders offered suggestions for all levels of EWD, including developing outreach programs that tie semiconductor technology to real-world applications, connecting students to industry professionals, and demonstrating the important positive social impact of microelectronics applications. Responders also noted that institute(s) could support efforts to strengthen K-12 math and science standards, build interest in coding and computer architecture, and improve graduation rates to ensure that students stay in the pipeline.

At the post-secondary level, responders suggested that institute(s) work with trade schools and community colleges to increase awareness of semiconductor career paths to develop technician level positions. Several responders suggested engaging college and graduate students directly in semiconductor technical programs to build awareness of potential careers. Aligned programming for internships, recruitment, training, and upskilling for both technician and engineering levels, along with degree programs and certificates across the entire supply chain were also cited as critically important. At the post-graduate level, responders suggested sharing expertise through faculty sabbaticals and joint appointments and cultivating greater access to industry-relevant facilities and equipment.

17. Engaging full diversity of education and vocational training organizations

RFI Question 17: How could a Manufacturing USA semiconductor institute best engage and leverage the diversity of educational and vocational training organizations (e.g., universities, community colleges, trade schools, etc.)?

RFI Question 17 Response Summary:

Most responders agreed that the new semiconductor institute(s) should forge a variety of relationships with educational and training organizations to ensure enough students in the talent pipeline to meet workforce demands. They also advised that the new semiconductor institute(s) should leverage the existing Manufacturing USA EWD network and work closely with the existing institutes in neighboring fields, and with NSTC and NAPMP.

Responders also suggested engagement with universities, trade schools, and community colleges with diverse education and vocational training offerings. Responders offered that these partnerships could lead to co-op and internship programs to recruit junior engineers and technicians into the workforce. Other suggestions included recruiting industry employees to become adjunct professors and instructors, to lead tours, lab activities, and projects complementing coursework. Responders also stressed the importance of updating existing curriculum and expressed support for job placement initiatives that align with industry needs both short- and longer-term. Others noted the value of on-the-job training and advocated for the development of a toolkit addressing certification and career pathways, including those that reach into both rural and urban areas and serve military veterans re-entering the private workforce. Responders also noted that it was important that new institute(s) offer attractive membership rates for EWD partners to lower barriers to participation.

18. Ensuring focus and industry priorities

RFI Question 18: How could a Manufacturing USA semiconductor institute best ensure that advanced manufacturing workforce development activities address the industry's priorities?

RFI Question 18 Response Summary:

The responders stressed that the importance of establishing a strong partnership with industry early to ensure advanced manufacturing workforce development activities that address industry's current and future priorities. Responders suggested that the new institute(s) include in leadership and advisory boards, members representing industry consortia or trade associations that have trusted relationships with small, medium, and large microelectronic companies and a strong understanding of current and expected future workforce challenges and opportunities. Responders also advised regionally aligning workforce development programs with organizations that already have deep EWD penetration in industry.

Responders also stated that workforce development activities should correlate with industry road-mapping activities and must be capable of responding with agility to the changing mix of skills and competencies needed for advanced manufacturing. Specific initiatives suggested included rotating industry professionals into community colleges and universities to teach courses and provide real-world, on-site training opportunities at small, medium, and large businesses via sustainable internship programs.

19. Leveraging existing workforce programs

RFI Question 19: How could a Manufacturing USA semiconductor institute best leverage and complement existing education and workforce development programs?

RFI Question 19 Response Summary:

Responders suggested institute(s) partner with organizations that have access to existing training facilities and resources. Close collaboration with NSF and regional/state programs to leverage existing programs was also suggested, along with assessing all current workforce development programs to identify gaps as well as opportunities for enhancement and support.

Responders also suggested that the institute(s) advocate for sharing proven curriculum, training facilities, and clean rooms to increase access where possible. To meet the shortage of skilled workers, responders suggested development of training programs for incumbent workers with on-the-job training opportunities at institute(s) facilities. Responders offered that graduate degree programs could be co-founded with industry partnerships to increase industrial relevance of the programs and provide strong job placement opportunities for graduates.

20. Success measures

RFI Question 20: What measures could assess Manufacturing USA semiconductor institute performance and impact on education and workforce development?

RFI Question 20 Response Summary:

Responders suggested that the determination of appropriate metrics will largely depend on the specific programs and projects that the institute(s) chooses to implement. Generally, responders agreed that impact metrics should assess successful recruitment and retention of a well-trained and diverse workforce over time. Responders also suggested measures to track the strength and breadth of partnerships among the institute(s) members engaged in EWD initiatives, including:

- Number of internships or apprenticeships funded or catalyzed by the institute(s)
- Regional enrollments in appropriate majors or certificate programs and in high school career and technical education programs, and number of relevant degrees and certificates awarded
- Number of community colleges and universities participating in EWD project calls
- Number of EWD projects funded
- Number of states represented in EWD partnerships
- Number of incumbent workers training through institute-developed programs
- Number of trainees at all levels who transitioned into semiconductor manufacturing jobs
- Diversity statistics on race and gender of participants in institute(s) programs and ultimately in semiconductor careers

21. Integration of R&D with workforce

RFI Question 21: How might a Manufacturing USA semiconductor institute integrate research and development activities and education to best prepare the current and future workforce?

RFI Question 21 Response Summary:

Responders suggested that strengthening industry/academic partnerships while focusing on demonstration of state-of-the-art technology would help integrate R&D with EWD goals. Responders agreed that the voice of industry should be included in developing training programs to ensure that programs developed meet real and evolving needs of industry. Responders also noted the importance of providing students access to industry equipment and instruments, and increasing the industrial relevance of graduate programs.

Responders suggested initiatives such as: developing innovative new graduate curricula better aligned with multiple career paths and team science training; “learn and earn” work-based opportunities; internships and apprenticeships with R&D departments; and other field-based opportunities within small, medium, and large firms where both technical and soft skills can be learned. Responders also noted that inclusion of students from partner organizations on institute(s) R&D project teams would directly integrate R&D and EWD objectives. Specifically, responders cited a need for institutes to work with partners to provide

educational opportunities for full-flow fabrication capacity and for online, AI-based learning and digital twins for training.

Other general comments included a suggestion to partner with local MEP centers for EWD training needs, and a reminder to train students at all levels, including incumbent workers. Responders also emphasized the need for role models and mentoring within inclusive and supportive environments to address, in part, the goal of a more diverse workforce.

22. Building a steady pipeline of skilled workers

RFI Question 22: How could a Manufacturing USA semiconductor institute help build a steady pipeline of skilled workers? What knowledge, skills and abilities will future workers need, and are there workers with those skills currently employed in other sectors?

RFI Question 22 Response Summary:

Respondent suggestions for achieving a steady pipeline of skilled workers can be summarized by one particular response: "1) quantify the needs [of industry], 2) minimize attrition, 3) reskill adjacent workforces, 4) grow the talent pipeline (students), and 5) [promote] diversity, equity, and inclusion." Many responders emphasized that outreach to K-12 was important to capture and retain young talent for the future workforce. Responders agreed that strong partnerships with federal, industry, non-profit, and academic stakeholders are needed to develop specific K-12 and post-secondary educational training programs. Credentialing, hands-on learning in facilities, internships, online learning, and non-traditional training were all provided as examples to train the future skilled workforce.

Responders listed a diverse set of professional and multidisciplinary technical knowledge, skills, and abilities needed to revitalize the nation's semiconductor manufacturing and noted that these skills are currently held by workers in several different manufacturing and STEM fields, including automotive, aerospace, and transportation.

Specifically, responders suggested many possible approaches to build a steady pipeline of skilled workers, including:

- Complement and expand existing initiatives and programs that focus on knowledge, skills, and abilities determination and adoption, as well as programs designed to reskill and upskill the current workforce
- Provide outreach, image, and awareness campaigns for the general public and K-12 to demystify microelectronics and dispel outdated impressions of the industry
- Establish veteran-focused programs that help transitioning military members find careers in the industry
- Provide AR and VR online tools and portals to help students and adults of all backgrounds find educational pathways and careers in the industry
- Establish "rotational internship programs" for students to spend time in various industries during college

Responders provided the following suggestions for knowledge, skills, and abilities future workers will need: PDK and EDA tool coding, power and control systems, computer science, electrical engineering, Python, debugging, semiconductors, supply chain, new product development, automation, 3D printing, MEMS, nanotechnology, machine learning, Six Sigma quality-control expertise, robotics, systems knowledge, digital engineering, cybersecurity, networks and data capabilities, critical thinking, problem-solving, operations knowledge, and collaboration skills.

Responders also suggested that workers in sectors such as construction, automotive and auto repair, transportation, power generation and renewables, and other

manufacturing industries could be trained and transitioned to semiconductor manufacturing, and pointed to veterans and returning service members as a talent pool as well.

23. Broadening the talent base

RFI Question 23: How could a Manufacturing USA semiconductor institute broaden the talent base (i.e., embrace diversity, equity, inclusion, and accessibility; reach women and minority communities, engage non-traditional workers, engage separating service members, veterans, and families) to modernize the workforce?

RFI Question 23 Response Summary:

The majority of responders agreed that the new institute(s) should work with industry to ensure that a broad talent base is captured, and all community groups, including those that have been under represented, are empowered and given the opportunity for successful careers. Many responders mentioned the importance of not only partnering and engaging with community, professional, and affinity organizations, including those that have been underrepresented in semiconductor manufacturing, but also ensuring that workplace cultures are welcoming and all individuals feel valued. Included among those organizations mentioned were historically Black colleges and universities, Hispanic serving institutions, and other minority-focused educational institutions as well as community-based organizations, faith-based organizations, labor representatives, and other local workforce agencies. Responders also noted that it was important to reach underserved and rural communities to reach untapped talent, and to provide training programs focused on veterans and women. Responders emphasized that outreach activities should be specifically tailored to each community group, and that it was important that activities and events are planned and scheduled where the communities currently exist. Responders also noted the importance of coordinating outreach and leveraging investments within NSTC and NAPMP, the existing Manufacturing USA institutes and other federal programs, and with established educational and vocational training organizations for greatest impact.

Additional suggestions to broaden the talent base included the following :

- Organize field trips and expose educators to new opportunities for instructional resources
- Provide subject matter experts to engage in inspirational talks at high schools, trade schools, or job fairs
- Provide on-site child care (including before/after school care for K-12 students) and out-of-school family learning experiences, and utilize community hubs and centers that introduce youth and families to both emergent technologies and potential careers in semiconductor manufacturing
- Organize a diversity, equity, inclusion, and accessibility (DEIA) board for each institute that consists of local and national leadership not only in semiconductors but also in community building and DEIA success

24. Education and workforce development mechanisms

RFI Question 24: What type of education and workforce development activities should a Manufacturing USA semiconductor institute support (e.g., curricula, online education, hybrid, entrepreneurship opportunities, credentialing, regional development, train the trainers, internships/apprenticeship, learning labs, etc.) and why?

RFI Question 24 Response Summary:

Most responders agreed that partnerships with other government, academic, and private organizations will help expand outreach, accessibility, and impact of the suggested EWD activities. Such partnerships

were also considered important to avoid duplication, address gaps, and ensure that the institute(s) efforts complement other initiatives. Some responders noted that the new semiconductor institute(s) should start EWD activities by collaborating with existing Manufacturing USA institutes that have demonstrated success in adjacent industries.

The responders proposed several different types of EWD activities to target specific audiences and provide different training functions. Responders also mentioned the importance of diversity, equity, and inclusion in the education and workforce training activities. Overall, responders noted the proposed activities should be tailored to support clear and successful career pathways.

Responders noted the following as impactful opportunities in EWD:

- Hybrid curricula that emphasize virtual training and digital twins for fabrication equipment systems and operations to aid training enhancement in a field setting
- Hands-on engagement opportunities through apprenticeships, internships, and experiential learning programs
- Mobile learning labs that can rotationally visit schools, colleges, and universities across the nation
- Job outlook pathways, encompassing flexible modalities of certifications and credentialing, including technical webinars, tutorials, and short courses
- Streamlined mentor training and "train-the-trainer" programs
- Entrepreneurship training sessions, such as how to write a business plan

Responders mentioned the institute(s) can provide educational capstone programs and senior design programs in higher education to mirror R&D initiatives without the high cost of permanent employee work for similar industry-driven programs, thereby leveraging students to carry out research.

Responders noted that direct company involvement in these types of initiatives results in research that can lead to patents, products enhancement, and testing that may one day become standard production while also generating a pipeline of students into the industry. Another suggested avenue is to train high school teachers to increase awareness in students about opportunities and subjects that exist in the semiconductor industry.

Metrics and Success

25. Sector-specific economic competitiveness, national security, technology innovation

RFI Question 25: What metrics could be used to best evaluate the performance of a Manufacturing USA semiconductor institute in accelerating innovation, and any associated impacts on economic competitiveness and national security? Are there sector-specific metrics for an institute in the semiconductor technology space?

RFI Question 25 Response Summary:

There was consensus among the responders on the need for clear metrics for a comprehensive view of the overall U.S. semiconductor manufacturing ecosystem. Several suggestions mentioned aligning metrics with the institute(s) operational and technical progress, innovation, economic competitiveness, and national security. Other responses suggested sector-specific metrics listed below.

Responses related to operational progress included metrics such as:

- Number of member organizations
- Participation from all segments of the ecosystem
- Financial performance metrics
- Number of projects transferred to the industry for scale-up

- Number of employees, internships, hosted people employed by other organizations
- Turnaround time required for manufacturing prototypes and production

Responses related to technical progress included metrics such as:

- Publications, patents, presentations
- Participation in conference and standards committees
- Talent development indicators, such as students graduating from academic programs associated with the institute(s)
- Number of students entering the semiconductor industry
- Defined TRL and MRL ladders for short to mid-term progress by the institute(s)

Responses related to accelerating innovation included metrics such as:

- Number of patents, start-ups, or the amount of venture capital or private investments made
- Number of citations of Manufacturing USA institute(s) projects by researchers
- Number of R&D projects funded per year
- Number of schools and students engaged in a workforce development program
- Qualitative metrics, feedback, continuous improvement, member surveys

Responses related to economic competitiveness impacts included metrics such as:

- Fill rate for manufacturing jobs in local communities
- Manufacturing yield and capacity resulting in cost and performance improvements
- Gross domestic product attributed to the semiconductor industry, international trade exports, international trade imports
- Number of commercial companies bidding or participating in R&D projects both coinvested and federally funded
- Supplier diversity index applied to various tiers within the supply chain

Responses related to national security impacts included metrics such as:

- Number of projects leveraging commercial capabilities
- Technologies developed that measurably impact the aerospace/defense
- Workforce training

Responses related to sector-specific metrics included the following:

- Decreased imports of foreign components, raw materials, and services
- Increased visibility and revenues for women and minority-owned businesses
- Share of the international market in selected semiconductor products
- Number of users/subscribers to the institute(s)

26. Semiconductor institute specific education and workforce development

RFI Question 26: What type of metrics could be used to best evaluate the performance and impact of a Manufacturing USA semiconductor institute on education and workforce development in support of U.S. competitiveness?

RFI Question 26 Response Summary:

Responders suggested that impact needs to be measured across the entire supply chain from component production to finished products for manufacturers

involved in the institute(s). Related metrics potentially include time-to-train workers and achieve proficiency, productivity, training effectiveness, number of internships and number of community colleges and universities participating in project calls, technician/trade certificates awarded, degrees awarded, regional expansion of training centers/trade schools as well as higher education offering new semiconductor/microelectronics related curricula and number of hires by the semiconductor industry and its supporting ecosystem.

27. Semiconductor manufacturing ecosystem development

RFI Question 27: What type of metrics could be used to best evaluate the performance and impact of a Manufacturing USA semiconductor institute in establishing and expanding the U.S. semiconductor manufacturing ecosystem?

RFI Question 27 Response Summary:

Responders generally favored impact metrics measured by commercial activities such as the number of start-ups in the institute(s) field, jobs added per year in the related industrial sector, number of new products introduced with semiconductor technology, sales volume related to technology development facilitated by the institute(s), patents and patent-protected sales for technology generated by the institute(s), commercial viability and institute(s) facilitated deployment of technologies, and expansion of domestic manufacturing capacity.

Several responders also suggested technology-specific performance metrics such as manufacturing output trends, wafers per month, and number of new chip fabrication facilities built that use advanced substrates developed and used at the new institute(s). For broader impact, responders suggested surveying semiconductor companies and members of the institute(s) while simultaneously considering other global semiconductor institution metrics to best evaluate performance and impact in establishing and expanding the ecosystem related to knowledge transfer, collaboration, pipeline and job creation, safety, quality, delivery, and growth metrics.

Responses related to impact metrics measured by commercial activities included the following:

- Project partnering arrangements between members and outsiders
- Jobs added per year in the related industrial sector and sales volume related to the technology development facilitated by the institute(s)
- Granted patents and patent-protected sales for technology generated by the institute(s)
- Revenue generated through licenses
- Business incubators for a given region
- End product performance versus cost compared to existing manufactured products
- Expansion of domestic manufacturing capacity and expansion of supply chain robustness

Responses related to technology-specific tracking metrics included the following:

- Manufacturing output trends, such as wafers per month
- Number of new chip fabrication facilities built that use advanced substrates developed and used at the new institute(s)
- Number of users that pay the institute(s) for manufacturing services and/or shared manufacturing/office space

Responses suggesting related institute-level metrics included the following:

- Successful and timely meeting of promised technical project deliverables
- Number of publications in peer-

reviewed journals and leading conferences
- Number of PhD students engaged
- Number and value of industry contracts, patents, and creation of spin-off companies
- Prototypes fabricated, standards and road mapping activities
- New member sign-up rates and renewal rates

28. First-year considerations

RFI Question 28: What constitutes a successful first year for a Manufacturing USA semiconductor institute? What forms of support, and from which partners, are needed to ensure a successful first year?

RFI Question 28 Response Summary:

Several responders provided input on year-one success metrics such as: institute(s) bylaws established with initial member participation, paid company membership dues that represents at least a 50% market share in the markets the institute(s) aims to influence, second year dues payments received from at least 90% of first-year members, signed commitment of state funding for more than five years, institute(s) value proposition defined with significant member contributions, and significant member contributions to technology roadmap, business plan, and budget.

The responses on the forms of support included the following:

- Support from NIST, the NAPMP, and NSTC and partnership with existing institutes are needed to ensure success
- Work with the federal government and private sector investor to ensure all funding is available prior to "work start"
- In-kind contributions from the institute(s) users
- Buy-in from major companies, which includes significant financial contribution as well as active technical participation in programs

Responders also suggested key considerations while setting up the new institute(s) such as defining clear scope and mission, capitalizing on existing industry and public and private partnerships, and finalizing key institute(s) documents. Other key considerations while setting up the new institute(s) included the following:

- Build the core team by putting in place key management and staff positions
- Define an operating budget and secure sufficient funding
- Develop infrastructure including finance, information technology, facilities, program plans, etc.
- Determine targeted industry partners and critical members and get early letters of commitment and support
- Paths to participate in project calls and programs defined
- Develop initial project, prototypes, and technical plans

Responders suggested establishing clear governance and interactions with NSTC and NAPMP and partnership with existing institutes. Other suggestions called for development of a strategic plan and framework to achieve the plan supported by Manufacturing USA, the Department of Commerce, and the broader federal government, as well as state and local agencies.

V. APPENDIX A - ACRONYMS

3D - three-dimensional

3DHI - 3D heterogeneous integration

AI - artificial intelligence

AR- augmented reality

VR - virtual reality

CHIPS Act - Creating Helpful Incentives to Produce Semiconductors for America Act

CMOS - complementary metal-oxide-semiconductor

DEIA - diversity, equity, inclusion, and accessibility

DOD - Department of Defense

EDA - electronic design automation

EWD - education and workforce development

HI – heterogeneous integration

IP - intellectual property

ITC - investment tax credit

K-12 - kindergarten to 12th grade

MEMS - micro electro-mechanical systems

MEP - Manufacturing Extension Partnership

NAPMP - National Advanced Packaging Manufacturing Program

NDA - non-disclosure agreement

NIST - National Institute of Standards and Technology

NSF - National Science Foundation

NSTC - National Semiconductor Technology Center

PDKs - process design kits

R&D - research and development

RF - radio frequency

RFI - request for information

ROI - return on investment

SMEs - small-to-medium enterprises

SMMs - small and medium-sized manufacturers

STEM - science, technology, engineering and mathematics

TRL - technology readiness level

MRL - manufacturing readiness level

UCIe - Universal Chiplet Interconnect Express

CITATIONS

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[5] The authorizing statute for Manufacturing USA requires at least an equal non-federal co-investment in Manufacturing USA institutes to match the federal investment as specified in 15 U.S.C. 278s(e).

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[11] https://www.commerce.gov/news/blog/2022/01/results-semiconductor-supply-chain-request-information

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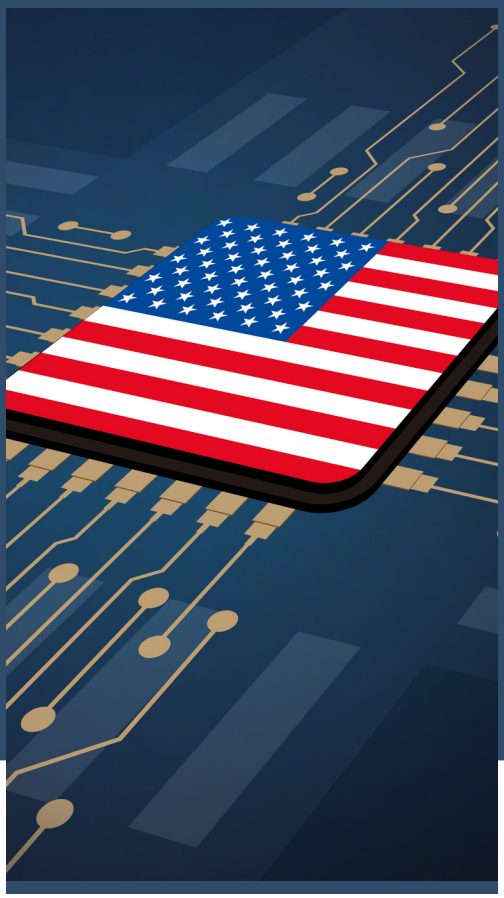

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