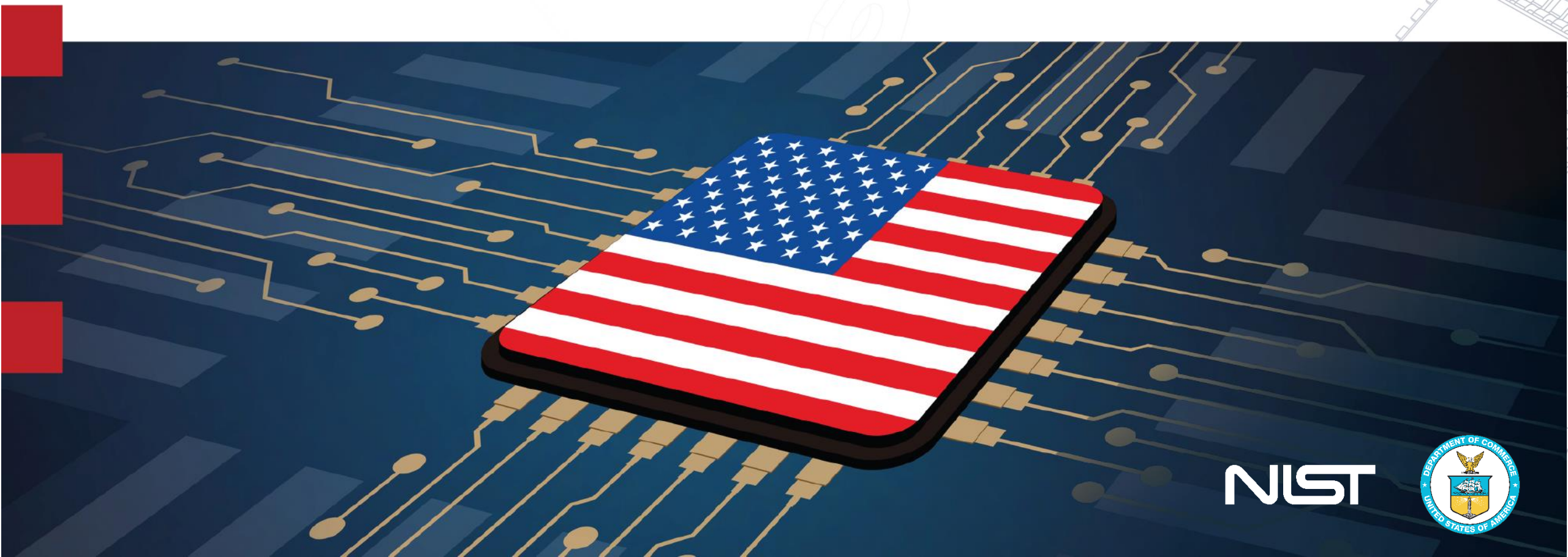
CHIPS R&D Update

December 8, 2022



Eric Lin

Interim Director

CHIPS Research and Development Office

CHIPS for America Vision

Economic Security

This act enables us to build more resilient supply chains for important components.

National Security

This act enables us to bring the most sophisticated technologies back to the U.S.

Future Innovation

Chips are key to the technologies and industries of the future, so we need to be at the forefront. This act will ensure long-term U.S. leadership in the sector.

CHIPS for America Incentives

$39 billion for manufacturing

- Incentivize expansion of manufacturing capacity for semiconductors
- Attract large-scale investments in advanced technologies such as leading-edge logic and memory
- Advance U.S. technical leadership
- NDAA Section 9902

$11 billion for R&D

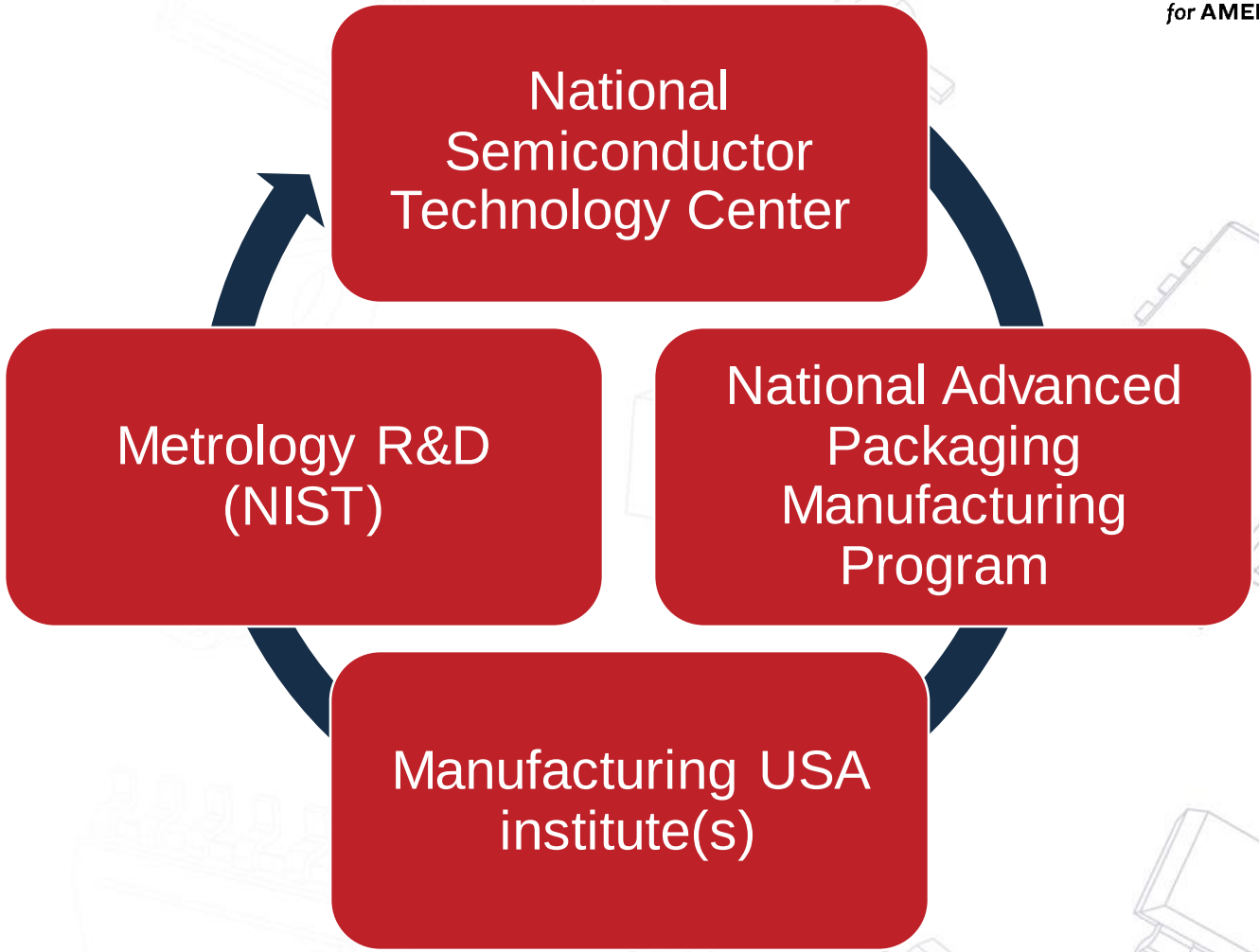
- National Semiconductor Technology Center
- National Advanced Packaging Manufacturing Program
- Manufacturing USA institute(s)
- National Institute of Standards and Technology measurement science
- NDAA Section 9906

Workforce development

Together with CHIPS initiatives from other agencies, including DOD, State, NSF, and Treasury

Research & Development

- Strengthen and advance U.S. leadership in R&D
- An integrated ecosystem that drives innovation
- In partnership with industry, academia, government, and allies
- A strategic view of R&D infrastructure, participant value-proposition, and technology focus areas
- Informed by the Industrial Advisory Committee



Engagement and Outreach

- Automotive
- Consumer products
- Defense and Aerospace
- Design
- Equipment vendors
- Fabless/Fablite
- Foundries
- Heterogenous Integration
- IDMs
- Materials suppliers
- System partners

AIM Photonics
Ansys
Applied Materials
Arizona Commerce Authority
Beltronics
Brewer Science
Bridg
Bruker
Cadence Design
Clark St. Associates
Corning
DARPA
Department of Energy
EMIR
Environmental Protection Agency
Femtometrix
Global Foundries
Google
HDR Architecture
Heterogeneous Integration Roadmap
HRL Labs
IBM
IEEE
Illumina
IMEC
IMMCO
INEMI
Integra Technologies
Intel
IPC
IRDS
ITB Group
ITI
Keysight
KLA
Lam Research
Micron
Mitre Engenuity
MTSI
NASA
NDIA
Northrop Grumman
Nova
NXP Semiconductors
NY Creates
Onto Innovation
Oxford Instruments
Perkin Elmer
Process Engineer
PSI Quantum
Qualcomm
Rigaku
SAE International
SEMI
SK hynix
Skywater Technology
Semiconductor Research Corporation
SPIE
Synopsys
TEL
Teledyne Technologies
Texas Instruments
Thermo Fisher
TTCA
UCLA
University of Florida
XCeleprint
xLight

Engagement and Outreach

Two semiconductor metrology-focused workshops, April 2022

Individual companies registered:	134+
Workshop #1 total registrants:	507+
Workshop #2 total registrants:	465+

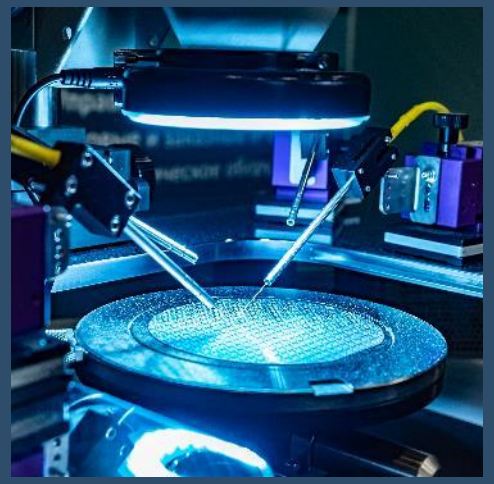
Breakout session representation:

Workshop #1

Sector	Number	%
Industry	91	63%
Academia	28	19%
Government	25	17%
Total	145	

Workshop #2

Sector	Number	%
Industry	81	55%
Academia	30	21%
Government	35	24%
Total	146	



National Semiconductor Technology Center

Vision: Will serve as the **focal point** for research and engineering throughout the semiconductor ecosystem, advancing and enabling disruptive innovation to provide U.S. leadership in the industries of the future.

Structure: A public-private consortium, as an independent entity with a governing board informed and advised by industry, academia, government, and key stakeholders.

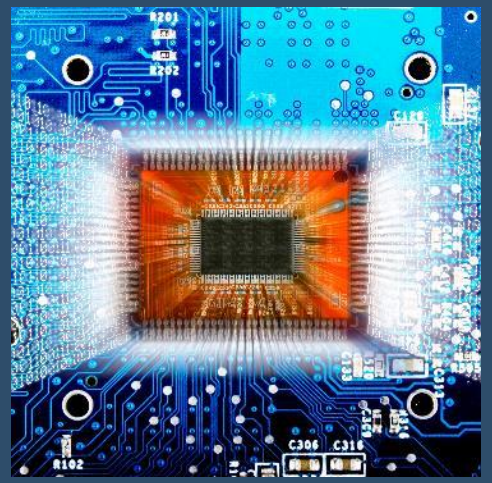
National Semiconductor Technology Center

Elements:

- Core of centrally operated, in-house research, engineering, and program capabilities combined with a network of directly funded and affiliated entities.
- Includes applied research, prototyping of devices and processes in a real-world environment, challenges related to scaling, start-up company support, or development of advanced manufacturing tools and processes.
- Focus research and engineering on challenging projects with a time horizon beyond 5 years.
- The NSTC will serve as a key convening body for the ecosystem.

Process:

- NSTC white paper, 1st quarter 2023.
- Summarize the results of a landscape analysis, outline a governance structure, and describe a preliminary operating and financial model.



National Advanced Packaging Manufacturing Program

- To strengthen semiconductor advanced test, assembly, and packaging capability in the domestic ecosystem
- Leverage public-private partnerships, including the NSTC and Mfg USA
- Technologies could include:
  - Heterogeneous integration
  - Wafer and panel-based approaches
  - Tooling and automation
  - Substrate technology

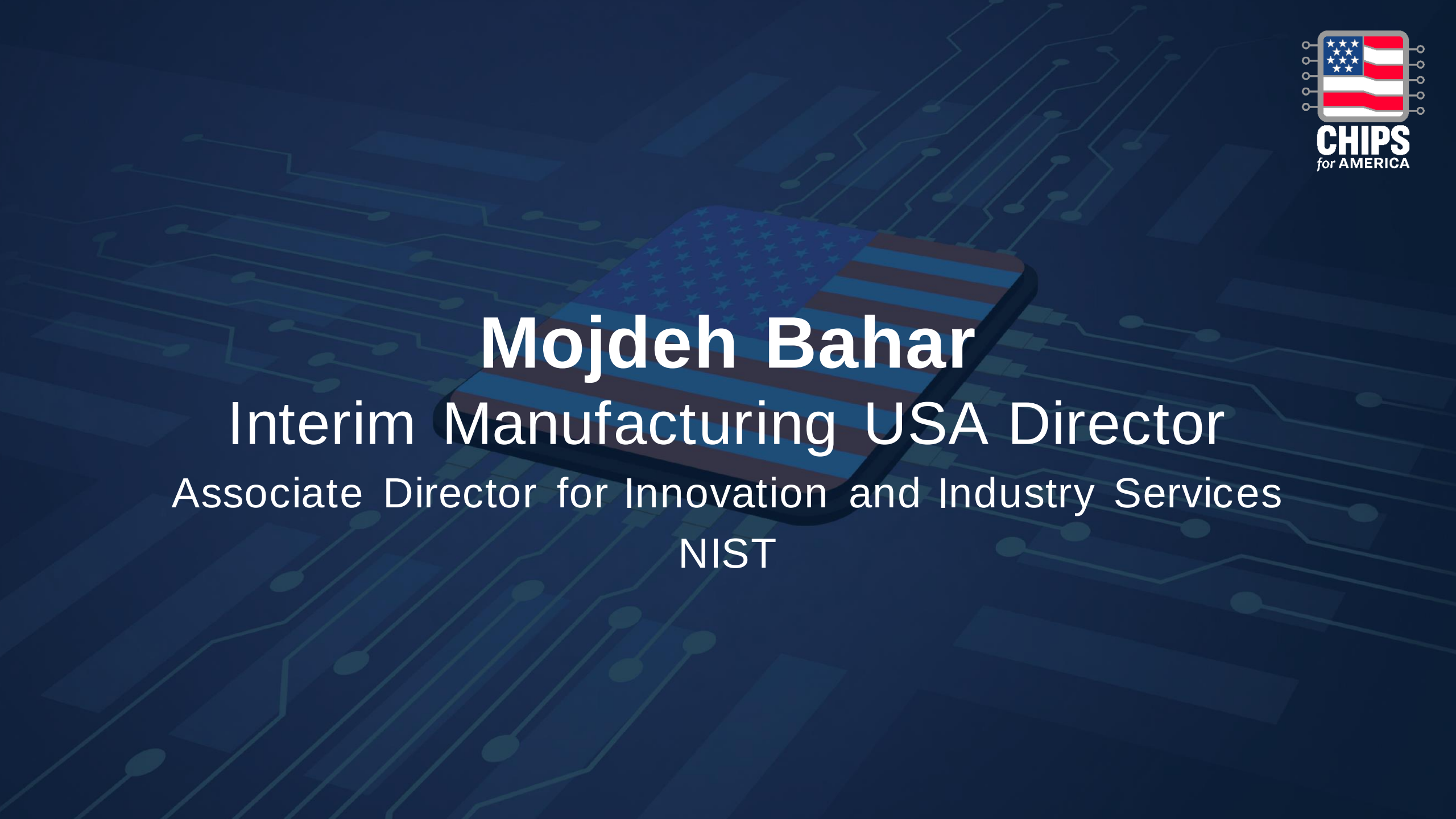
National Advanced Packaging Manufacturing Program

Technology Areas

Co-Design	Chiplets	Heterogenous Integration	Design	Platforms	Advanced Tooling	Materials and Substrates
• Co-design • Simulation • Validation	• Design • Simulation • Validation • Chiplet standards • IP	• Pilot and integration Line(s) • High density interconnects • Materials Systems • Etc.	• Simulation • Validation • PDKs • ADKs • IP	• Flip-Chip • 2D, 2.5D, • 3D Stacking • Fan-Out • Fan-In • System in Package (SiP) • Interposer • Etc.	• Automation • Dicing • Bonding • Integrated Assembly • Metrology and Inspection	• Glass • Ceramics • Substrates • Interposers • PCB • Etc.

Approach

- Identify areas of focus and services needed to build domestic capacity for key areas
- Identify opportunities to strengthen alignment of key areas with facilities, partnerships, and program integration



Mojdeh Bahar

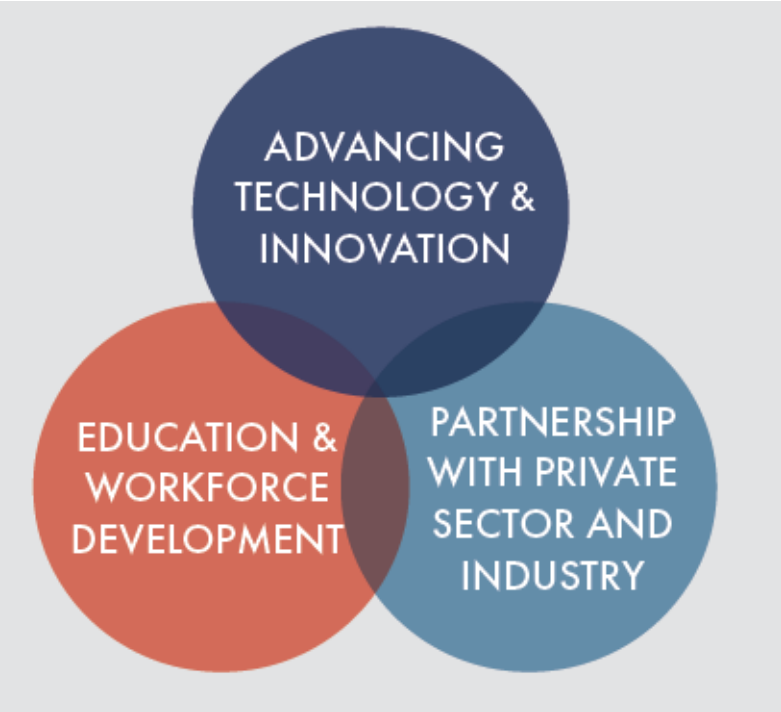
Interim Manufacturing USA Director

Associate Director for Innovation and Industry Services

NIST

Manufacturing USA Program Design

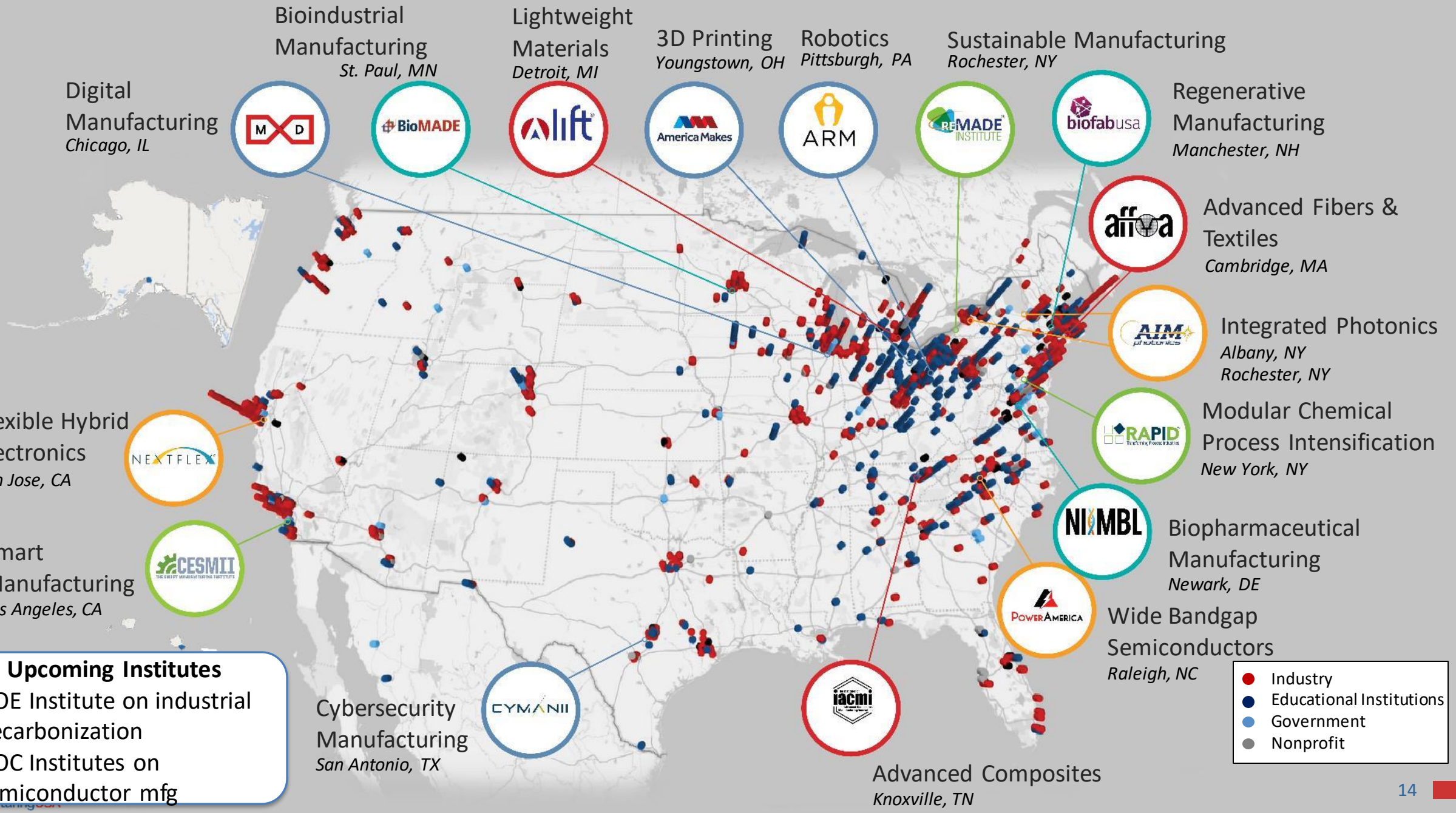
Mission: "Connecting people, ideas, and technology to solve industry-relevant advanced manufacturing challenges, thereby enhancing industrial competitiveness and economic growth, and strengthening our national security."



Four goals:

1. Increase the competitiveness of U.S. manufacturing;
2. Facilitate the transition of innovative technologies into scalable, cost-effective, and high-performing domestic manufacturing capabilities;
3. Accelerate the development of an advanced manufacturing workforce;
4. Support business models that help the institutes become stable and sustainable.

Manufacturing USA Institute Network



Upcoming Institutes

- DOE Institute on industrial decarbonization
- DOC Institutes on semiconductor mfg

Manufacturing USA 2021 Impacts

16 institutes with **2,320** member organizations partnering on grand challenges

708 major collaborative technology and workforce R&D projects

63% of members are from industry and **72%** are small

$127M in federal program funds attracts **$354M** in state, private, and pandemic funds

Over 90,000 people trained in advanced manufacturing

Roadmaps and White Papers

MfgTech Microelectronics Roadmaps

MfgTech Roadmaps bring together manufacturers, universities, industrial organizations and other stakeholders into consortia that identify barriers to advancing new manufacturing technologies.

Title	Recipient
Manufacturing Roadmap for Heterogeneous Integration and Electronics Packaging	The Regents of the University of California, Los Angeles
Microelectronic and Advanced Packaging Technology (MAPT)	Semiconductor Research Corporation
5G/6G mmWave Materials and Electrical Test Technology	International Electronics Manufacturing Initiative, Inc.
Industrial Artificial Intelligence Consortium to Advance High Mix Production	University of Cincinnati

White Papers

Internal white papers have provided planning on the National Advanced Packaging Program, Education and Workforce Development, and International Benchmarking of International Innovation Programs

Request for Information (RFI)

- Responses to this RFI will inform NIST's development of funding opportunities for federal assistance to establish Manufacturing USA semiconductor institutes.
  - RFI Published October 13, 2022
  - Three public informational webinars held on October 20, November 2, and November 16, 2022.
  - Public comment period extended until December 12th.
  - 57 comments received to date.
- A summary of the public input is expected to be available in early February 2023.

https://www.federalregister.gov/documents/2022/10/13/2022-22221/manufacturing-usa-semiconductor-institutes

James Olthoff

Interim Metrology Director

Associate Director for Laboratory Programs

NIST

Overview: CHIPS ACT + NIST Metrology

SECTION 9906 (e) - MICROELECTRONICS RESEARCH AT NIST

The Director of the National Institute of Standards and Technology shall carry out a microelectronics research program

*to **enable advances and breakthroughs** in measurement science, standards, material characterization, instrumentation, testing, and manufacturing capabilities*

*that will **accelerate** the underlying research and development for **metrology of next-generation microelectronics***

*and **ensure the competitiveness and leadership of the United States** within this sector.*

CHIPS METROLOGY PROGRAM AREAS

Focus areas from Grand Challenges

Broad-based awards and partnerships

Workforce

Instruments and facilities

Focused Stakeholder Input to Focus Areas

- Two semiconductor metrology focused workshops, April 2022
- On September 1, 2022, NIST released a report outlining seven strategic **Grand Challenges** in measurement, standardization, and modeling, and simulation that, if met, will strengthen the U.S. semiconductor industry.

https://nvlpubs.nist.gov/nistpubs/CHIPS/NIST.CHIPS.1000.pdf

Metrology Grand Challenges

1. Metrology for materials purity and properties
2. Future microelectronics manufacturing
3. Advanced packaging
4. Security of devices across the supply chain
5. Modeling and simulating semiconductor materials, designs and components
6. Improve the manufacturing process
7. Standardize new materials, processes and equipment

Programmatic Focus Areas

Example grand challenge path forward elements in published report (green bullets below)

The challenge: Provide enabling metrology that spans multiple length scales and physical properties and supports acceleration of advanced packaging concepts for future-generation microelectronics.

The strategy: Develop metrology to enable complex integration of sophisticated components and novel materials for advanced microelectronics, strengthening the domestic semiconductor packaging industry and U.S. leadership in this critical sector.

The path forward: Conduct R&D to develop metrology to address the unique challenges presented by advanced packaging, including subsurface features and aspects related to heterogeneous integration and other innovative concepts. Critical areas include:

- Measurements for in situ, rapid measurements and verification methods for interfaces and subsurface interconnects, and internal 3D structures including warpage, voids, substrate yield, stresses, adhesion, and reliability with improved throughput and resolution.
- Physical properties (e.g., size, thermal, mechanical, electrical, magnetic, optical) for films, surfaces, buried features, and interfaces.
- Methods for integrating chiplets, dielets, SoCs, and memories into packages.
- Mechanical measurements for component integration (e.g., hybrid bonding and interfacial adhesion and bond integrity).
- Evaluation and correlation of data across the packaging process.
- Standards for packaging, such as reference materials and documentary standards for areas including chiplets and SoCs.

- Total of 7 grand challenges and **32 path forward elements** in published report
- Consolidated 32 path forward elements into **20 programmatic focus areas**
- The 20 programmatic focus areas **capture the full technical scope and content** of the 32 published path forward elements

Focus Areas

Initial needs of the semiconductor industry to be considered by the CHIPS Metrology R&D Program

Cluster 1:

- Advanced metrology for supply chain trust and assurance
- Verification and validation of advanced models
- Advanced modeling for next-generation manufacturing processes
- Standards for automation, virtualization, and security
- Interoperability standards for equipment and software

Cluster 2:

- Metrology for advanced materials and devices
- Metrology for nanostructured materials characterization
- Advanced measurement services
- Advanced metrology for 3D structures and devices
- Materials characterization metrology for advanced packaging

Eric Lin

Interim Director

CHIPS Research and Development Office

International Coordination

- We are engaged with similarly-oriented, partner nations
- Strong alignment on the value of partnership in R&D
- Identifying effective leverage points, mechanisms, and specific program areas
- In parallel with discussions around supply chain, guardrails, and other topics

Interagency Coordination

The impact of the CHIPS R&D program is maximized when integrated with programs across the USG.

We are working closely with DOD, NSF, DOE, and other agencies to realize this integration with guidance and support from the White House and OSTP.

DOC Programs	DOD Microelectronic Commons
Support growth of domestic capacity, capability for US commercial market	Ensure that growth supports, and takes advantage of, national defense technologies
CHIPS for America R&D	**Regional Hubs**
• NSTC - Supports the future market for, leading edge, heterogeneous integration, non-CMOS • NAPMP – Supports the future market for heterogeneous integration, advanced packaging • Mfg USA, NIST Metrology - Support the industry with manufacturing solutions and characterization methods	• Distributed network of technology-focused hubs that build on regional strengths • Support prototyping, leverage unique capabilities • Guided by national defense needs, projects proposed by hubs foster the best solutions
Incentives	**Cores**
Expanded capability and capacity to support high TRL / MRL development • High-TRL prototyping • Pilot, manufacturing processes • Test and assembly	• Commercial fabs and foundries • Mid-TRL prototyping, pilot, test and assembly through Commons • High TRL production and commercialization for DIB, services & others

Shared resources, network access, coordination, and planning

Alignment Timeframes

Interagency | DOD – DOC Alignment (in a dynamic ecosystem)

Hypothetical scenario – Large auto manufacturer to build sensor for autonomous driving, adding chiplets to existing 3D platform from Commons

Automotive Company
Technology Developer

NSTC
Primary Shepherd
Provides support for EDA, early stage prototyping, FEOL, BEOL prototyping and assembly, testing, coordinates with Commons, NAPMP, DARPA ERI 2.0

Commons
Proven Technology - Coordinated Access
3D platform taped out

NAPMP
Unique Technology - Coordinated Access
Chiplet library

NAPMP
Access to Process - Standard Handoff
Advanced Packaging

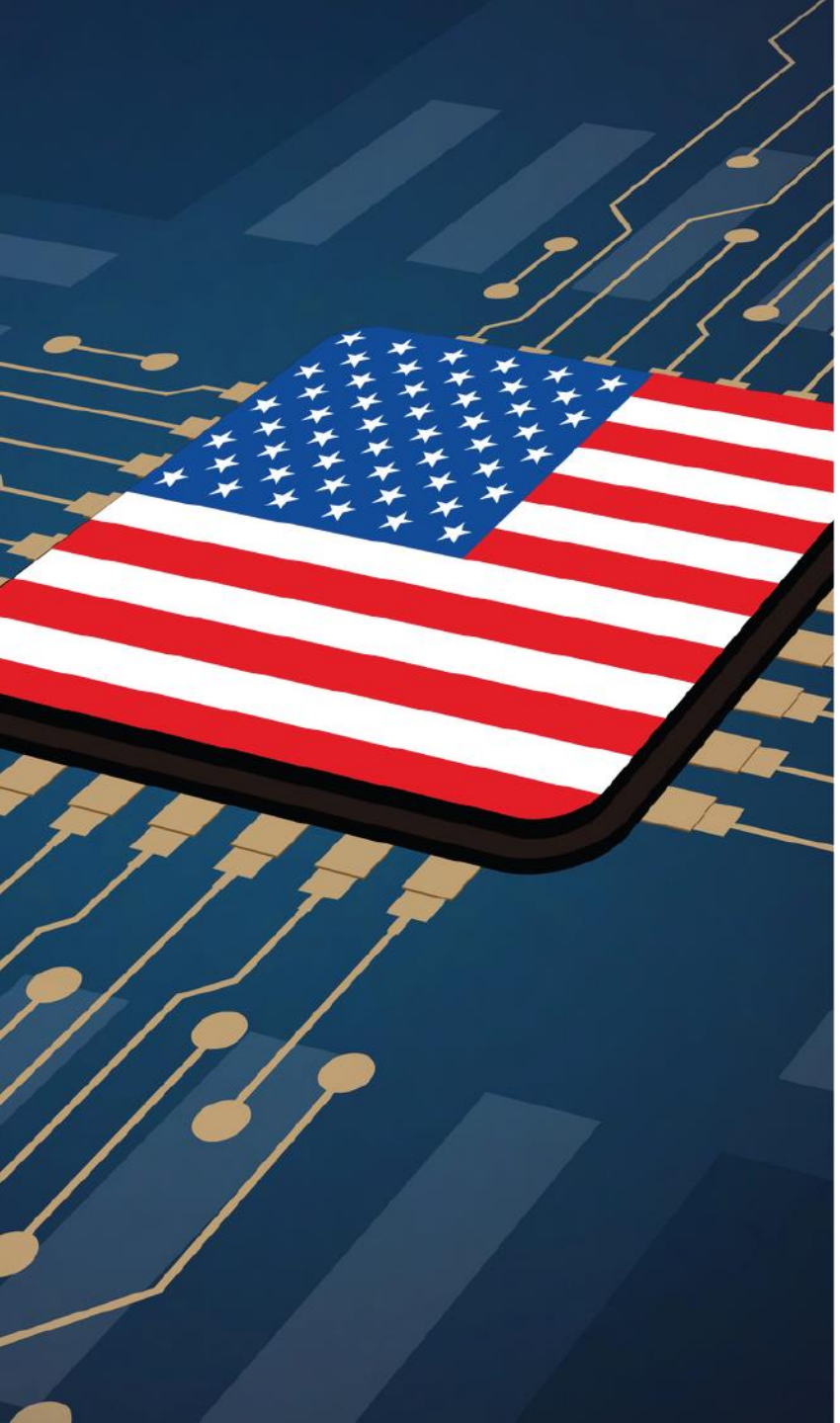
Foundry
Solution fabricated

Defense Programs
Technology evaluated as possible solution for next gen warfighter

Commercial
Technology reaches automotive marketplace, inspires new technology planning

USG Shared Resource Network
Expanded capability, higher chance of success

Disclaimer: Hypothetical capabilities and functions of programs are included only to show the potential benefits of shared resources. Actual capabilities and functions of programs TBD.



Next Steps

- Next steps
  - NSTC White Paper in 1st Quarter 2023
  - Additional steps to be shared afterwards

- Learn more
  - Visit CHIPS.gov
  - Read the Implementation Strategy
  - Join our mailing list

Question and Answers