NIST Integrated Circuits for Metrology Workshop

September 20, 2022 – September 21, 2022

September 20, 2022: Invited Speakers

Workshop Facilitators: Brian Hoskins, Angela Kang, Pauline Truong

10:00 am – 10:10 am (EDT) **Welcome & Introduction** **Brian Hoskins (NIST)**

10:10 am – 10:50 am (EDT) **CMOS Characterization** **Anthony Chou and Victor Chan (IBM)**

Discuss the inline parametric tests of CMOS transistors in logic digital circuits. We monitor electrical data and improve the baseline to meet technology and circuit requirements. After technologies are moved from planar to FinFET era, we will also discuss the challenge in electrical characterization.

10:50 am – 11:25 am (EDT) **Connecting Integrated Circuit Aging to Underlying Transistor Mechanisms** **Stephen Ramey (Intel)**

Interpretation of transistor level reliability from integrated circuit stresses is complicated by the mixing of modes and indirect measurement of the transistor behavior. Additionally, limited circuit response metrics are typically available to give direct, explicit visibility to transistor performance. For example, even simple circuits like ring oscillators are challenging to decipher due to all aging modes typically manifesting along with aging generally being captured simply as an oscillator frequency degradation. This paper details some of the integrated test circuits used by Intel and others, as well as how to interpret the response in the context of the underlying transistor reliability mechanisms.

11:25 am – 11:50 am (EDT) **Smart Arrays: Statistical Technology Assessment at Cryo-Temperatures** **Alexander Grill (IMEC)**

Integrating CMOS circuits and qubits at cryogenic temperatures is one of the key challenges to mitigate wiring constraints and ensure signal integrity to enable up-scaling of quantum computers. While operating in the GHz-regime, interfaces between classical and quantum circuits need to maintain ultra-low power consumption together with very low noise figures. One approach to reduce power consumption is to optimize designs towards operation at lower supply voltages. However, this reduces the tolerable margins on variability, parameter drift, and device to device variations.

In this talk, I will highlight the importance of integrated metrology structures to overcome the measurement bottleneck at cryogenic temperatures based on two case studies: The statistical analysis of time-zero variability and mismatch and the parameter degradation across a large range of gate and drain bias conditions of 28nm foundry technology.

11:50 am – 12:15 pm (EDT) **CMOS & Memory** **Dan Mocuta (Micron)**

In this short presentation we will outline trends in future memories and the increased need for CMOS to provide higher performance and lower power. In this context, we will address some of the challenges encountered in the introduction of advanced CMOS and suggest opportunities for novel characterization techniques.

12:15 pm – 12:45 pm (EDT) **CMOS Electrical Characterization: Needs, Future, Challenges**

This panel will include experts in integrated circuit design and electrical measurement to discuss the future metrology needs for CMOS technology from legacy to advanced nodes.

Moderator: Jason Campbell (NIST)

Panelists: Andreas Olofsson (ZeroASIC), Jason Verley (Sandia), Alexander Petr (Keysight), Zak Chbili (Intel)

12:45 pm – 1:05 pm (EDT) **Break for Lunch**

1:05 pm – 1:30 pm (EDT) **3D NanoSystems for the N3XT 1,000X** **Subhasish Mitra (Stanford)**

The computation demands of 21st-century abundant-data workloads, such as AI / machine learning, far exceed the capabilities of today's computing systems. This challenge gets worse with growing problem sizes especially as conventional transistor miniaturization gets increasingly difficult. This talk will present transformative NanoSystems that target 1,000X system-level energy-delay-product benefits, especially for abundant-data workloads. We create new chip architectures through ultra-dense (e.g., monolithic) 3D integration of logic and memory – the N3XT 3D approach. Multiple N3XT 3D chips are integrated through a continuum of chip stacking/interposer/wafer-level integration — the N3XT 3D MOSAIC. Several hardware prototypes, built in industrial and research fabrication facilities, demonstrate the effectiveness of our approach. We also address new ways of ensuring robust system operation despite the growing challenges of design bugs, manufacturing defects, reliability failures, and security attacks. For example, today's test and diagnosis methods cannot meet the levels of thoroughness demanded by today's (and future) systems --- from (self-driving) cars to the cloud. New "System-Driven" approaches to address these robustness challenges will also be discussed.

1:30 pm – 1:50 pm (EDT) **Photonic Integrated Circuits (PICs) for Sensing and Metrology** **Marcel Pruessner (NRL)**

Photonic integrated circuits (PICs) – similar to electronic ICs but with optical signals – enable new applications in areas ranging from communications to sensing. In particular, the emergence of optical foundries makes possible very large-scale-integrated (VLSI) PICs. Complete optical systems can be realized by combining photonic and electronic components on a single chip resulting in reduced size, weight, and power while lowering manufacturing costs. Much like with electronic chips, however, the growing complexity and density of PICs requires increasing manufacturing process control and metrology tools. This presentation will review some PIC efforts

at NRL and will discuss our recent development of on-chip metrology test structures for extracting material and geometric parameters of optical waveguide components.

1:50 pm – 2:10 pm (EDT) **BioChips: Opportunities and Challenges in Leveraging Integrated Circuits for Bioelectronic Metrology** **Andrew Mason (MSU)**

The aggressive miniaturization of CMOS technology has created unprecedented opportunities and applications in bioelectronic measurement and actuation – which are accompanied by a distinct set of technical challenges and requirements arising from the disparate requirements of biosensors and integrated circuits. These emerging biochips provide new approaches to sense a variety of physical and biochemical properties including nucleic acids, redox reactions, and optical, electromagnetic, electrical, and capacitive properties of samples, in many cases performing completely novel functions that cannot be achieved using traditional approaches. Ongoing challenges include new versions of classical issues in system-on-chip integration, such as wireless power transfer, thermal effects, floor-planning, and signal coupling, as well as new topics that are specifically attributable to the biological domain, such as biocompatibility of materials, integration with MEMS and microfluidics, transparency for optical monitoring, microfabrication processing on single die, electrochemical effects, non-standard packaging, surface functionalization, and sterilization. By establishing dense and information-rich interfaces for biological measurements, biochips offer the potential for significant and disruptive changes in sensing, healthcare diagnosis and delivery, and scientific understanding.

2:10 pm – 2:30 pm (EDT) **PCM for Analog AI** **Victor Chan (IBM)**

We discuss inline electrical testing to monitor the baseline of Analog Computing hardware using Phase Change Memory (PCM) technology. Tightening the PCM resistance distribution is necessary to meet analog computation requirement. A new yield methodology is introduced.

2:30 pm – 2:50 pm (EDT) **Metrology of Ferroelectric Memories** **Asif Khan (Georgia Tech)**

Ferroelectrics based on hafnia and related binary oxides are receiving significant attention as the basis for multiple, next-generation memory technologies such as the ferroelectric random-access memory (FERAM) and ferroelectric field-effect transistors (FEFET). The emergence of ferroelectricity in these materials requires them to be in their crystalline form in these devices, which brings up unique challenges for their technology enablement. This talk will focus on unique metrology aspects with regards to the polycrystallinity of the ferroelectric materials in the context

2:50 pm – 3:10 pm (EDT) **Superconducting Electronics in the "CMOS-Plus" Era** **Karl Berggren (MIT)**

Superconducting electronics has sometimes been considered a "Beyond CMOS" technology: something that might allow electronics to continue its relentless pace of growth in the economy and in technological advancement. However, this status has persisted for decades, yet superconductors have not yet realized their full potential to provide ultra-low-power, ultra-high-performance, low-cost cloud computing in diverse computing architectures. In this talk, I will discuss the key advantages and disadvantages of superconducting computing, and touch on fields such as neuromorphic, reversible, and thermodynamic computing, where superconductors could play a significant role in the future. Most importantly, I will lay out a possible vision for how superconductors can complement CMOS to realize significant future gains in computing.

of their memory applications.

3:10 pm – 3:25 pm (EDT) **15 Minute Break**

3:25 pm – 3:55 pm (EDT) **Metrology, R&D, and Expanding the Foundry Value Chain**

This panel will include experts in materials to systems prototyping for diverse technologies to discuss the opportunities in meeting the metrology challenges of new innovations in the semiconductor and foundry supply chains.

Moderator: Mark Stiles (NIST)

Panelists: Tom Boone (WDC), Ken Shepard (Columbia), Rashmi Jha (U. Cincinnati), Jean Anne Incorvia (U. Texas), Luc Thomas (AMAT)

3:55 pm – 4:10 pm (EDT) **Open science: How open source has enabled the silicon ecosystem acceleration over the last 2 years!** **Tim Ansell (Google)**

Google has been helping more open science to happen in the silicon space since 2020. Open science includes open access, open data, open source, and open standards that offer unfettered dissemination of scientific discourse. Since starting, the work has been getting significant attention with new partners and many users joining the club. This talk will cover the latest updates and the planned roadmap for the coming years of many exciting projects. It will also include Google's perspective on why this is important to a software company. We look forward to enabling more reproducible science by giving full access to all major components of scientific research!

4:10 pm – 4:30 pm (EDT) **Closing Remarks and Nanotechnology Accelerator Platform** **Brian Hoskins (NIST)**

Day 2 of the workshop will feature a working group meeting on the public-private partnership for the nanotechnology accelerator platform. The accelerator platform is a community driven project to create a wafer scale test vehicle for monolithic integration of novel technologies with CMOS. The test vehicle features a planarized form factor and alignment marks to enable university researchers and small businesses to easily perform CMOS integration. User submissions are needed for up to 40 projects in novel nanoelectronic devices, bioelectronics, and more.

September 21, 2022: Working Group Meeting on the Nanotechnology Accelerator Platform

Workshop Facilitators: Brian Hoskins, Angela Kang, Pauline Truong

1:00 pm – 1:15 pm (EDT) **Welcome & Introduction** **Brian Hoskins (NIST)**

A second review of the nanotechnology accelerator platform project as well as an outline of the upcoming talks. Talks will include an introduction to the open source technology used in the platform, a prior history of other community led chip design projects, and talks detailing existing plans and ideas for the upcoming project. The session will end with open discussion to solicit ideas and circuit design contributions from the community of researchers in attendance.

1:15 pm – 1:30 pm (EDT) **Enabling an Open Source Manufacturing Supply Chain** **Steve Kosier (Skywater)**

Open source design is a concept widely associated with software development, offering designers flexibility, lower costs, improved security and faster cycles of learning and progress. Open source has not historically been associated with chip design, until now. In this talk, I will discuss how partnerships among industry, government and academic researchers can enhance U.S. leadership in developing and producing new nanotechnology and semiconductor devices by removing barriers and obstacles related to cost and collaboration for IC design. I will further discuss the ongoing open source initiative and the innovative potential and opportunities for the future of open source chip design and manufacturing.

1:30 pm – 1:40 pm (EDT) **SSCS Committee on Open-Source** **Mehdi Saligane (U. Michigan)**

A new technical committee dedicated to the open source ecosystem (TC-OSE) was approved by the IEEE Solid-State Circuits Society (SSCS) Administrative Committee. Last year's successful Platform for IC Design Outreach (PICO) design contest bolstered this decision to foster the rapidly growing open source community. While still in its ramp-up phase, the nascent open source hardware community is likely to bring a breath of fresh air to the SSCS In its first year, the PICO program was focused on supporting the ramp-up of the open-source ecosystem through sponsored IC fabrication runs on SkyWater's open-source 130 nm-CMOS process. Four shuttle seats were used to support undergraduates and geographical regions that are underrepresented in IC design. Additional six seats were dedicated to an open-source "Chipathon" that ran from July-November 2021. The contest received 61 submissions and a volunteer jury selected 18 teams from 9 different countries. Through a three-month journey with weekly online meetups, these teams collaborated to combine their designs and fill the available silicon real estate with a variety of analog and digital circuits. This presentation will provide an overview of past and ongoing SSCS PICO activities and their broader goals.

1:40 pm – 1:45 pm (EDT) **Michigan Test Structures** **Mehdi Saligane (U. Michigan)**

Since the start of the Google/Skywater open-source initiative, the OpenFASOC project has been at the forefront of open-source chip design. This talk will go through our latest tapeouts using OpenFASOC to support NIST's and Google's nanofabrication project.

1:45 pm – 1:50 pm (EDT) **Maryland Test Structures** **Advait Madhavan (UMD)**

Advait will talk about design considerations in building cross-point arrays for nanodevice characterization. The first round of such designs have been completed and have resulted in successful demonstrations of integration with a variety of material stacks at different organizations. The next round will port these designs to the Skywater PDK and add local measurement circuits at various design scales.

1:50 pm – 1:55 pm (EDT) **GWU Test Structures** **Gina Adam (GWU)**

The ADAM group at GWU will discuss designs for integrated testing of single resistive switching devices, as well as pseudo-resistors, low-frequency amplifiers and computing units for distributed networks such as cellular neural networks and decision trees.

1:55 pm – 2:00 pm (EDT) **CMU Test Structures** **Rick Carley (CMU)**

In this talk Carnegie Mellon will describe an integrated circuit designed to carry out ferromagnetic resonance (FMR) analysis of nanometer-scale thin film magnetic islands. The magnetic island under study will be placed in the middle of one of the two nearly identical transmission lines and the FMR signal will be detected as a tiny change in the magnitude and phase of the RF signal.

2:00 pm – 2:15 pm (EDT) **Open Discussion: Memory/AI Technologies**

2:15 pm – 2:30 pm (EDT) **Open Discussion: Thin Film Transistors**

2:30 pm – 2:45 pm (EDT) **Open Discussion: Bioelectronics**

2:45 pm – 3:00 pm (EDT) **Open Discussion: All topics**

September 20 – Workshop Speaker and Moderator Bio's

Workshop Facilitator: Brian Hoskins (NIST) – Brian Hoskins is a research physicist in the Alternative Computing Group in the Nanoscale Device Characterization Division of the Physical Measurement Laboratory (PML). He received both a B.S. and an M.S. in Materials Science and Engineering from Carnegie Mellon University and a Ph.D. in Materials from the University of California, Santa Barbara. For his doctoral research, he developed and characterized resistive switching devices for use in neuromorphic networks. Brian is working on CMOS integration of resistive switches for the development and characterization of intermediate scale neuromorphic networks.

First Session Speaker: Anthony Chou (IBM) – Anthony Chou has worked in CMOS semiconductor research and development for nearly 25 years in areas spanning from device design to process development. He is currently with IBM Research in IBM Nanotech Center, Albany, NY focusing on advanced CMOS devices.

First Session Speaker: Stephen Ramey (Intel) – Stephen Ramey received the B.S. degree in physics from Carnegie Mellon University, Pittsburgh, PA, USA, the M.S.E.E. degree from the University of Nevada at Las Vegas, Las Vegas, NV, USA, and the Ph.D. degree in electrical engineering from Arizona State University, Tempe, AZ, USA, with a focus on device simulators to include quantum mechanical effects into MOSFETs. He developed a device simulator to include quantum wells into photovoltaic devices at the University of Nevada at Las Vegas. He has been with Solid State Measurements, Inc., developing new spreading resistance and CV metrology systems and published multiple articles on various aspects of the measurement technology. Since 2003, he has been with the Logic Technology Development Transistor Reliability Group, Intel, which he now manages. He has helped develop Intel's logic process technologies from the 90-nm through 7-nm technology nodes. Some notable achievements include guiding the development of the world's first commercial high-k gate process technology (Intel's 45 nm) with a focus on developing first-of-kind models to predict aging and the impact of dielectric breakdown in CPU products. He was the Lead Transistor Reliability Engineer responsible for guiding the development of the world's first commercial FinFET technology (Intel's 22-nm node). In that capacity, he discovered and mitigated multiple new reliability issues associated with the FinFET architecture. His primary contributions to the success of these technologies have been optimizing process flows and device architectures to meet reliability requirements, as well as developing novel predictive reliability modeling capabilities to treat the new physics that emerge with each new technology node. He has authored more than 50 publications spanning the range from semiconductor measurement techniques, photovoltaic devices, device simulation, transistor reliability, and semiconductor process development. He has delivered tutorials and short courses at the IEEE International Reliability Physics Symposium (IEEE IRPS), IEDM, and IIRW. He has multiple U.S. patents granted and in progress. Dr. Ramey won the Best Article Award at the International Reliability Physics Symposium in 2013. He has chaired technical committees at IRPS, IEDM, and IIRW and serves on the Reliability Committee of the Electron Device Society.

First Session Speaker: Alexander Grill (IMEC) – Alexander Grill studied Microelectronics at the Vienna University of Technology, where he received his master's degree in 2013 and his doctoral degree in 2018. He is currently working as a researcher for cryogenic electronics at imec, Leuven. His main scientific interests are characterization and modeling of semiconductor devices at cryogenic temperatures

with a special focus on charge trapping and reliability. His current focus is time-zero variability and the extraction of physical defect properties at cryogenic temperatures to enable technology optimization for low-noise, low-power circuits at cryogenic temperatures.

First Session Speaker: Dan Mocuta (Micron) – Dan Mocuta is working on advanced CMOS for DRAM and emerging memory at Micron. Previously he was the director of the Logic program at imec (Belgium), where he led various projects, including some at the forefront of logic technology research (GAA, VFET SRAM, Beyond CMOS, Quantum computing and advanced BEOL). Before imec Dan lead the FEOL development for several of IBM's logic SOI nodes. Dan holds a PhD in Physics from the University of Pittsburgh, has more than 180 publications and has been cited more than 4300 times.

Second Session Speaker: Subhasish Mitra (Stanford University) – Subhasish Mitra is Professor of Electrical Engineering and of Computer Science at Stanford University. He directs the Stanford Robust Systems Group, leads the Computation Focus Area of the Stanford SystemX Alliance, and is a member of the Wu Tsai Neurosciences Institute. His research ranges across Robust Computing, NanoSystems, Electronic Design Automation (EDA), and Neurosciences. Results from his research group have influenced almost every contemporary electronic system, and have inspired significant government and research initiatives in multiple countries. He has held several international academic appointments — the Carnot Chair of Excellence in NanoSystems at CEA-LETI in France, Invited Professor at EPFL in Switzerland, and Visiting Professor at the University of Tokyo in Japan. Prof. Mitra also has consulted for major technology companies including Cisco, Google, Intel, Samsung, and Xilinx.

In the field of Robust Computing, he has created many key approaches for circuit failure prediction, on-line diagnostics, QED system validation, soft error resilience, and X-Compact test compression.

Their adoption by industry is growing rapidly, in markets ranging from cloud computing to automotive systems. His X-Compact approach has proven essential for cost-effective manufacturing and high-quality testing of almost all 21st century systems, enabling billions of dollars in cost savings.

With his students and collaborators, he demonstrated the first carbon nanotube computer. They also demonstrated the first 3D NanoSystem with computation immersed in data storage. These received wide recognition: cover of NATURE, Research Highlight to the US Congress by the NSF, and highlight as "important scientific breakthrough" by global news organizations.

Prof. Mitra's honors include the Harry H. Goode Memorial Award (by the IEEE Computer Society for outstanding contributions in the information processing field), Newton Technical Impact Award in EDA (test-of-time honor by ACM SIGDA and IEEE CEDA), the University Researcher Award (by the Semiconductor Industry Association and Semiconductor Research Corporation to recognize lifetime research contributions), the Intel Achievement Award (Intel's highest honor), and the US Presidential Early Career Award. He and his students have published over 10 award-winning papers across 5 topic areas (technology, circuits, EDA, test, verification) at major venues including the Design Automation Conference, International Solid-State Circuits Conference, International Test Conference, Symposium on VLSI Technology, Symposium on VLSI Circuits, and Formal Methods in Computer-Aided Design.

Stanford undergraduates have honored him several times "for being important to them." He is an ACM Fellow and an IEEE Fellow.

In the field of Robust Computing, he has created many key approaches for circuit failure prediction, on-line diagnostics, QED system validation, soft error resilience, and X-Compact test compression. Their adoption by industry is growing rapidly, in markets ranging from cloud computing to automotive systems. His X-Compact approach has proven essential for cost-effective manufacturing and high-quality testing of almost all 21st century systems, enabling billions of dollars in cost savings.

Second Session Speaker: Karl Berggren (MIT) – Karl Berggren is the Keithley Professor of Electrical Engineering at Massachusetts Institute of Technology, Department of Electrical Engineering and Computer Science, where he heads the Quantum Nanostructures and Nanofabrication Group. From December of 1996 to September of 2003, Prof. Berggren served as a staff member at MIT Lincoln Laboratory in Lexington, Massachusetts, and from 2010 to 2011, was on sabbatical at the Technical University of Delft in the Netherlands. Prof. Berggren is a fellow of AAAS, fellow of IEEE and a fellow of the International Society for Nanomanufacturing. He is a Kavli fellow, and a recipient of the 2015 Paul T. Forman Team Engineering Award from the Optical Society of America. In 2016, he received a Bose Fellowship and was also a recipient of the EECS Department's Frank Quick Innovation Fellowship. In 2022 he received the Jamieson teaching award from the Dept. of EECS.

Second Session Speaker: Andrew Mason (Michigan State) – Andrew J. Mason received the BS in Physics with highest distinction from Western Kentucky University in 1991, the BSEE with honors from the Georgia Institute of Technology in 1992, and the MS and Ph.D. in Electrical Engineering from The University of Michigan, Ann Arbor in 1994 and 2000, respectively. From 1999 to 2001 he was an Assistant Professor at the University of Kentucky. In 2001 he joined the Department of Electrical and Computer Engineering at Michigan State University in East Lansing, Michigan, where he is currently a Professor and Associate Chair. His research explores mixed-signal circuits, microfabricated structures and machine learning algorithms for integrated microsystems in biomedical, environmental monitoring and sustainable lifestyle applications. Current projects are focused on design of augmented human awareness systems including signal processing algorithms and hardware for brain-machine interface, wearable/implantable biochemical and neural sensors, and lab-on-CMOS integration of sensing, instrumentation, and microfluidics. Dr. Mason is a Senior Member of the Institute of Electrical and Electronic Engineers (IEEE) and an Associate Editor for the IEEE Trans. Biomedical Circuits and Systems. Dr. Mason was co-General Chair of the 2011 IEEE Biomedical Circuits and Systems Conference. He is a recipient of the 2006 Michigan State University Teacher-Scholar Award and the 2010 Withrow Award for Teaching Excellence.

Second Session Speaker: Victor Chan (IBM) – Victor Chan has over 20 years' experience in semiconductor research, development and manufacturing from 90 to sub-10nm technologies for CMOS device design and yield learning. He is currently with IBM Research in IBM Nanotech Center, Albany, NY. Recent research interests include emerging devices for Analog AI computing.

Second Session Speaker: Asif Khan (Georgia Institute of Technology) – Asif Khan is an Assistant Professor in the School of Electrical and Computer Engineering with a courtesy appointment in the School of Materials Science and Engineering at the Georgia Institute of Technology. Dr. Khan's research focuses on microelectronic devices, specifically on ferroelectric devices that address the challenges faced by the semiconductor industry due to the end of transistor miniaturization. His research group at Georgia Tech focuses on all aspects of ferroelectricity ranging from materials physics, growth, and electron microscopy to micro-/nano-fabrication of electronic devices, all the way to ferroelectric circuits and systems for artificial intelligence, machine learning, and data-centric applications.

Second Session Speaker: Marcel Pruessner (Naval Research Laboratory) –
Marcel Pruessner is a research scientist in the Optical Sciences Division at the US Naval Research Laboratory (NRL) in Washington, DC where he leads programs on photonic integrated circuits (PICs), optomechanics and optical MEMS. Beyond these research areas he is also involved in a variety of nanophotonics efforts for chemical sensing, microwave photonics, single photon emitters, and other emerging areas. He received his PhD from the University of Maryland, College Park.

Second Session Speaker: Tim Ansell (Google) – Tim "mithro" Ansell is a software engineer at Google and has been developing open-source software for 20+ years. Tim has recently started trying to shake things up in the hardware accelerator development ecosystem by removing roadblocks to having a completely open ecosystem. Recently he worked with SkyWater Foundry to release a fully open source,

manufacturable PDK for their 130nm process node and is funding a free shuttle program for open-source designs. He has also contributed to projects in the open EDA ecosystem like OpenROAD, OpenRAM, Magic and many others.

Panel 1– CMOS Electrical Characterization: Needs, Future, Challenges

Panel Moderator: Jason Campbell (NIST) – Dr. Campbell is an electrical engineer in the Nanoscale Processes and Measurements Group in the Nanoscale Device Characterization Division of the Physical Measurement Laboratory (PML) at the National Institute of Standards and Technology (NIST). He received his B.S. and Ph.D. in Engineering Science from the Pennsylvania State University, University Park, PA in 2001 and 2007, respectively. His research was focused on electrically-detected magnetic resonance measurements to identify the atomic scale defects involved in one of the most important advanced CMOS reliability problems (the negative bias temperature instability). In 2007, he was awarded a National Research Council (NRC) post-doctoral fellowship which he spent in the Semiconductor Electronics Division at the National Institute of Standards and Technology (NIST) where he is currently employed as a staff member. He has contributed to more than 50 refereed papers and conference presentations at national and international conferences and has been involved in the technical and managerial committees of both the IEEE IIRW and IEEE IRPS conferences. His research interests involve the fundamentals of the negative bias temperature instability, random telegraph noise in highly scaled devices, galvanomagnetic transport effects, and alternative magnetic resonance measurements.

Panelist: Andreas Olofsson (ZeroAsic) – Mr. Andreas Olofsson is the CEO of ZeroAsic. Prior to this he joined DARPA as a program manager in the Microsystems Technology Office in January 2017. His interests include intelligent design automation, system optimization, and open hardware. Mr. Olofsson devoted 20 years to designing and testing low-power processors and mixed-signal circuits at Texas Instruments, Analog Devices, and Adapteva. Chip products designed by Mr. Olofsson include low-power digital signal processors (DSPs), charge-coupled device (CCD) readout circuits, and massively parallel reduced instruction set computing (RISC) processors. From 2008 to 2016, Mr. Olofsson served as the CEO of Adapteva, where he developed the Epiphany architecture and Parallella open source computer. The Parallella democratized access to parallel computing and catalyzed the growth of a community of 10,000 developers and 200 universities across the globe. Mr. Olofsson received his Bachelor of Science in Physics and Electrical Engineering and Master of Science in Electrical Engineering from the University of Pennsylvania. Mr. Olofsson is a member of IEEE and holds nine U.S. patents.

Panelist: Jason Verley (Sandia National Laboratory) – Jason Verley is a developer for Sandia National Laboratories' Xyce analog circuit simulator (SPICE). His focus is radiation-aware compact models and their development. Jason started his Sandia career as a Metrology Process Engineer in Sandia's silicon fab. His other work has included photolithography process engineering, FTIR and emission spectroscopy of photonic microstructures, and optoelectronic simulations using TCAD software. He has been a member of the Xyce team since 2012.

Panelist: Alexander Petr (Keysight) – Alex graduated from the Technical University of Dresden (TU-Dresden) in 2008 with an M.Sc. in microelectronics on the topic of `Carbon Nanotube MOSFET device modeling` under Prof. Schroeter. After graduation, he joined one of the top 10 analog/mixed-signal Foundries (X-Fab) to work as a Characterization, Device Modeling, and Design Support engineer. In his 10 years in X-Fab he developed hardware and software solutions for Semiconductor Device characterization, Big Data workflows for Design enablement, and managed characterization Labs globally.In 2017 he joined Keysight EEsof business to drive software development for Device Modeling and Characterization. In the past 5 years with Keysight, Alex drove transformation projects to enable

more system-level solutions at the customer side using the PathWave Device Modeling solutions through Python enablement and introduction of AI/ML technologies.

Panel 2– CMOS Electrical Characterization: Needs, Future, Challenges

Panel Moderator: Mark Stiles (NIST) – Mark Stiles is a Project Leader and NIST Fellow in the Alternative Computing Group in the Nanoscale Device Characterization Division of the Physical Measurement Laboratory (PML). His research, published in over 165 papers, has focused on the development of a variety of theoretical methods for predicting the properties of magnetic nanostructures and has recently shifted to neuromorphic computing. He has helped organize numerous conferences and has served the American Physical Society on the Executive Committee of the Division of Condensed Matter Physics and as Chair and on the Executive Committee of the Topical Group on Magnetism. He has also served as a Divisional Associate Editor for Physical Review Letters, served on the Editorial Board of Physical Review Applied, and is an Associate Editor for Reviews of Modern physics. Mark is a Fellow of the American Physical Society and IEEE and has been awarded the Silver Medal from the Department of Commerce and the Samuel Wesley Stratton Award from NIST.

Panelist: Tom Boone (Western Digital) – Tom Boone is a technology executive with over 20 years' experience in R&D management and project leadership within the microelectronics and data storage industries. He specifically focuses on HiRel rad-hard microelectronic solutions for defense and aerospace applications. He has expertise in program development and contracting, strategic technical resource planning and timeline execution to achieve challenging milestones. He has made contributions to novel current and future products. (e.g. Spin Torque Embedded MRAM, perpendicular magnetic recording; SoloPower SP1/SP3 large flexible solar modules; heat assisted magnetic recording; advanced diesel engine fuel systems) and is co-inventor of over 20 issued U.S. patents and co-author of 26 peer-reviewed journal articles.

Panelist: Jean Anne C. Incorvia (University of Texas) – Jean Anne C. Incorvia is an Assistant Professor and holds the Fellow of Advanced Micro Devices (AMD) Chair in Computer Engineering in the Department of Electrical and Computer Engineering at The University of Texas at Austin, where she directs the Integrated Nano Computing (INC) Lab. Dr. Incorvia develops practical nanodevices for the future of computing using emerging physics and materials, with a focus on spintronics and low-dimensional materials for neuromorphic computing. Dr. Incorvia received her bachelor's in physics from UC Berkeley in 2008; her Ph.D. in physics from Harvard University in 2015, cross-registered at MIT; and she did postdoctoral research at Stanford University until 2017. She received a 2020 US National Science Foundation CAREER award, the 2020 IEEE Magnetics Society Early Career Award, and a 2021 Intel Rising Stars award.

For this panel, Dr. Incorvia will contribute her experience developing in-memory and neuromorphic computing devices, co-leading a 2022 DOD workshop on R&D for microelectronics, and chairing the Emerging Device and Compute Technologies committee for the 2022 International Electron Devices Meeting.

Panelist: Rashmi Jha (University of Cincinnati) – Dr. Rashmi Jha is a Professor in Electrical and Computer Engineering (ECE) Department at the University of Cincinnati, Cincinnati, USA. She worked as a Process Integration Engineer for Advanced CMOS technologies at IBM Semiconductor Research and Development Center, East Fishkill, NY, USA prior to moving to the academia. She finished her Ph.D. and M.S. in Electrical Engineering from North Carolina State University, Raleigh, North Carolina, USA

in 2006 and 2003, respectively, and B.Tech. in Electrical Engineering from Indian Institute of Technology (IIT) Kharagpur, India in 2000. She has been granted 13 US patents and has authored/co-authored several publications. She has been a recipient of Summer Faculty Fellowship Award from AFOSR, USA in 2021 & 2017, CAREER Award from the National Science Foundation (NSF), USA in 2013, IBM Faculty Award in 2012, and IBM Invention Achievement Award in 2007. She is the director of Microelectronics and Integrated-Computing-Systems with Nanoelectronic Devices (MIND) laboratory at the University of Cincinnati. Her current research interests lie in the areas of Advanced CMOS and Beyond CMOS Devices (such as Resistive Random Access Memory Devices, Ferroelectric FETs, Synaptic Memory Devices), Cross-Technology Heterogenous Integration, Neuromorphic and Brain-Inspired SoC, Trusted Microelectronics, and Neuroelectronics. She is passionate about developing workforce in semiconductors and has been teaching several courses in this area. She is the director of Cleanroom Microfabrication Facility at the University of Cincinnati.

Panelist: Ken Shepard (Columbia University) – Kenneth L. Shepard received the BSE degree from Princeton University, Princeton, NJ, in 1987 and the MS and PhD degrees in electrical engineering from Stanford University, Stanford, CA, in 1988 and 1992, respectively. From 1992 to 1997, he was a Research Staff Member and Manager with the VLSI Design Department, IBM T. J. Watson Research Center, Yorktown Heights, NY, where he was responsible for the design methodology for IBM's G4 S/390 microprocessors. Since 1997, he has been with Columbia University, New York, where he is now Professor of Electrical Engineering and Biomedical Engineering. He also was Chief Technology Officer of CadMOS Design Technology, San Jose, CA, until its acquisition by Cadence Design Systems in 2001. His current research interests include power electronics, carbon-based devices and circuits, and CMOS bioelectronics.

Panelist: Luc Thomas (Applied Materials) – Luc Thomas is a Senior Director at Applied Materials, where he manages the Test and Reliability group. This group is responsible for electrical tests of structures and devices fabricated in Applied's fabs (Maydan Technology Center in Santa Clara and META center in Albany NY). The group activities cover a wide range of current and future semiconductor technologies, from CMOS and MOS capacitors to 3DNAND memory devices, vias and dielectric gap fill to spintronics films and devices (STT and SOT MRAM). Prior to joining Applied Materials, Luc was a Principal Technologist in the STT-MRAM R&D group at TDK-Headway Technologies, and a Research Staff Member at the IBM Almaden Research Center. He has authored and co-authored more than 100 publications and patents on magnetic and spintronics materials and devices. He received his Ph.D. in Physics in 1997 from the University Joseph Fourier in Grenoble, France, and was elected fellow of the American Physical Society in 2012.

September 21 – Workshop Speaker and Moderator Bio's

Workshop Facilitator: Brian Hoskins (NIST) – Brian Hoskins is a research physicist in the Alternative Computing Group in the Nanoscale Device Characterization Division of the Physical Measurement Laboratory (PML). He received both a B.S. and an M.S. in Materials Science and Engineering from Carnegie Mellon University and a Ph.D. in Materials from the University of California, Santa Barbara. For his doctoral research, he developed and characterized resistive switching devices for use in neuromorphic networks. Brian is working on CMOS integration of resistive switches for the development and characterization of intermediate scale neuromorphic networks.

Second Day Speaker: Steve Kosier (Skywater Technology) – Dr. Steven Kosier is responsible for forming and managing strategic technology partnerships and alliances, developing the company's technology roadmap and IP strategy, and growing the value of the company's technology portfolio. His background includes 25 years of experience and successive growth in technical, marketing and business leadership positions. A founding member of PolarFab and Polar Semiconductor wafer foundries, he has developed and transferred to volume production many generations of analog, mixed-signal, and high-voltage technologies for automotive and industrial end markets. Most recently, Dr. Kosier was president at Kanomax FMT, a nanoparticle measurement instrumentation start-up with industry-leading resolution down to 2 nm

Second Day Speaker: Mehdi Saligane (University of Michigan) – Mehdi Saligane received the B.S. and M.S. degrees in electrical engineering systems and industrial computing from the Ecole Polytechnique de Grenoble, Grenoble, France, in 2009, the M.S. degree in electrical engineering from the University of Grenoble, Grenoble, in 2011, and the Ph.D. degree in electrical engineering and computer science from the University of Aix-Marseille (IM2NP), Marseille, France, in 2016.,During his Ph.D. studies, he joined the Michigan Integrated Circuit Laboratory (MICL), University of Michigan, Ann Arbor, MI, USA, as a Visiting Researcher. From 2010 to 2015, he was with the Central Research and Development Group, STMicroelectronics, Crolles, France, as a Research Engineer, where he focused on developing new adaptive solutions and ultra-low power digital design. In 2015, he joined the Michigan Integrated Circuit Laboratory, University of Michigan, as a Research Investigator, where he has been a Senior Research Fellow since 2019, working on synthesizable analog circuits, SoC generations, and automation. He is currently a Visiting Scholar with the Computer Science and Engineering Department, University of California at San Diego, San Diego, CA, USA, where he is also a Design Advisor to the OpenROAD Project. His research interests include adaptive techniques for variability-tolerant designs, near-threshold/subthreshold energy-efficient systems, and design automation.

Second Day Speaker: Advait Madhavan (NIST) – Advait Madhavan is a UMD Assistant Research Scientist in the Alternative Computing Group in the Nanoscale Device Characterization Division of the Physical Measurement Laboratory (PML). He received a Ph.D. in Electrical and Computer Engineering from the University of California, Santa Barbara and is currently working with Mark Stiles and Jabez McClelland. His interests lie in various brain inspired approaches to computation such as temporal, analog and stochastic codes. His expertise lies in VLSI, with the objective of building chips to interface with emerging technologies in order to realize these unconventional computing paradigms.

Second Day Speaker: Gina Adam (George Washington University) – Professor Adam's lab develops novel hardware foundations at the intersection of materials, devices, and circuits to enable new ways of computing. Her research interests are focused on emerging nanoelectronic and nanoelectromechanical

devices and their integration in beyond von Neumann systems such as computation-in-memory and neuromorphic platforms. Her group innovates at the design, simulation and nanofabrication level with a vision of system-level experimental demonstrations. Recent work has been investigating two-terminal non-volatile memory devices called memristors that have an electrical behavior similar to that of an artificial synapse and can be used for both data storage and processing.

Second Day Speaker: Rick Carley (Carnegie Mellon University) – L. Richard Carley (S'74-M'84-SM'90-F'97) received an S.B. in 1976, an M.S. in 1978, and a Ph.D. in 1984, all from the Massachusetts Institute of Technology. He became a Professor in the Electrical and Computer Engineering Department at Carnegie Mellon University (CMU) in Pittsburgh Pennsylvania in 1984. From March 2001 - June 2020, he held the STMicroelectronics Professorship of Engineering. Dr. Carley's research interests include analog and RF integrated circuit design in deeply scaled CMOS technologies, and novel micro-electro-mechanical and nano-electro-mechanical device design and fabrication. For the past several years, Dr. Carley has studied the design of efficient RF Power Amplifiers in advanced BiCMOS technologies. Dr. Carley has been granted 24 patents, authored or co-authored over 200 technical papers, and authored or co-authored over 20 books and/or book chapters. He has won numerous awards including Best Technical Paper Awards at both the 1987 and the 2002 Design Automation Conference (DAC), a "Most Influential Paper" award from DAC, and a "Best Panel Session" award at ISSCC in 1993. In 1997, Dr. Carley co-founded the analog electronic design automation startup, Neolinear, which was acquired by Cadence in 2004. Dr. Carley has served on various conference program committees (e.g., CICC, ISLPED, and TMRC), was Associate Editor of IEEE Transactions on Circuits and Systems from 1993-1996, and was the General Chairman for the RFID-TA 2016 Conference in Shunde, China.