

Instruction Manual

This manual contains instructions for installation and operation of firmware/software necessary to control the Digital Control Box for Phase Stabilization of a Frequency Comb for the purpose of stabilizing a frequency comb. The firmware/software is unsupported with this manual serving as the main documentation. The end-user is responsible for verifying that all software licenses are correct for their use.

Installation

To interface with the FPGA lockbox, you will need to install the following software.

1. WinPython-64bit-2.7.6.4
 - Other Python 2.7 distributions may also work but we cannot guarantee all the correct packages will be installed.
 - The development was performed with the 64 bit version so while the 32 bit version may work, it has not been tested.
 - The python GUI relies on PyQt4. For commercial applications, an additional license would be needed from Riverbank software to use the software as is.
2. Opal Kelly Frontpanel v. 4.0.8
 - Run Setup-Win-x64-4.0.8.exe
 - Make sure that the FPGA box's USB cable is not connected to the PC. Apparently that can mess up with the driver installation (because Windows assigns a generic one if it can't find the correct driver).
 - Windows complains that the driver is not signed but that is OK.

Once the software is installed, files from the Opal Kelly installation will need to be copied into python site-packages folder. Create a new sub-folder named **OpalKelly** in the site-packages sub-folder, i.e. **C:\WinPython-64bit-2.7.6.4\python-2.7.6.amd64\Lib\site-package\OpalKelly**.

Now copy the files from **C:\Program Files\Opal Kelly\FrontPanelUSB\API-64\Python27** to this new folder. The following files should get copied, “__init__”, “__version__”, “_ok.pyd”, “ok”. Change the above paths if you didn't install in the default location.

Python needs know to use the files in **site-packages\OpalKelly**. Open a text editor and write the following “OpalKelly”. Save the file as **C:\WinPython-64bit-2.7.5.3\python-2.7.5.amd64\Lib\site-packages\opalkelly.pth**. The location and extension of the file is important, but not its name. This tells python to load the Opal Kelly package when it boots. Make sure that the extension of the file is indeed .pth and not .pth.txt, as Windows hides known extensions by default. If Python was running while this was done, it needs to be restarted.

The installation is now done. Connect the FPGA board's USB cable to the PC, and turn the board power switch (on the back panel) to ON.

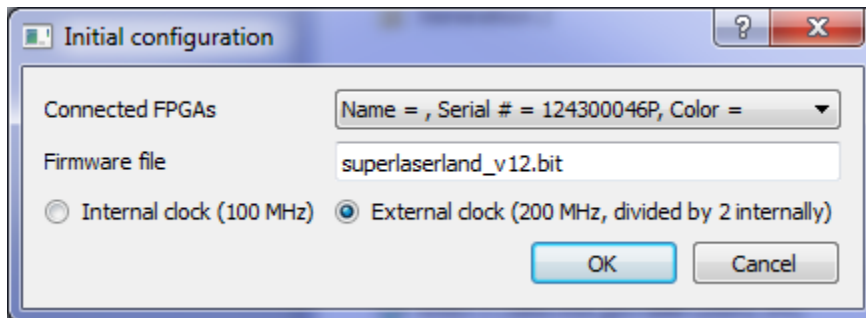
Operation

For general purpose Python use, a Python IDE which installs with the WinPython distribution (Spyder) is started by launching **C:\WinPython-64bit-2.7.5.3\Spyder.exe**.

To operate the control software, run the GUI script file **XEM_gui.py** from **code_packages_for_companies\digital_servo_python_gui**. After running this, the initial configuration window should appear.

The control software includes an assumption that the f_{ceo} input is connected to ADC0, the f_{opt} input is connected to ADC1, the f_{ceo} control output is connected to DAC0, the fast f_{opt} control output is connected to DAC1, and the slow f_{opt} control output is connected to DAC2HV.

Initial Configuration



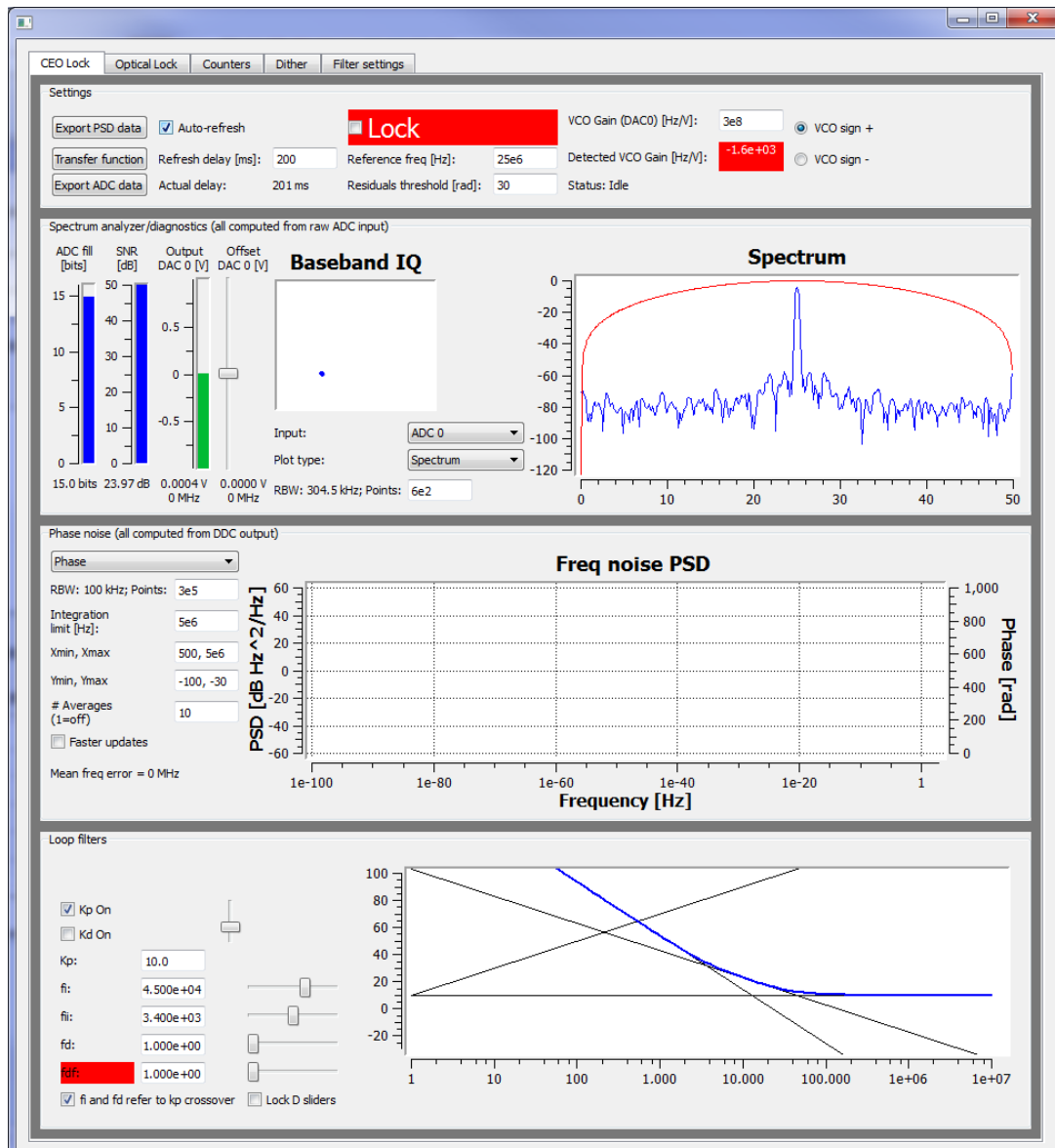
Connected FPGAs provides a drop down list of boxes currently connected to the computer that are not currently controlled by the software. Once an FPGA is controlled by the Python GUI, it will not appear on this list when a second instance of the python script is run.

Internal Clock clocks the FPGA off of its internal 100 MHz clock

External Clock clocks the FPGA off of a 200 MHz input which is divided by two to produce a 100 MHz clock.

OK/Cancel Pressing ok will send the bit file to the selected FPGA with the chosen clock setting and the main GUI should appear.

CEO Lock Tab



Settings Panel

LOCK when checked attempts to phase-lock the input signal to the reference frequency. If the system is successfully locked, the background will be green instead of red. Two warning messages may appear when trying to lock the system. The first will warn the user that the user-input VCO gain appears to differ from the detected VCO gain by more than a factor of 2. The second will warn the user that the detected VCO gain is negative suggesting that the wrong VCO sign has been selected. The user may choose to disregard one or both warnings and have the system try to lock or the user may hit cancel and the system will not try to close the loop.

Auto-refresh should be checked for the upper two panels to be updated at **Refresh Delay**.

Export PSD data saves the realtime phase noise diagnostics to the following files in the data export folder:

- Date_time_freq_noise_axis.bin
- Date_time_freq_noise_psd.bin
- Date_time_inst_freq.bin
- Date_time_raw_adc_samples.bin

Transfer Function creates a pop-up window for recording transfer functions via the virtual network analyzer (VNA).

Export ADC data exports the raw analog-to-digital (ADC) data for the selected number of pts for the selected ADC channel into a binary file.

Reference Frequency is the frequency you wish to lock the input signal to.

Detected VCO Gain [Hz/V] is the estimate of the VCO gain based on the small dither signal applied to DAC0. This box will be green if this value is positive, i.e. the correct VCO sign has been selected, and red if it is negative.

VCO Gain (DAC0) [Hz/V] is the user-input value for the gain which is used for scaling the gains for the CEO lock. Best practice is to use the estimate from the detected VCO gain.

VCO sign +/- Select the sign for the lock.

Residuals Threshold is a tool for diagnosing the quality of the lock and is used by the **Status** display. When locked, the **Status** display will indicate a warning and become orange when the residuals are exceed the threshold given here.

Status indicates the status of the system. Initially, this will read idle. When locked, this will read locked and the background will be green. If the system is railed or the residuals are above threshold, the background will be orange and the system will read a warning. If the system is unlocked, this will read unlocked and have a red background. This will change even if auto-refresh is not checked.

Spectrum analyzer/diagnostics panel

The realtime signal displays here are all computed from the raw ADC input. (Note this is different from the phase noise panel.)

Input selects the input channel. The default is ADC0 and other inputs should only be needed for troubleshooting.

Plot type selects the type of information to display on the right hand plot from the drop down menu.

RBW XXX Hz; Points selects the number of points resolution bandwidth (RBW)

ADC fill is the number of bits used by the ADC currently.

SNR [dB] is the signal to noise ratio of the tone in the selected filter bandwidth (see filter settings for the filter bandwidth).

Offset DAC0 [V] adjusts the DC offset of the DAC0 output. The default value on the system starting is currently 0 V with software limits set to +/- 1 V. The current output voltage is display on the **Output DAC 0 [V]** level display as well as in the text below. The **VCO Gain** is used to compute the frequency shift from the voltage for the display.

Baseband IQ displays the location of the phase of the input signal on an IQ plot.

Phase noise panel

The realtime diagnostics displayed here are all computed from the digital down converter (DDC) output. The graph shows either the phase noise PSD or the frequency noise PSD based on the choice from the drop down menu on the left. The blue curve is the un-averaged PSD, the green curve is the averaged value (if averaging is chosen), and the black curve is the integrated phase noise (plotted on the right y-axis).

RBW: XXX Hz, Points: Select the number of datapoints to achieve the desired RBW for the realtime diagnostics. Selection of a large number of points will slow the update of the window and it may be necessary to adjust the refresh delay (Settings Panel) to longer times.

Integration limit [Hz] sets the starting point for the integration of the phase noise from the integration limit to the x-value.

Xmin, Xmax give the frequency range for the display

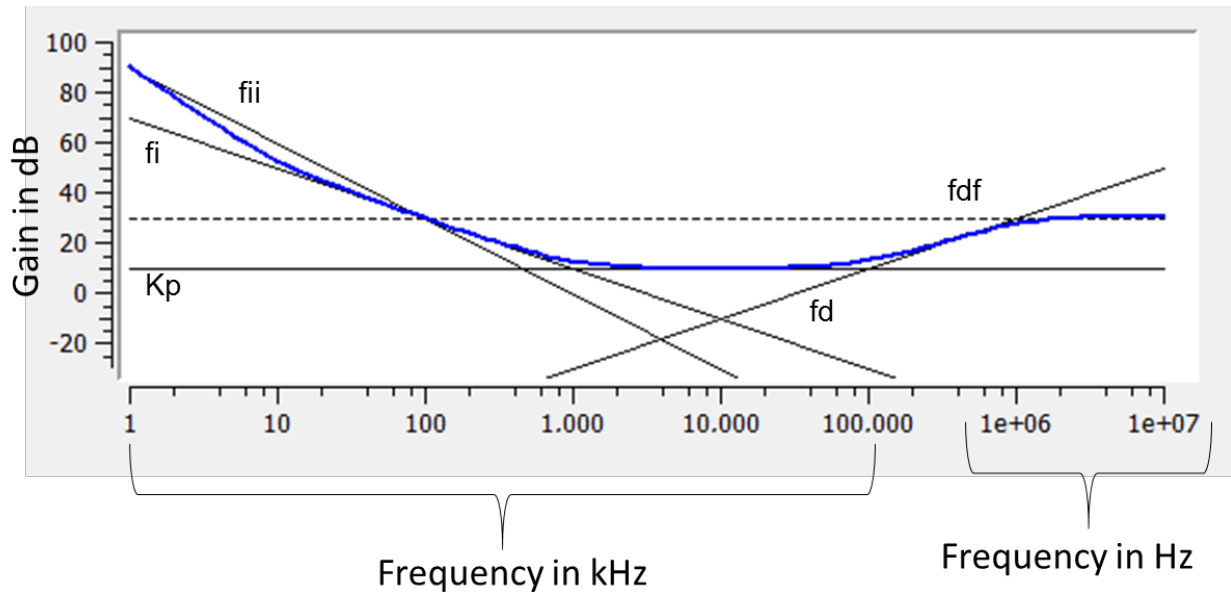
Ymin, Ymax give the y-axis range for the PSD in dBc/Hz.

Averages produces an averaged psd if not equal to 1.

Faster Updates causes the display to update faster.

Loop filters panel

These are the settings to control the loop filter parameters. The results of these are illustrated in the graph below to clarify the inputs. The blue curve is result of using all loop filter options. It should be the sum of the black curves but due to the difference between the s and z transforms it isn't quite.

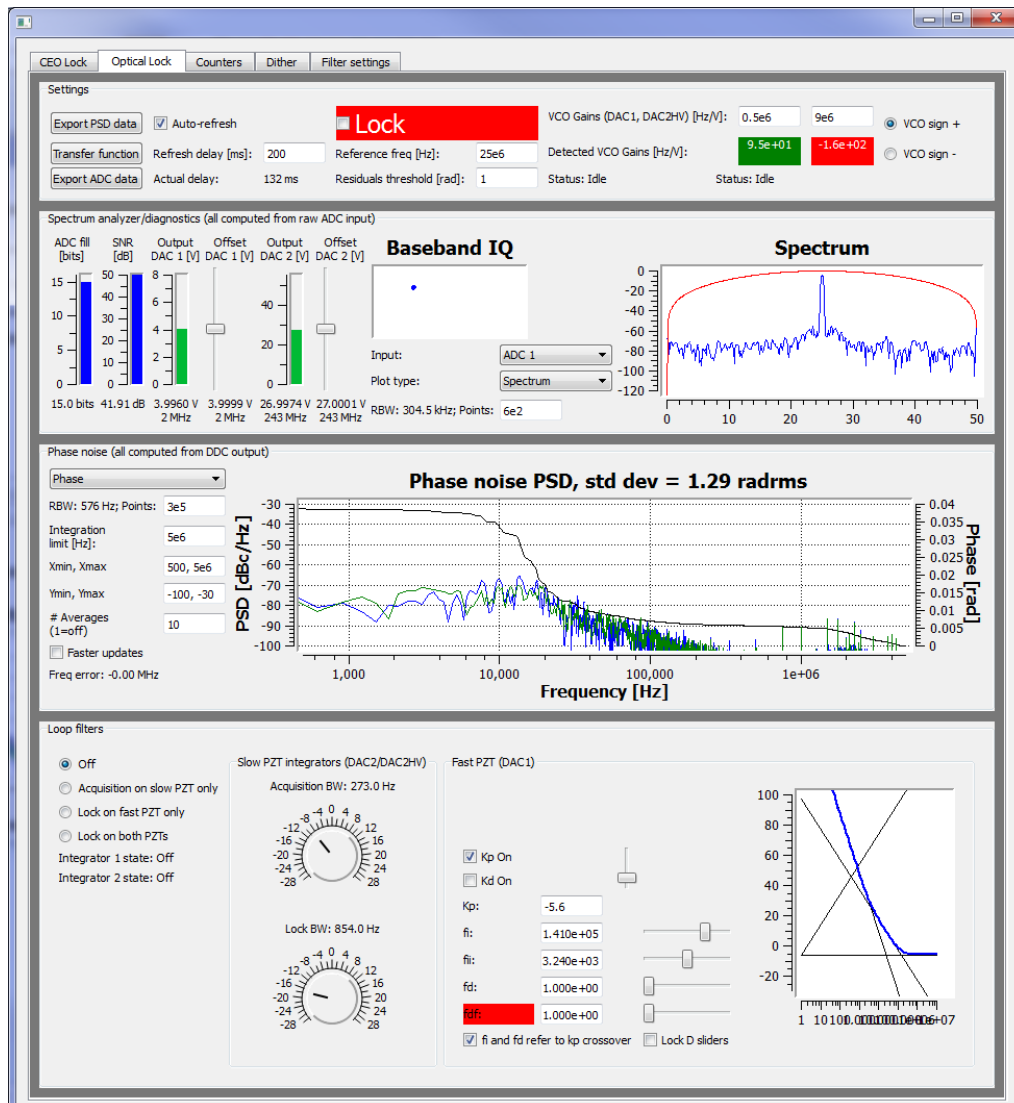


Kp on should be checked to use proportional gain.

fi and fd refer to kp crossover ties fi and fd to the proportional gain level and should be un-checked when using fi and fii only.

Kd on should be checked to use the derivative term.

Optical Lock Tab



Many of the controls for the optical lock tab are identical to those of the ceo lock tab and thus will not be discussed or discussed in less detail.

Settings Panel

Detected VCO Gains [Hz/V] is the estimate of the VCO gain based on the small dither signal applied to DAC1 and DAC2HV, respectively. These boxes will be green if these values are positive, i.e. the correct VCO sign has been selected, and red if they are negative.

VCO Gains (DAC1, DAC2HV) [Hz/V] is the user-input value for the gains which are used for scaling the gains for the optical lock. Best practice is to use the estimate from the detected VCO gains below.

VCO sign +/- Select the sign for the lock. There is only one VCO sign for the lock as this version of the code assumes that the same sign is needed for slow (DAC2HV) and fast (DAC1) outputs.

Spectrum analyzer/diagnostics panel

Offset DAC1 [V] adjusts the DC offset of the DAC1 output. The default value is currently 4 V with software limits set to 0 to 8 V. The current output voltage is display on the **Output DAC 1 [V]** level display as well as in the text below. The **VCO Gain** is used to compute the frequency shift from the voltage for the display.

Offset DAC2 [V] adjusts the DC offset of the DAC2HV (and un-amplified DAC2) output. The default value is currently 27 V with a range of 0 to 55 V. The current output voltage is display on the **Output DAC 2 [V]** level display as well as in the text below. The **VCO Gain** is used to compute the frequency shift from the voltage for the display.

Phase noise panel

This panel is identical to that of the CEO lock tab.

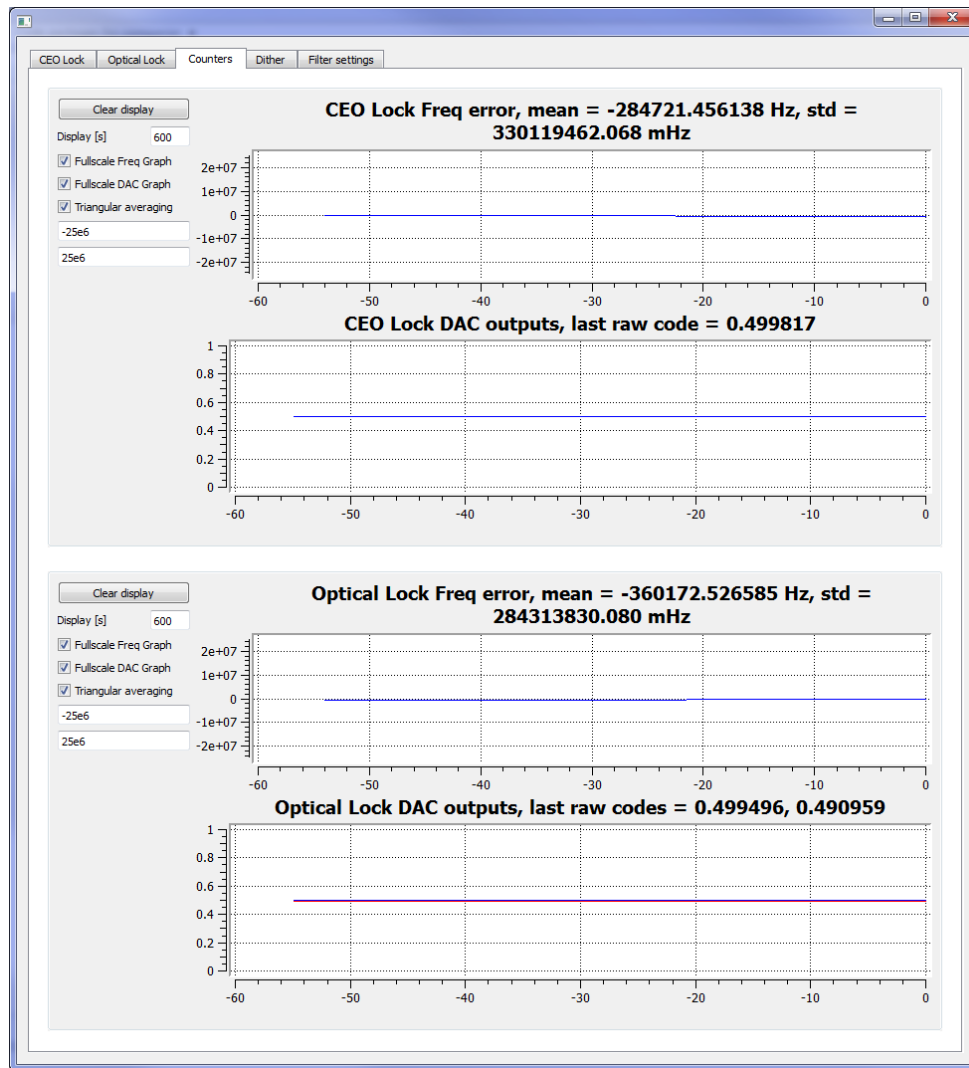
Loop filters panel

This panel contains additional functionality not present in the CEO lock tab due to the presence of two outputs. The Fast PZT (DAC 1) section is identical in operation to that of the loop filter panel on the CEO lock tab.

On this panel, the user can choose to turn the lock off (**Off**), lock using only the DAC2HV output (**Acquisition on slow PZT only**), lock using only the DAC1 output (**Lock on fast PZT only**), or lock using both outputs (**Lock on both PZTs**). Checking the **LOCK** check box in the settings panel will automatically select **Lock on both PZTs** and un-checking the box will automatically select **Off**. This functionality is useful for characterizing the response of the slow/fast actuator.

The **Slow PZT integrators (DAC2/DAC2HV)** allows for the selection of the integrator bandwidth for the DAC2/DAC2HV output when **Acquisition on slow PZT only** is selected, **Acquisition BW**, or for when **LOCK/Lock on both PZTs** is selected, **Lock BW**. The DAC2/DAC2HV portion of the loop only has integral gain.

Counters Tab



The data that is displayed here is also recorded to a log file in the data_logging folder. The log file format is date_time_serialnumber_type where serialnumber is the serial number for the given FPGA and type is the frequency error for the CEO lock (freq_counter0), the frequency error for the Optical Lock (freq_counter1), the normalized DAC outputs for the three DACs (DAC0, DAC1, DAC2), and the time axis (freq_counter0_time_axis).

CEO panel

CEO Lock Freq error plots the deviation of the ADC0 input from the reference frequency defined on the CEO Lock tab.

CEO Lock DAC outputs plots the current DAC output on a normalized scale where 0 is the minimum of the software defined range and 1 is the maximum.

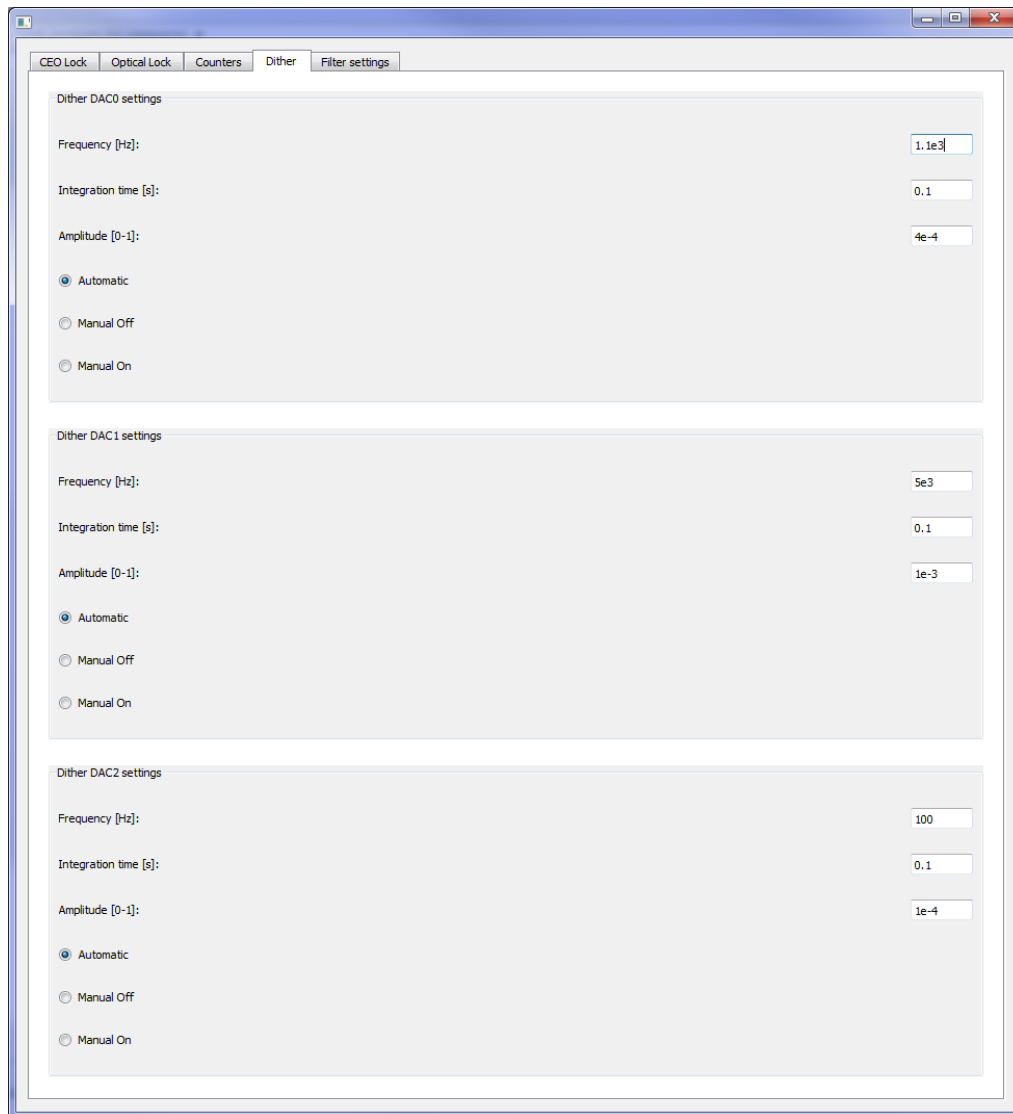
Display [s] the time window over which data is plotted.

Fullscale Freq Graph when checked plots the frequency error on a fixed scale set by the text inputs below the check boxes. When un-checked this autoscales.

Fullscale DAC Graph when checked plots the normalized DAC output from 0 to 1 and when un-checked autoscales.

Triangular Averaging when checked provides triangular averaging vs a boxcar averaging when un-checked. (CHECK THAT THIS IS RIGHT)

Dither Tab



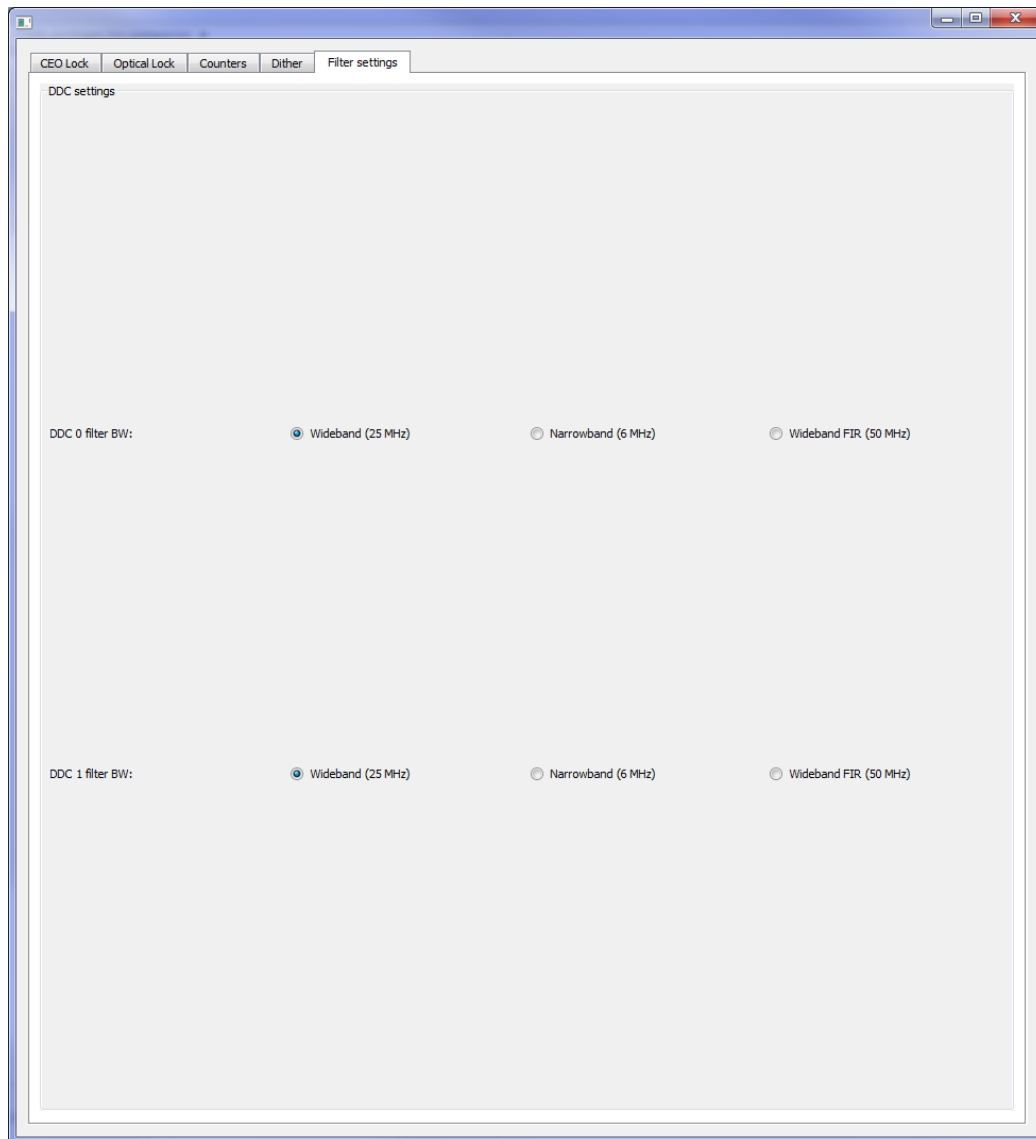
For DAC0 (CEO), DAC1 (Optical, fast) and DAC2 (Optical, slow) a dither is initially automatically applied when the signal is unlocked and turned off upon locking, **Automatic**. It can be manually turned off, **Manual Off**, if needed and once manually turned off must be manually turned back on via **Manual On**. If needed, a dither can be applied while the system is locked via **Manual On**.

Frequency [Hz] sets the frequency of the dither.

Integration time [s] sets the integration time for the detection of the VCO gain.

Amplitude [0-1] sets the amplitude of the dither in units of the scaled DAC output.

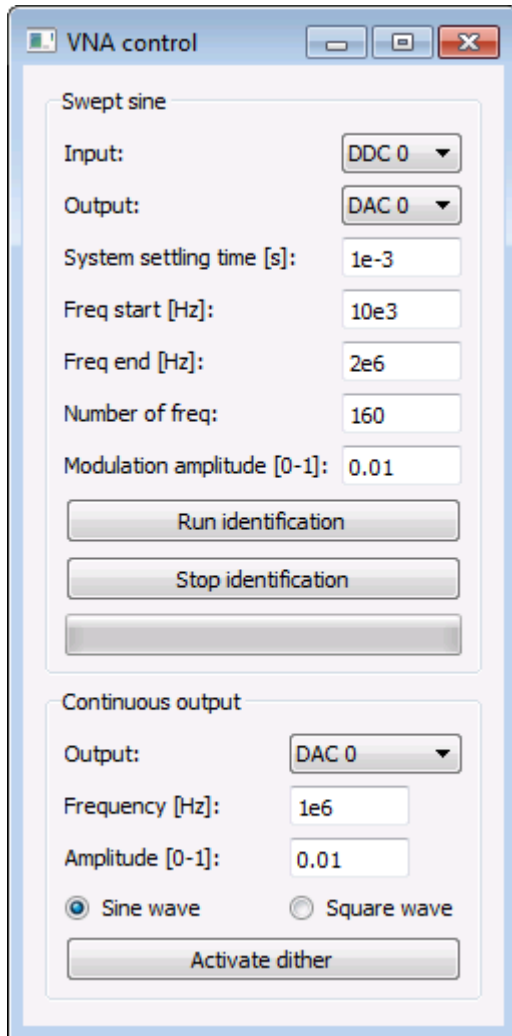
Filter Settings



This tab provides a choice of filter bandwidth for the two inputs. The **DDC0 filter BW** corresponds to the filter for the ceo input and the **DDC 1 filter BW** corresponds to the filter for the optical input.

Transfer Function

The transfer function window is accessed via the CEO Lock or Optical Lock tabs. This provides either a swept sine transfer function measurement or a continuous output of a dither signal. The transfer functions are saved as text files in the transfer function folder with the format of date_time_number.



Input provides a drop down menu to choose either the raw ADC signals (ADC0 or ADC1) or the DDC signals (DDC0 or DDC1) as the input to the measurement. This allows for the measurement of the transfer function of both IF and baseband signals.

Output provides a drop down menu to select which DAC output to put the swept sine signal onto.

System settling time [s] is the amount of time the system waits after it steps to a new frequency.

Freq start [Hz] is the start frequency for the measurement and **Freq end [Hz]** is the stop frequency with the measurement taking linear steps in frequency.

Number of freq is the number of measurement points.

Modulation amplitude [0-1] is the amplitude of the modulation in units of the scaled DAC output.

Run identification starts the transfer function measurement.

Stop identification allows the user to stop the transfer function measurement before it is completed.

Continuous output creates a continuous output on the selected DAC output. This duplicates much of the functionality of the **Manual On** of the dither tab with the additional choice of either a sine or square wave output. **Activate dither** when pressed starts or stops the continuous output.