Microfabricated Surface Electrode Ion Traps

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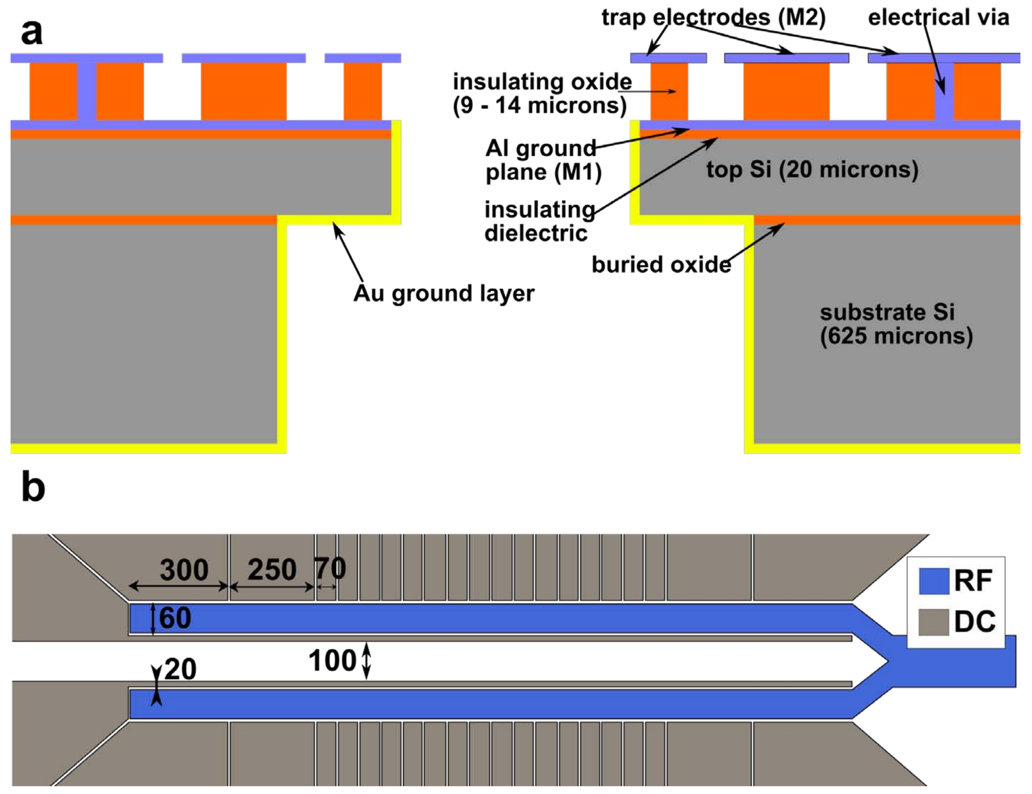
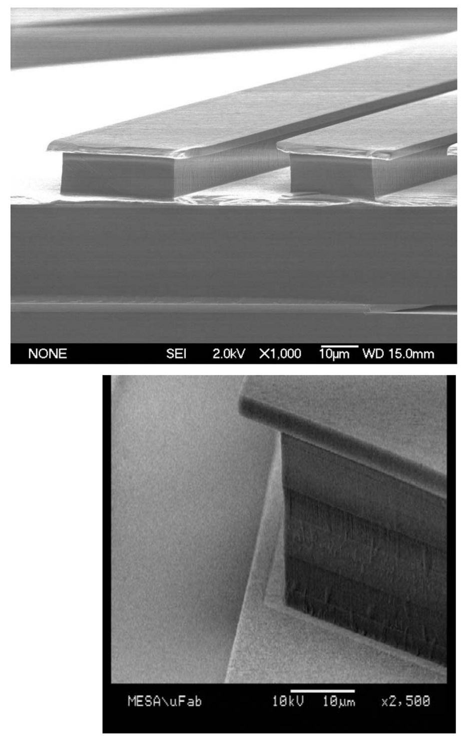
Surface Electrode Ion Microtrap Fabrication

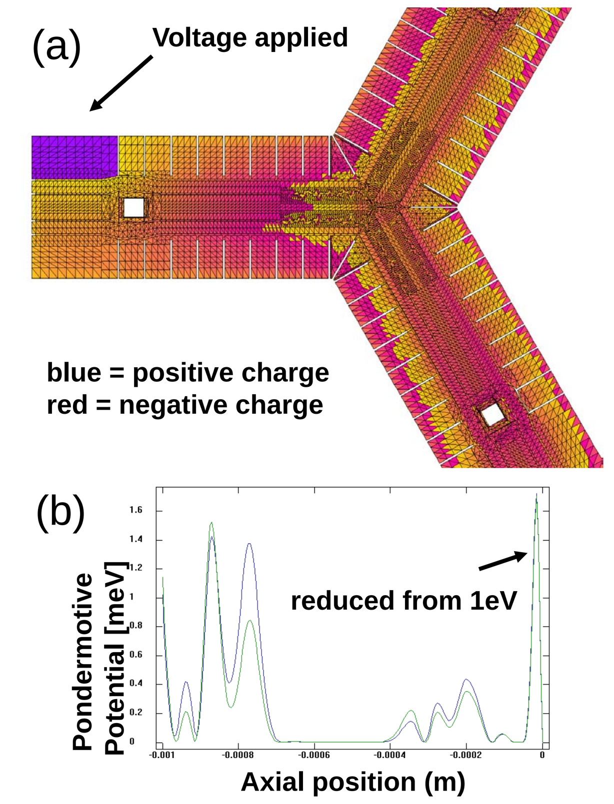




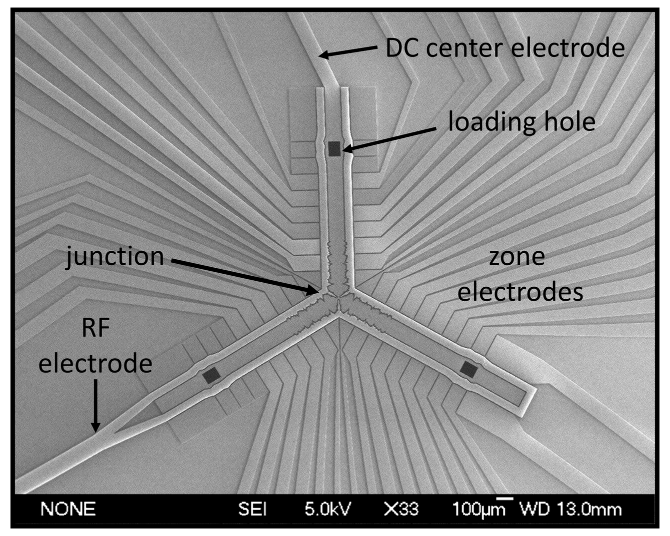
Precision dielectric set-back

- 5 linear traps tested in 3 different groups with Ca⁺ and Yb⁺ [arXiv:1008.0990v1].

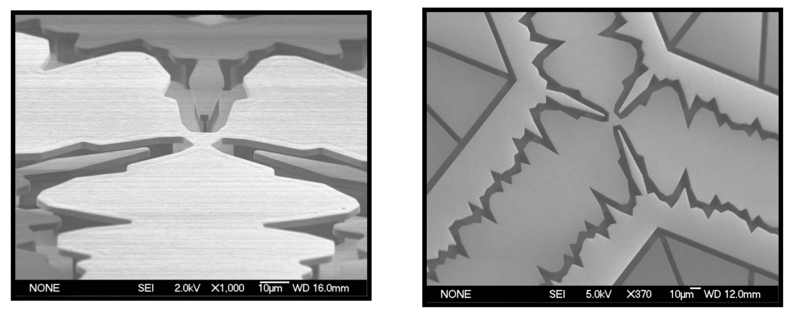
Junction trap



(a) Finite element model of charge distribution
(b) Design minimized RF potential axial variation



With 4 metal levels, all electrode routing will be invisible to ion.



- Trapped single and multiple ions
- Shuttled ion single axis (830 μm) - 10^5 repeat fidelity
- Shuttled to each leg of junction 10^6 times without ion loss
- ***Successful junction shuttling in two different Y-junction models***

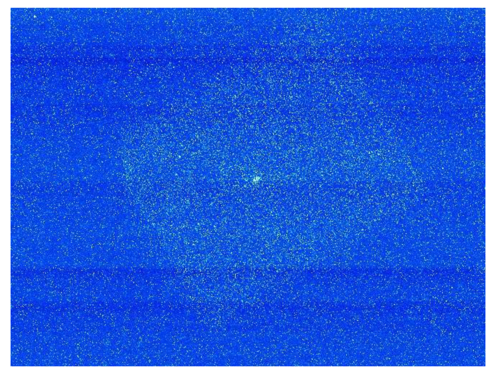


Image of a trapped ion - loading hole is illuminated by the oven

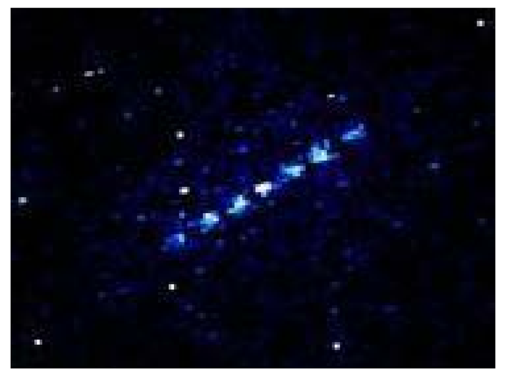


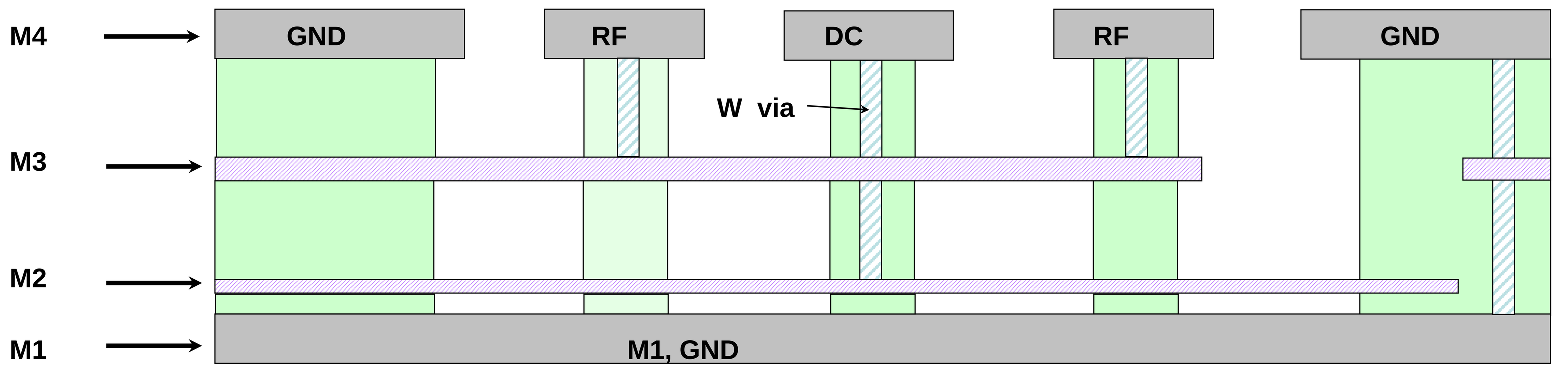
Image of multiple ions trapped within the loading hole

Time lapse image in the junction - a single ion moving up each leg

4 level metal

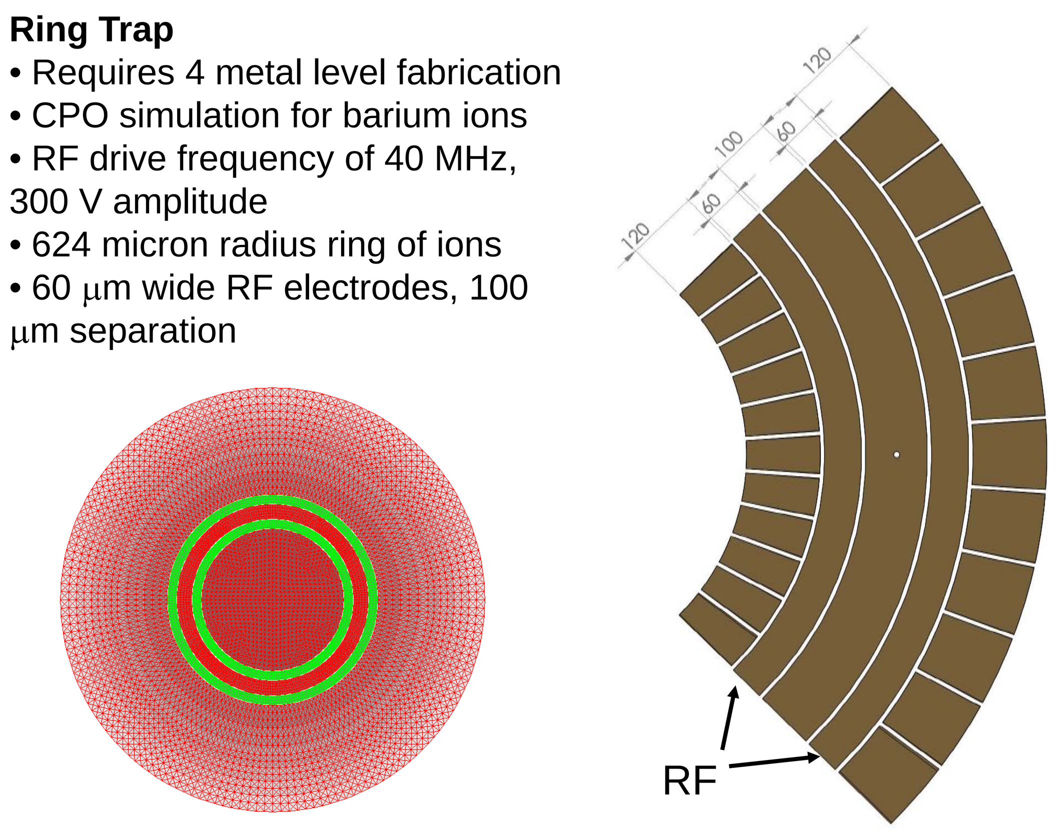
Development - Four metal layer process:

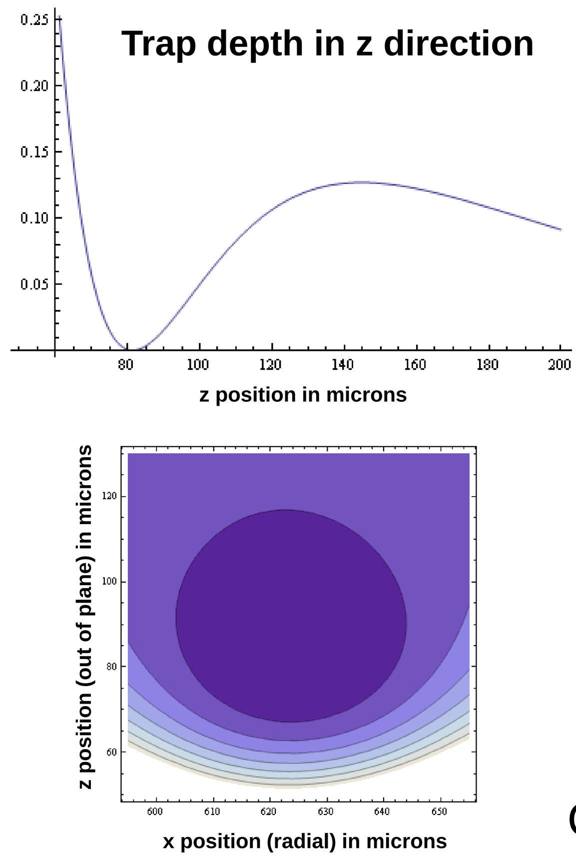
- Routing of RF and Crossing of DC electrodes is required away from trapping regions
- Allows for interior RF/DC electrodes to be wired (e.g. ring trap)
- Simplifies simulations by eliminated need to model effect of leads
- DC lead crossings below M4 electrode level and above M1 ground
- RF routing in stripline configuration with RF, below trap electrode level



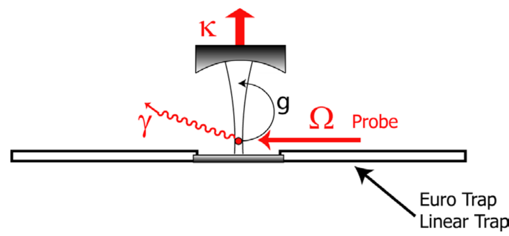
Ring Traps and Cavity QED – MQCO collaboration

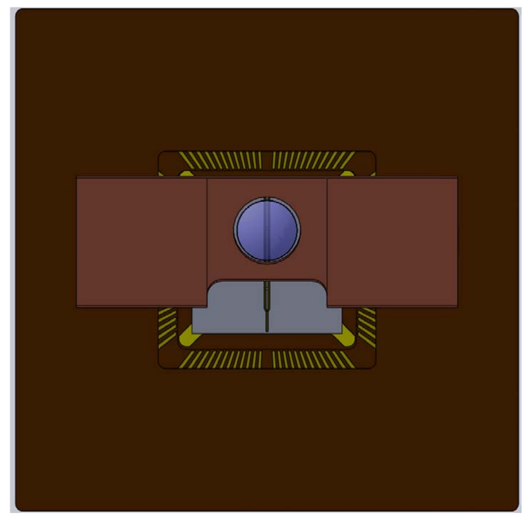
Ring Trap
- Requires 4 metal level fabrication
- CPO simulation for barium ions
- RF drive frequency of 40 MHz, 300 V amplitude
- 624 micron radius ring of ions
- 60 μm wide RF electrodes, 100 μm separation

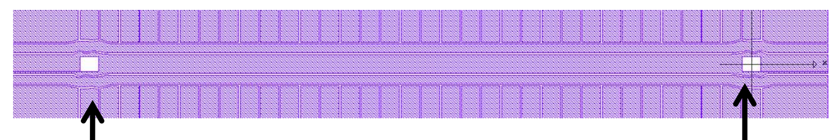




Cavity QED Trap
- Integrate with linear trap
- Sandia will test with Yb⁺
- Mount registered to Si chip
- Initial cavity design for Yb⁺
  - Length = 1 mm
  - Finesse ≈ 4000
  - C_1 = 0.23
  - % Light Collected = 13.73

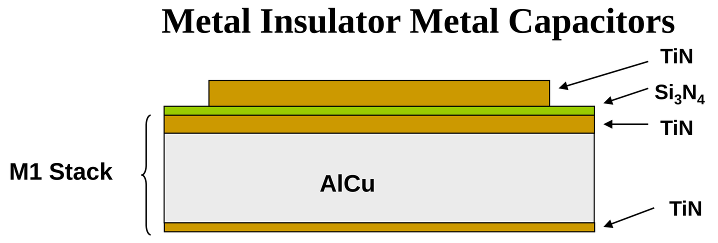






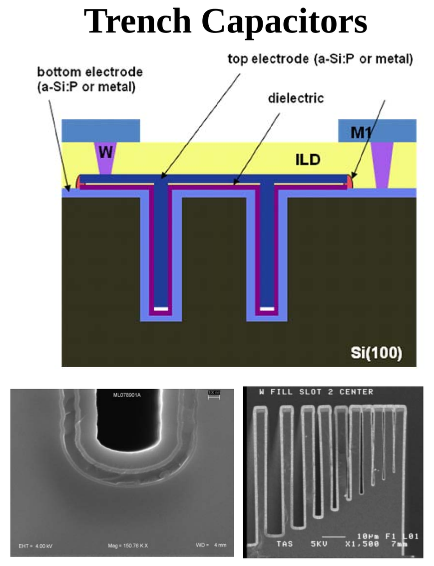
On chip capacitors

Metal Insulator Metal Capacitors

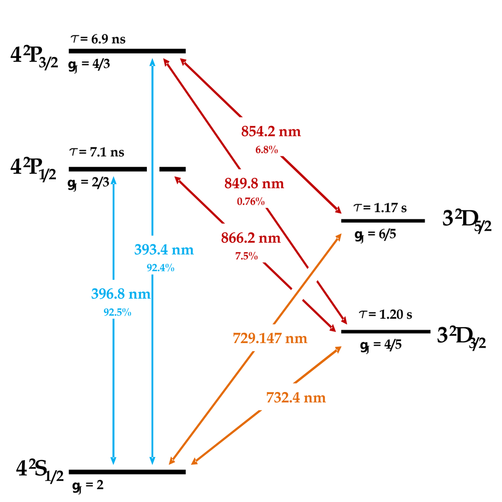


- Higher capacitance density for trench capacitors (94.3 fF/μm² vs. 1.3 fF/μm²).
- Capacitors are located within microns of DC electrode.
- 1nF trench capacitor is about the size of an electrode

Trench Capacitors

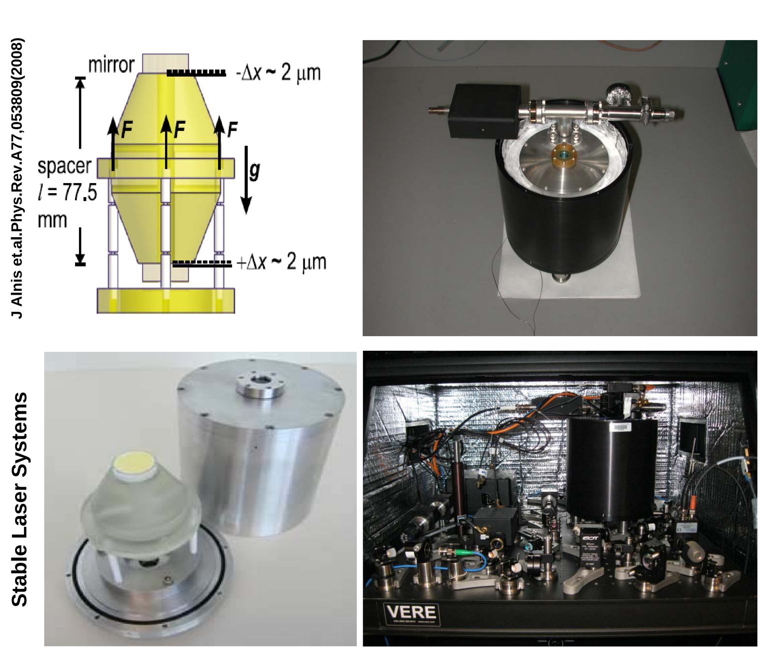


729nm ECDL with a narrow linewidth



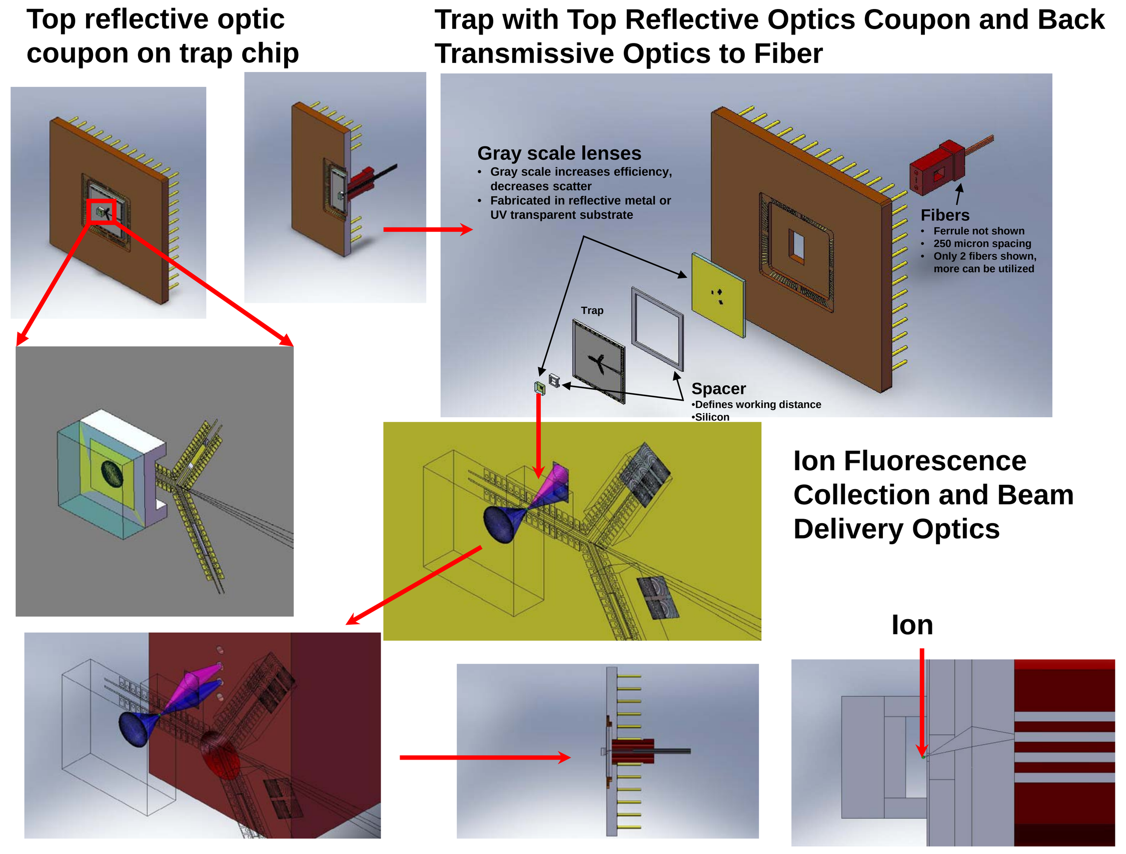
Data source: JBenhelm , Ph.D. thesis(2008)

- ULE midplane mounted vertical cavity and vacuum can
- The cavity has a zero crossing of the thermal expansion typically between 16C and 30C

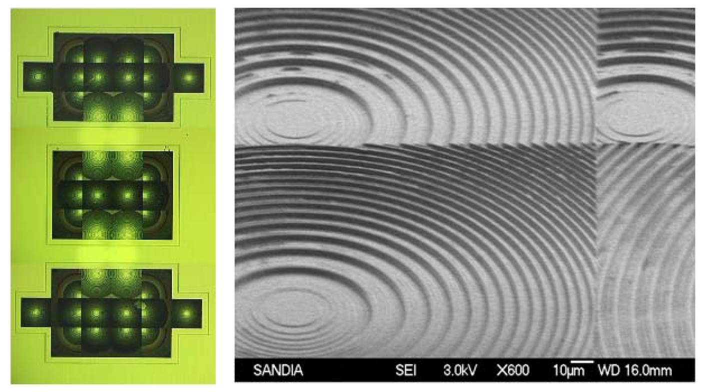


Integrated Diffractive and Micro Optics

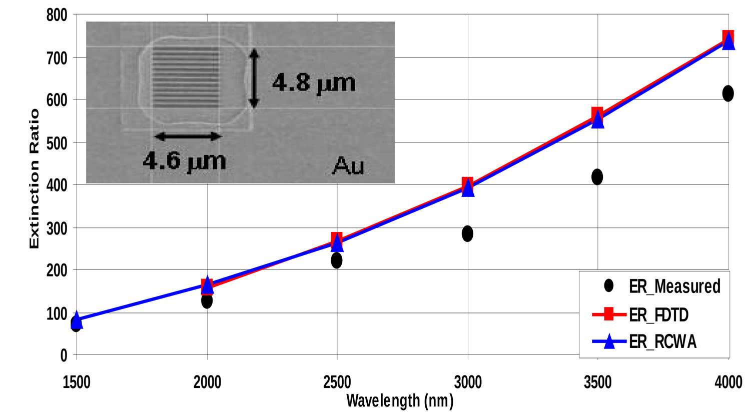
- Can realize transmissive and/or reflective integrated optics
- Off-axis capability → dense optic arrays with 100% fill factor
- Entire lens set is aligned to ions and in-vacuum fiber connector
- Maximum photon interaction in a simple, robust configuration



Existing Sandia Capabilities
- Diffractive Optical Element (DOE) arrays in fused silica with 100% fill factor
- Fused silica and lithium fluoride polarizers with extinction ratios > 100:1
- Microwaveplates with 9.4º rms variation across broad MWIR band

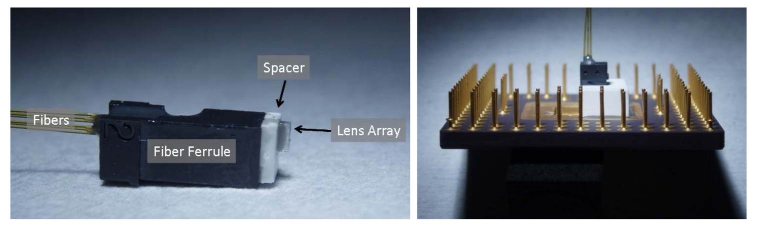


Sandia DOE array in fused silica with 100% fill-factor Optical microscope (L) and SEM (R) images



Broadband extinction ratio of microfabricated polarizer in fused silica

Milestones
- Fabricated 8-level F/1 lenses with focused spot diameters < 1micron at 397 nm
- Multi-fiber feed-throughs and in-vacuum connectors survive bake-out and maintain ultra-high vacuum



G.R. Brady et al. arXiv:1008.2977v1, accepted to Applied Physics B