Characterization Of Nanodevices By STEM Tomography

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ABSTRACT

In order to overcome the limitations encountered by the further scaling of the metal-oxide-semiconductor field effect transistors (MOSFETs) and of the flash memories, new device architectures are introduced. The vertical nanowire tunnel field effect transistor (TFET), with good short channel characteristic (low leakage current) and a subthreshold slope smaller than 60mV/decade (physical limit for the MOSFETs), and the bit cost scalable (BICS) flash memory are among the considered structures for further miniaturization.

The vertical nanowire TFET device consists of a cylindrical single crystalline silicon wire perpendicular to the silicon substrate with the gate layers stack wrapped around it. The BICS flash memory device consists of a cylindrical plug in the polysilicon control gate (CG) in which the memory layers stack (silicon oxide/silicon nitride/ silicon oxide) is deposited. The plug is subsequently filled with the polysilicon channel. Both the nanowire of the TFET device and the plug of the BICS flash memory have a diameter of about 70nm for the studied devices.

Due to the cylindrical symmetry and to the dimensions of these structures, smaller than the typical thickness of the TEM specimens, the overlap of different materials along the electron beam direction renders the interpretation of the conventional TEM and STEM images difficult. Tomographic 3D reconstruction from high angle annular dark field scanning (HAADFS) TEM images series overcomes this problem and is therefore likely the most suited technique to characterize the structure of such nanodevices.

Frontal tomographic slices coming from the center of the TFET and of the flash memory are presented in figure 1 and 2, respectively. Due to the presence of materials with a wide range of atomic numbers for the TFET device, the difference of contrast exhibited by the low-Z materials is small limiting the clear distinction of these layers. The different low-Z materials composing the BICS flash memory however are more clearly observed in tomography than on the conventional TEM and STEM images.

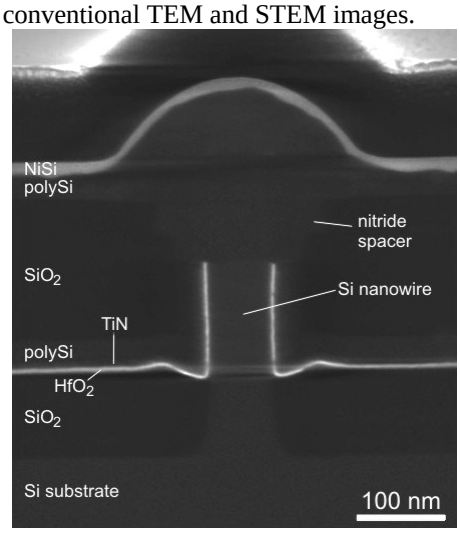

FIGURE 1. Frontal tomographic slice of the center of the TFET device

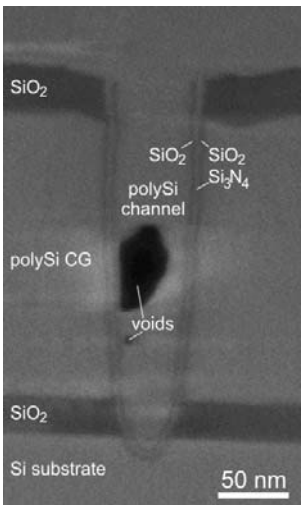

FIGURE 2. Frontal slice of the center of the BICS flash memory

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