

# AFM analysis of high temperature dewetting under ultra high vacuum of ultrathin solid silicon films on insulator

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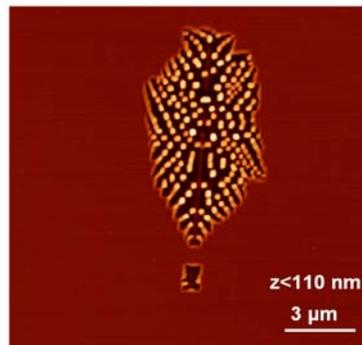
## ABSTRACT

The dewetting of ultrathin silicon layers, induced by the thermal budget, is an issue to develop SOI-based technology. This study aims at demonstrating the effect of the strain on the dewetting mechanism [1] (Figure 1). For that purpose, we present the results obtained on (001) oriented ultrathin (<11 nm) silicon layers on silicon dioxide (SOI). Both stress-free and strained (s-SOI) films fabricated using the “Smart-cut®” [2] process have been studied. We used two s-SOI samples, with respectively 0.8% and 1.6% in-plane strain in the top silicon film.

In order to understand the dewetting mechanism, samples were heated up to ~800°C under ultra high vacuum ( $1 \times 10^{-9}$  mBar) during 10 minutes. The dewetted area topography was characterised by both non-contact and tapping-mode AFM. In addition the chemical composition of these areas was analysed by nano-Auger electron spectroscopy.

AFM results show that Si agglomerates are always present during the dewetting. We will present clear evidences of the influence of strain on the size and density of these Si agglomerates. Moreover, we will show the importance of surface contamination. It is well known that, when heated in ultra high vacuum, carbon contamination can result in silicon carbide (SiC) nanodots [3]. These nanodots induce instabilities at the silicon film surface. Thus, it affects the dewetting mechanism.

To summarize: (i) the level of strain in the silicon films impacts the size and the density of Si agglomerates (ii) silicon carbide nanodots induced by surface contamination influence the dewetting.



**Figure 1.** Topography of SOI sample after dewetting. Image by AFM in tapping mode.

Keywords: dewetting, strained silicon, surface contamination.

## REFERENCES

1. This work was partially supported by the French “Recherche Technologique de Base” Program and performed in the frame of the ANR P3N DEFIS project.
2. B. Ghyselen et al. *Solid-state electronics*, 48, 1285-1296 (2004)
3. Henderson et al. *Journal of Applied Physics* 42, 3 (1970)