Characterization of Strain Induced by PECVD Silicon Nitride Films in Transistor Channel

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In order to reach high level of transistor performances, it is desirable to increase electrical conductivity of the device. An efficient way to enhance carrier mobility in conduction channel is to generate strain in the structure induced by process. To achieve that, stress engineering of the contact etch stop layer (CESL), an amorphous hydrogenated silicon nitride film deposited by plasma enhanced chemical vapour deposition on top of the metal oxide semiconductor assembly, is widely used since it is a low-cost technique. Indeed, this film possesses an intrinsic stress that can be set from tensile (σ=1.6GPa) to compressive (σ=-3.0GPa) depending on deposition conditions.

From an electrical point of view, strain induced in silicon channel can lead to an increase of carrier mobility as high as 8-10% which in turn increases Ion/Ioff and decreases switching time of the transistor. Usually, strain induced in the channel is very low (0.1 – 0.3%), making quantitative measurements challenging. Moreover, stress transmission mechanisms are not fully understood at a nano-metric scale.

To evaluate stress transmission to silicon channel, we are using dark-field electron holography characterization technique operating on both Titan and Tecnai F20 transmission electron microscopes. Strain maps with nanometre spatial resolution, high sensitivity ($\Delta\varepsilon \approx 10^{-3}$%) and large field of view (400 – 500nm²) have been obtained on CESL strained devices. To understand stress transfer mechanisms, we have analysed structures with varying parameters such as film thickness, stoichiometry, film stress, structure density. The experimental results are compared to those obtained by simulation.

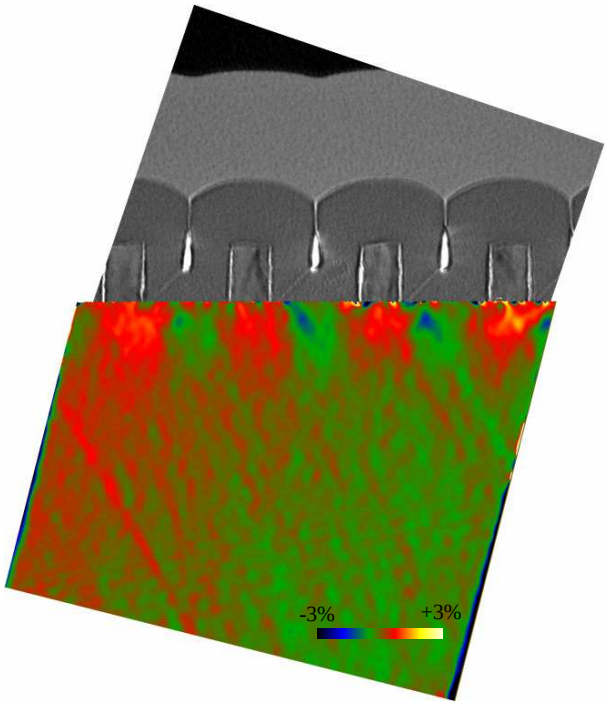

Figure 1: Strain map of a MOS structure with tensile (σ=1.6GPa) CESL stressor

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