Metrology for Emerging Devices and Materials

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Outline

- Acknowledgments
- Trends in Electronics
- The End of CMOS?
- Beyond CMOS – Emerging Devices and Materials

Characterization Needs for Emerging Devices and Materials (using examples)
- Analytical characterization of chemical, structural, electrical, and atomic bonding at the nano-/atomic-scale.
- Electrical test structures for timely characterization of electronic properties of nanoscale components (e.g. molecules, nanotubes, nanowires).
Acknowledgments

People

John Bonevich (TEM)
Christina Hacker (FTIR)
Joseph Kopanski (Scanning Capacitance Microscopy)
Sang-mo Koo (Nanowires)
Michael Gaitan (Single Molecule Measurement and Manipulation)
Qiliang Li (Nanowires)
Eric Lin et al. (Organic Electronics)
Seoung-Eun Park (Scanning Kelvin Probe)
Curt Richter (Molecular Electronics)
John-Henry Scott (Analytical Characterization)
Acknowledgments

CMOS and Novel Devices Group

Performs research and development for the metrology, test structures, and reference materials required for CMOS and Beyond devices and their constituent materials.

Summary of Core Competencies
1. Electrical characterization of CMOS and Beyond devices
2. Broad understanding of electronic materials characterization and surface science including specific expertise in SCM and Ellipsometry
3. Micro-/Nano- fabrication
Acknowledgments

Intl. Tech. Roadmap for Semiconductors

Emerging Research Devices

Emerging Materials

Emerging Logic and Memory Devices

Emerging Architectures

Added to ERD in 2004

Emerging Materials Scope
- Materials to support ERD
- Synthesis
- Characterization
- Modeling
Trends in Electronics

Moore’s Law

- 1945: ~2 cm
- 1948:
- 1959:

Timeline:
- 1948
- 1949
- 1959
- 2014

Graph:
- Heading toward 1 billion transistors in 2007
- Pentium® 4 Processor
- Pentium® III Processor
- Pentium® II Processor
- Pentium® Processor
- 486™ DX Processor
- 386™ Processor
- 8086
- 8088
- 8080
- 400

Published Data
Intel 30nm
Intel 20nm

Gate Delay (psec)

NMOS

1.45 Tera Hertz
VCC=0.75V
L_GATE (μm)
Trends in Electronics
More than Moore’s Law

**Moore’s Law:** Smaller, faster and cheaper logic and memory (CMOS and Beyond)

**Functional Electronics:** On-chip optical components, RF, power, sensors, bio tools, MEMS

**Ubiquitous Electronics:** Putting cheap electronics everywhere
Trends in Electronics

Functional Electronics

On-chip power, optical, memory, RF, sensors

Extracted from Dennis Buss’ Centennial Lecture Series Talk at NIST, “Jack Kilby’s Invention and the Ensuing 40 Years of IC Technology Innovation,” March 30, 2001
On-chip molecular/ biological manipulation and characterization using MEMS

Technical Approach
SM³ Platform

Platform based on Nanofabrication Molecular Assembly

Manipulation (Transport):
Fluidic Restrictions, Beads

Measurments:
Electronic, Optical, Force

Manipulation (Capture):
Vials, Beads, Arrays

M. Gaitan et al. (NIST)
Trends in Electronics

Ubiquitous Electronics

Organic Electronics

cheap dynamic signs

wearable electronics

sensors

semiconducting polymer

dielectric material

electronic paper

source

drain

gate

switching signal

conductive plastic

RFID tags

flexible solar cells

The NIST Organic Electronics Competence Team (E. Lin, C. Richter et al.), Marc Gurau and C. K. Chiang
The Basis of Moore’s Law

**CMOS**

CMOS = Complementary Metal Oxide Semiconductor

FET = Field Effect Transistor

---

**Gate Stack**
- Dual workfunction
- Low sheet resistance
- No boron penetration
- Tight dimensional control

**Gate Dielectric**
- Very thin to improve SCE and current drive
- Limitations: defect density, tunneling current, reliability

---

**Shallow Trench Isolation**
- Litho limited dimensions
- Thickness indep. of size
- Lower capacitance
- No extended thermal oxidation

**Source/Drain**
- Shallow extension to reduce SCE
- Profile optimized for reliability + performance
- Low sheet rho

**Non-uniform Channel**
- Improve SCE
- Halo to counter $V_T$ rolloff
- Reduce junction capacitance

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CMOS = Complementary Metal Oxide Semiconductor

FET = Field Effect Transistor
Possible “Red Brick Walls”
- Equivalent gate dielectric thickness <1nm
- Random dopant fluctuation
- Depletion of the polysilicon gate electrode
- Resistance of contact to devices too high

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**Table 71a**  Thermal and Thin Film, Doping and Etching Technology Requirements—Near-term

<table>
<thead>
<tr>
<th>Year of Production</th>
<th>2003</th>
<th>2004</th>
<th>2005</th>
<th>2006</th>
<th>2007</th>
<th>2008</th>
<th>2009</th>
<th>Driver</th>
</tr>
</thead>
<tbody>
<tr>
<td>Technology Node</td>
<td>hig30</td>
<td>hig30</td>
<td>hig30</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>DRAM 1/4 Pitch (nm)</td>
<td>100</td>
<td>100</td>
<td>100</td>
<td>80</td>
<td>70</td>
<td>65</td>
<td>65</td>
<td>DRAM</td>
</tr>
<tr>
<td>MPU/ASIC 1/2 Pitch (nm)</td>
<td>107</td>
<td>90</td>
<td>80</td>
<td>70</td>
<td>65</td>
<td>57</td>
<td>50</td>
<td>MPU</td>
</tr>
<tr>
<td>MPU Printed Gate Length (nm)</td>
<td>65</td>
<td>53</td>
<td>45</td>
<td>40</td>
<td>35</td>
<td>32</td>
<td>28</td>
<td>MPU</td>
</tr>
<tr>
<td>MPU Physical Gate Length (nm)</td>
<td>45</td>
<td>37</td>
<td>32</td>
<td>28</td>
<td>25</td>
<td>22</td>
<td>20</td>
<td>MPU</td>
</tr>
<tr>
<td>Equivalent physical oxide thickness for MPU/ASIC $T_{ox}$ (nm) $[\text{A, A1}]$</td>
<td>1.3</td>
<td>1.2</td>
<td>1.1</td>
<td>1.0</td>
<td>0.9</td>
<td>0.8</td>
<td>0.8</td>
<td>MPU</td>
</tr>
<tr>
<td>Gate dielectric leakage at 100°C (mA/μm) High-performance [B, B1, B2]</td>
<td>100</td>
<td>170</td>
<td>170</td>
<td>170</td>
<td>230</td>
<td>230</td>
<td>230</td>
<td>MPU</td>
</tr>
</tbody>
</table>

**Table 71b**  Thermal and Thin Film, Doping and Etching Technology Requirements—Long-term

<table>
<thead>
<tr>
<th>Year of Production</th>
<th>2010</th>
<th>2012</th>
<th>2013</th>
<th>2015</th>
<th>2016</th>
<th>2018</th>
<th>Driver</th>
</tr>
</thead>
<tbody>
<tr>
<td>Technology Node</td>
<td>hig25</td>
<td>hig25</td>
<td>hig25</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>DRAM 1/2 Pitch (nm)</td>
<td>45</td>
<td>33</td>
<td>32</td>
<td>25</td>
<td>22</td>
<td>18</td>
<td>DRAM</td>
</tr>
<tr>
<td>MPU/ASIC 1/2 Pitch (nm)</td>
<td>45</td>
<td>33</td>
<td>32</td>
<td>25</td>
<td>22</td>
<td>18</td>
<td>MPU</td>
</tr>
<tr>
<td>MPU Printed Gate Length (nm)</td>
<td>25</td>
<td>20</td>
<td>18</td>
<td>14</td>
<td>13</td>
<td>10</td>
<td>MPU</td>
</tr>
<tr>
<td>MPU Physical Gate Length (nm)</td>
<td>18</td>
<td>14</td>
<td>13</td>
<td>10</td>
<td>9</td>
<td>7</td>
<td>MPU</td>
</tr>
<tr>
<td>Equivalent physical oxide thickness for MPU/ASIC $T_{ox}$ (nm) $[\text{A, A1}]$</td>
<td>0.7</td>
<td>0.7</td>
<td>0.6</td>
<td>0.6</td>
<td>0.5</td>
<td>0.5</td>
<td>MPU/ASIC</td>
</tr>
<tr>
<td>Gate dielectric leakage at 100°C (mA/μm) high-performance [B, B1, B2]</td>
<td>0.33</td>
<td>0.33</td>
<td>1</td>
<td>1.00</td>
<td>1.57</td>
<td>1.57</td>
<td>MPU/ASIC</td>
</tr>
</tbody>
</table>
The End of CMOS?
It’s Going to be Tough to Replace

$>> 10^9$ devices
$<< 10$ nm feature size
$<< 1$ psec gate delay
$\sim 10$ year reliability
$<< 100$ Watts*
$<<$4B to fab*

Feature Size Projections

70% linear shrink every 2 years

Industry Expectation
1999 Forecast
1997 Forecast
1994 Forecast

Published Data
Intel 30nm
Intel 20nm

Gate Delay (psec)

Vcc=0.75V

Pentium® 4 Processor
Pentium® III Processor
Pentium® II Processor
Pentium® Processor
486™ DX Processor
386™ Processor

8088
8086
8080

400
800


1,000,000,000
100,000,000
10,000,000
1,000,000

NMOS

L_{GATE} (\mu m)
Beyond CMOS
Numerous Possibilities

Emerging Technology Sequence

- Cellular array
- Defect tolerant
- Biologically inspired
- Quantum computing

Architecture

- RSFQ
- 1-D structures
- Resonant tunneling
- SET
- Molecular
- QCA
- Spin transistor

Logic

- Phase change
- Floating body DRAM
- Nano FG
- Insulator resistance change
- Molecular

Memory

- Transport enhanced FETs
- UTB single gate FET
- Source/Drain engineered FET
- UTB multiple gate FET
- Quasi ballistic FET

Non-classical CMOS

Risk
### Beyond CMOS

#### Emerging Logic Devices

<table>
<thead>
<tr>
<th>Availability Sequence</th>
<th>1</th>
<th>2</th>
<th>2–3</th>
<th>2–3</th>
<th>4</th>
<th>5</th>
<th>6</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Device</strong></td>
<td>FET</td>
<td>RSFQ</td>
<td>1D structures</td>
<td>Resonant Tunneling Devices</td>
<td>SET</td>
<td>Molecular</td>
<td>QCA</td>
</tr>
<tr>
<td><strong>Types</strong></td>
<td>Si CMOS</td>
<td>JJ</td>
<td>CNT FET</td>
<td>RTD-FET</td>
<td>SET</td>
<td>2-terminal</td>
<td>E: QCA**</td>
</tr>
<tr>
<td></td>
<td>NW FET</td>
<td>NW heterostructures</td>
<td>RTT</td>
<td>3-terminal</td>
<td>3-terminal</td>
<td>M: QCA**</td>
<td>Spin-valve transistor (SVT)</td>
</tr>
<tr>
<td></td>
<td>CNT nanostructures</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Supported Architectures</strong></td>
<td>Conventional</td>
<td>Pulse</td>
<td>Conventional</td>
<td>Conventional</td>
<td>CNN</td>
<td>Memory-based</td>
<td>QCA</td>
</tr>
<tr>
<td></td>
<td>Cross-bar</td>
<td>CNN</td>
<td>CNN</td>
<td>CNN</td>
<td>CNN</td>
<td>QCA</td>
<td>Programmable logic</td>
</tr>
<tr>
<td><strong>Cell Size</strong></td>
<td>100 nm*</td>
<td>0.3 μm</td>
<td>100 nm*</td>
<td>100 nm*</td>
<td>40 nm</td>
<td>Not known</td>
<td>60 nm</td>
</tr>
<tr>
<td>(spatial pitch)</td>
<td>3E9</td>
<td>1E6</td>
<td>3E9</td>
<td>3E9</td>
<td>10E9</td>
<td>1E10</td>
<td>1E10</td>
</tr>
<tr>
<td><strong>Switch Speed</strong></td>
<td>700 GHz</td>
<td>1.2 TzH</td>
<td>Not known</td>
<td>1 TzH</td>
<td>1 GHz</td>
<td>Not known</td>
<td>30 MHz</td>
</tr>
<tr>
<td><strong>Circuit Speed</strong></td>
<td>30 GHz</td>
<td>256–800 GHz</td>
<td>30 GHz</td>
<td>30 GHz</td>
<td>1 GHz</td>
<td>&lt;1 MHz (NEMS)</td>
<td>1 MHz</td>
</tr>
<tr>
<td><strong>Switching Energy, J</strong></td>
<td>2×10⁻¹⁸</td>
<td>2×10⁻¹⁶ (Nb)</td>
<td>2×10⁻¹⁸</td>
<td>&gt;2×10⁻¹⁸</td>
<td>1×10⁻¹⁸</td>
<td>1.3×10⁻¹⁶</td>
<td>2×10⁻¹⁸</td>
</tr>
<tr>
<td><strong>Binary Throughput, GBit/s/cm²</strong></td>
<td>86</td>
<td>0.4</td>
<td>86</td>
<td>86</td>
<td>10</td>
<td>NA</td>
<td>0.06</td>
</tr>
<tr>
<td><strong>Gain</strong></td>
<td>RT</td>
<td>4 K (Nb)</td>
<td>RT</td>
<td>20 K</td>
<td>RT</td>
<td>E QCA Cryogenic</td>
<td>Cryogenic (SFET)</td>
</tr>
<tr>
<td><strong>Operational Temperature</strong></td>
<td>Critical</td>
<td>Not critical</td>
<td>Not critical</td>
<td>Very critical</td>
<td>Very critical</td>
<td>Not critical</td>
<td>Very critical</td>
</tr>
<tr>
<td><strong>CD Tolerance</strong></td>
<td>Si</td>
<td>Nb</td>
<td>CNT</td>
<td>III-V</td>
<td>III-V</td>
<td>C-60</td>
<td>Al/Al₂O₃ (E: QCA)</td>
</tr>
<tr>
<td><strong>Materials System</strong></td>
<td>Si</td>
<td>Nb</td>
<td>HTS</td>
<td>Si</td>
<td>Si-Ge</td>
<td>Si</td>
<td>III-V (SFET)</td>
</tr>
<tr>
<td><strong>Most Complex Circuit Demonstrated</strong></td>
<td>See Table 63b</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
## Beyond CMOS

### Emerging Memory Devices

**Table 62a** Emerging Research Memory Devices—Projected Parameters

<table>
<thead>
<tr>
<th>Storage Mechanism</th>
<th>Present Day Baseline Technologies</th>
<th>Phase Change Memory*</th>
<th>Floating Body DRAM</th>
<th>Nano-floating Gate Memory**</th>
<th>Single-Few Electron Memories**</th>
<th>Insulator Resistance Change Memory***</th>
<th>Molecular Memories****</th>
</tr>
</thead>
<tbody>
<tr>
<td>Device Types</td>
<td>DRAM</td>
<td>NOR Flash</td>
<td>OUM</td>
<td>1TDRAM</td>
<td>Engineered nanowires or nanocrystal</td>
<td>SET</td>
<td>MIM</td>
</tr>
<tr>
<td>Cell Elements</td>
<td>1T1C</td>
<td>1T</td>
<td>1T1R</td>
<td>1T</td>
<td>1T</td>
<td>1T1R</td>
<td>1T1R</td>
</tr>
<tr>
<td>Initial $F$</td>
<td>90 nm</td>
<td>90 nm</td>
<td>100 nm</td>
<td>70 nm</td>
<td>80 nm</td>
<td>65 nm</td>
<td>65 nm</td>
</tr>
<tr>
<td>Cell Size</td>
<td>$&lt;6^2$</td>
<td>$0.065 \mu m^2$</td>
<td>$12.5%$</td>
<td>$0.101 \mu m^2$</td>
<td>$&lt;6^2$</td>
<td>$0.0049 \mu m^2$</td>
<td>$&lt;6^2$</td>
</tr>
<tr>
<td>Access Time</td>
<td>$&lt;15$ ns</td>
<td>$&lt;30$ ns</td>
<td>$&lt;100$ ns</td>
<td>$&lt;10$ ns</td>
<td>$&lt;10$ ns</td>
<td>$&lt;10$ ns</td>
<td>$&lt;10$ ns</td>
</tr>
<tr>
<td>Store Time</td>
<td>$&lt;15$ ns</td>
<td>$&lt;1$ ms</td>
<td>$&lt;100$ ns</td>
<td>$&lt;10$ ns</td>
<td>$&lt;10$ ns</td>
<td>$&lt;10$ ns</td>
<td>$&lt;10$ ns</td>
</tr>
<tr>
<td>Retention Time</td>
<td>$64$ ms</td>
<td>$10-20$ yrs</td>
<td>$&gt;10$ yrs</td>
<td>$&lt;10$ ms</td>
<td>$&lt;10$ yrs</td>
<td>$&lt;160$ sec</td>
<td>$&lt;1$ year</td>
</tr>
<tr>
<td>E/W Cycles</td>
<td>Infinite</td>
<td>$1E3$</td>
<td>$&gt;1E3$</td>
<td>$&gt;1E15$</td>
<td>$1E6$</td>
<td>$1E9$</td>
<td>$&gt;1E3$</td>
</tr>
<tr>
<td>General Advantages</td>
<td>Density</td>
<td>Economy</td>
<td>Non-volatile</td>
<td>Multi-bit cells</td>
<td>Density</td>
<td>Economy</td>
<td>Non-volatile</td>
</tr>
<tr>
<td>Challenges</td>
<td>Scaling</td>
<td>Scaling</td>
<td>Large E/W current</td>
<td>New materials and integration</td>
<td>Need SOI</td>
<td>Retention versus scaling</td>
<td>Dopant diffusion</td>
</tr>
<tr>
<td>Maturity</td>
<td>Production</td>
<td>Production</td>
<td>Development</td>
<td>Demonstrated</td>
<td>Research</td>
<td>Research</td>
<td>Research</td>
</tr>
<tr>
<td>Research Activity****</td>
<td>3***</td>
<td>3</td>
<td>61</td>
<td>40</td>
<td>3</td>
<td>43</td>
<td></td>
</tr>
</tbody>
</table>
Characterization Needs for Emerging Devices and Materials

**Analytical characterization** of chemical, structural, and electrical, properties at the nano-/atomic- scale.

- Unlikely to find one “holy grail”
- Need 2D/3D
- Need Å spatial resolution
- Need atomic sensitivity
- Need subsurface characterization (specifically organic/inorganic).
- Need to profile local properties

**Electrical test structures** for timely characterization of electronic properties of nanoscale components (e.g. molecules, nanotubes, nanowires).

- Results must be independent of contacts
- Need independent confirmation of results
Analytical Characterization

Unlikely to Find One “Holy Grail”

• Quantum dot memories generally show hysteresis and retention time that is strongly dependent on the size and distribution of the dots.

• The measured size of the quantum dots determined using AFM is larger than that determined using TEM.

Analytical Characterization

Need 3D

FIN/Tri-gate FETs are based upon Si-nanowires

Need to monitor:
- 3D properties…
  - Accurate size of wire
  - Film thicknesses (i.e., gate dielectric) on a 3D structure
- 3D Processing parameters:
  Pattern/orientation dependent oxidation?

Multiple Si-nanowire FET

Silicon nanowire

S D G

Intel
Analytical Characterization

2D Compositional Mapping

Energy Filtered Imaging

Spatial Resolution, \(d = C_c \beta \frac{\Delta E}{E_0}\)

\(C_c = 1.4 \text{ mm}, \beta = 10 \text{ mrad}, \Delta E = 20 \text{ eV}, E_0 = 300 \text{ keV}\)

\[\therefore d \approx 1 \text{ nm}\]

"Tuning the Magnetic Properties of Multilayer Nanowires,"
M. Chen, L. Sun,
J.E. Bonevich, D.H. Reich,
C.L. Chien, and P.C. Searson,
Analytical Characterization

Need 3D

J.-H. Scott (NIST)

- Currently, most used approach is 2D projection or surface morphologic imaging with limited chemical mapping
- This approach can easily lead to misinterpretation
- Chemical 3D information is required.

Analytical Characterization

3D Holography using TEM

Electron phase shifts are sensitive to variations in:
- Mean inner potential (thickness)
- Electro-magnetic fields (fluxons, pn junctions)
Analytical Characterization

Need Å Resolution and Atomic Sensitivity

J.-H. Scott (NIST)

Number of Atoms vs. Size

U3O8 Spheres

Increasing Spatial Resolution

Comfort zone for most analytical laboratories

Current research

New technology needed
Spectroscopic characterization of the buried metal-SAM interface can be studied by using infrared radiation through IR-transparent substrates and thin films.

Device = Molecules + Electrodes

*Characterizing the structure of organics is a problem.
Analytical Characterization

Need Subsurface Characterization

**Au (and Al):** minimal perturbation

**Ti:** strong perturbation (but not complete destruction)

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C. Hacker (NIST)
Analytical Characterization

Need to Profile Local Electronic Properties

Scanning Kelvin to profile the surface potential

- Non-contact/destructive measurements of variations in surface potential
- Available for mapping local charge distributions
- Able to monitor processes
- Capable of determining the relative work functions of a conducting surface with a precision of 2~3 meV and a spatial resolution of about 10 nm

S.-E. Park (NIST)

(A conventional MOS structure) (SKPM tip radius ≈ 10 nm)
Analytical Characterization

Need to Profile Properties

- The true tip geometry must be deconvolved from the measurement of the sample.

J. Kopanski (NIST)
A Device prototype that enables robust electrical measurements of molecules.

**Schematic of planar nanoBucket**

**Criteria:**
- Characterizes Molecules
- Tunable to fit Molecules
- Prototypical Device Structure
- “Makeable” (i.e., transferable)

**NanoBuckets allow control:**
- Variety (contacts & molecules)
- Depth (molecular length)
- Area (no. of molecules)
Electrical Test Structures

Contacts

“Ideal structure”

1. Non-invasive top-metal
2. Well-ordered monolayer
3. Smooth bottom contact

• Most common failure mode during fabrication is physical shorting of top- to bottom-metal through molecular monolayer

• Observed electrical behavior in moletronic devices is often not intrinsic to molecules, but attributed to metal interfaces/behavior.

C. Richter (NIST)

We must learn how to successfully put metals on monolayers for molecular electronics to succeed.
Nanowires transistors with different metal contacts (Cr, Ti) were fabricated.

The metal contacts to the nanowire strongly influence the conduction characteristics.

S. M. Koo (NIST)
Methods to characterize the contact resistance to nanowires

4-point Kelvin test structure

Q. Li (NIST)

Transfer length method structure

\[ R_{\text{total}} = \left( \frac{\rho_{\text{nw}}}{S_{\text{nw}}} \right) d + 2R_C \]

Use linear-fit of \( R_{\text{total}} \sim d \)

R-intercept is \( 2R_C \)
Electrical Test Structures

Reproducible Data

- First independent confirmation of molecular device behavior. (Switching observed at both NIST and HP.)

Device = Molecules + Electrodes

CA Richter (NIST) & DR Stewart (HP)

C. Richter (NIST)
Recent results by Lieber et al. suggest that silicon nanowires may have hole mobility much greater than that of bulk silicon => this result was in question.
High Inversion Current in Silicon Nanowire Field Effect Transistors
Sang-Mo Koo, Akira Fujiwara, Jin-Ping Han, Eric M. Vogel, Curt A. Richter, and John E. Bonevich
Web Release Date: 30-Sep-2004; *NanoLetters*

Using geometrically controlled test structures, the dependence of mobility on nanowire width was determined.
Summary

• The future of electronics involves many thrusts: Moore’s Law (faster, smaller, cheaper CMOS and Beyond), Functional Electronics (On-chip optical components, RF, power, sensors, bio tools, MEMS), and Ubiquitous Electronics (Cheap electronics everywhere).

• There are many “red brick walls” for CMOS technology, but it will likely continue for the foreseeable future.

• There are numerous emerging architectures, logic & memory devices, and materials that are being researched for Beyond CMOS.
Analytical characterization of chemical, structural, electrical, and atomic bonding at the nano-/atomic- scale.

- Unlikely to find one “holy grail”
- Need 2D/3D
- Need Å spatial resolution
- Need atomic sensitivity
- Need subsurface characterization (specifically organic/inorganic).
- Need to profile local properties

Electrical test structures for timely characterization of electronic properties of nanoscale components (e.g. molecules, nanotubes, nanowires).

- Results must be independent of contacts
- Need independent confirmation of results