Frontiers in Defect Detection

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Agenda

- Introduction
- Yield Enhancement & ITRS
- Metrology
- Latest Equipment Developments
  - Defect Inspection Tools
  - Gi-SAXS
  - Vacuum Ultra-Violet (VUV)
  - Makyoh Metrology Tool
  - Zero-Defect Resizing of Large Crystalline Silicon Wafers with TLS
  - 450 mm Developments
  - Virtual Metrology (VM)
- Summary and Outlook
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- Summary and Outlook
Introduction

Overall objective: to increase manufacturing yields

- Strong increase in processing complexity requires growing efforts in tackling the challenges in defect detection and yield control
- Defect detection is more than “looking for particles”!
- All defects leading to lower yield must be identified and controlled.

Examples of yield distracting defects possible during microelectronics production processes (source: ITRS YE chapter)
Agenda

Introduction

Yield Enhancement & ITRS

Metrology

Latest Equipment Developments

- Defect Inspection Tools
- Gi-SAXS
- Vacuum Ultra-Violet (VUV)
- Makyoh Metrology Tool
- Zero-Defect Resizing of Large Crystalline Silicon Wafers with TLS
- 450 mm Developments
- Virtual Metrology (VM)

Summary and Outlook
Defect detection is one major scope of activities.

Focus of respective activities was changed and extended with time:

- Defect detection for leading edge technologies
- Defect detection for broad applications (“More Moore” (MM) and “More than Moore” (MtM) technologies, power electronics, mechatronics, MEMS applications, …)

Ever remaining challenges for defect inspection:

- Satisfaction of demands arising from shrinking of device dimensions and corresponding critical defect dimensions
- Keeping in-line inspection costs low!
  → Need for high sensitivity, high throughput and low CoO tools.
Yield Enhancement & ITRS

Overview of focus change and extension of defect detection activities within ITRS

Yield Enhancement with time

Ever remaining challenges:

- Detection and classification of defects of sizes that scale as quickly or faster than the device features
- Increase of measurement sensitivity with simultaneously enhanced differentiation between nuisance defects and killer defects

Wafer edge and bevel inspection; effective inspection of high-aspect-ratio

Defect detection and classification coping with requirements of leading edge technology
Overview of focus change and extension of defect detection activities within ITRS

Yield Enhancement with time

- Introduction of 450 mm wafers
- Requirement for new tool generations providing improved measurement quality with simultaneous reduction of measured data amount to maintain throughput and cost-effectiveness
- Wafer edge and bevel inspection; effective inspection of high-aspect-ratio defect detection and classification coping with requirements of leading edge technology
Overview of focus change and extension of defect detection activities within ITRS Yield Enhancement with time

Focus on broad applications due to advent of MM & MtM technologies, power electronics, mechatronics, MEMS applications, ...

- Inspection of patterns for assembly, packaging and 3D interconnects
- Increased demand for high-throughput in-line characterization combined with automated and intelligent data analysis
- Improvement of 3D inspection: Tool development for high-aspect-ratio and non-visual defects* inspection in 3D structures
- Requirement for new tool generations providing improved measurement quality with simultaneous reduction of measured data amount
- Wafer edge and bevel inspection; effective inspection of high-aspect-ratio
- Defect detection and classification coping with requirements of leading edge technology

* e.g. voids, embedded and sub-surface defects
Yield Enhancement & ITRS

Overview of focus change and extension of defect detection activities within ITRS

Yield Enhancement with time

How to supplement common defect detection for yield enhancement purposes?

→ Use of electrical device characteristics and pass or fail characteristics of chips
→ Use of already present data and statistical/systematical approaches for data analysis

Future challenge:
Appropriate defect detection despite of lacking measurement capacity

Inspection of patterns for assembly, packaging and 3D interconnects
Increased demand for high-throughput in-line characterization combined with automated and intelligent data analysis
Improvement of 3D inspection
Requirement for new tool generations providing improved measurement quality with simultaneous reduction of measured data amount
Wafer edge and bevel inspection; effective inspection of high-aspect-ratio
Defect detection and classification coping with requirements of leading edge technology
Metrology in Semiconductor Manufacturing
Production Ramp Curve

- Process Integration
- Pilot
- Mass Production

Technology Transfer

- Process Creation
- Process Selection
- Process Tuning
- Process Stabilization
- Product Production

Source: Giichi Inoue, Toshiba Semiconductor
Contributions by Fraunhofer IISB
Network in Metrology
Agenda

- Introduction
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- Metrology
- **Latest Equipment Developments**
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Latest Equipment Developments
Innovative Meso Defect Inspection (SEA-Project)

Short description:
- Implementation of new very high throughput and high sensitivity approach for wafer inspection
- Assessment for 3D-Integration (TSV), patterned and un-patterned wafer inspection

Today's Standard Technology:

Advances
- Combines bright field illumination, dark field illumination with full wafer illumination without movement of the wafer
- Bright or dark field images of the full 300mm wafer are captured in one shot at high sensitivity of 1-10µm
- Use of full-wafer imaging permits for the first time to rapidly inspect every processed wafer at 100% of the surface
- SW algorithms to extract the defects of interests reliably and to automatically identify defect signatures are being optimized during the project
Latest Equipment Developments

Defect Inspection Tools

State of the Art in defect inspection:

- SEM (pixel resolution < 3nm)
- Patterned and unpatterned wafers
- Root cause analysis:
  - Difficult due to variety of defect types
  - Material information required
- Slow SEM measurements
  - throughput limited
  - especially for upcoming 450 mm wafer processing

Source: Applied Materials
Latest Equipment Developments
Defect Inspection Tools

New developments in defect inspection:

- Increased pixel resolution (< 1nm) enables detection of smaller defects
- Integration of material analysis detectors (e.g. EDX, WDX) for improved defect review
- Utilization of multi-column e-beam SEM systems for improved throughput

Source: Applied Materials
Latest Equipment Developments
Grazing-incidence small-angle x-ray scattering (GI-SAXS)

Inspection of surface structures in thin layers

- Novel functional layers increase demand for advanced layer characterization techniques (e.g. pore size distribution in low-k materials)
- GI-SAXS enables detection and characterization of surface structures in thin layers ➔ improved defect inspection capabilities
- Full layer characterization through combination with XRR/XRD techniques:
  - Film thickness
  - Film density
  - Crystallographic properties

(source: Institute of Physical Chemistry – University of Hamburg)
Latest Equipment Developments
Vacuum Ultra-Violet (VUV)

Characterization of ultra thin layers at VUV wavelengths

- Key dielectric materials applied in semiconductor manufacturing have unique absorption properties at VUV wavelengths (120 nm to 200 nm)

- VUV measurement applications
  - Thickness measurement at ultra thin (<10 nm) layers, e.g. SiO2/Si3N4 (ONO), HfO2
  - Determination of material composition, e.g. SiON, high-k layers
  - Fast, non-destructive inline characterization

VUV reflectometer for 200 mm/300 mm wafers
Investigation of *in situ* contamination layer removal by VUV/VIS exposure

- Efficiency and control of the contamination removal
- Influence of the VUV exposure on the measurement result

**Results**

- Repeated measurements clean monolayer from surface
- Selection of measurement point reflecting clean surface depends on type of material
- Layer modification visible as small increase of thickness (1 to 4 pm/pt); reduction by minimization of measurement time

**Surface contamination removal and layer modification during the VUV measurement**

- Clean surface

- ≈ 0.2 nm (monolayer)
Latest Equipment Developments
Vacuum Ultra-Violet (VUV)

Application example – analysis of SiON thin films

- Analysis of the measurement point after contamination removal

<table>
<thead>
<tr>
<th>Method</th>
<th>$N_2$ concentration (%)</th>
<th>SiON layer thickness (nm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>VUV</td>
<td>9.9 ± 0.35</td>
<td>1.6 ± 0.01</td>
</tr>
<tr>
<td>XPS</td>
<td>9.4 ± 0.30</td>
<td>1.9 ± 0.02</td>
</tr>
</tbody>
</table>

- The results show a good correlation to the XPS measurement for nitrogen concentration

- The layer thickness measured by VUV is ≈ 0.3 nm thinner than the XPS results which may indicate the present contamination layer measured within the XPS results
Makyoh (magic-mirror) principle:

- The intensity distribution of initially collimated light that was reflected from the wafer surface carries (qualitative) information about the wafer topography

→ real-time defect detection

**Polishing marks and dimples on a Si wafer**
Latest Equipment Developments
Makyoh Metrology Tool

Quantitative Makyoh
Structured illumination is used to quantify the measurement

- Projection of patterns e.g. gratings (binary intensity coding) or continuous (color) patterns (multi-level intensity coding or multi-wavelength coding)
- Detect pattern distortion
- Calculate surface slopes
- Retrieve height topography by 2D-integration

Flatness (top) and Nanotopography (bottom) of a polished Si wafer
Latest Equipment Developments
Makyoh Metrology Tool

- Current specifications of prototype
  - Measuring area: φ 135 mm (→ R&D for φ 300 mm)
  - Vertical resolution: < 20 nm
  - Lateral resolution: 100 µm

- Benefits
  - Large measuring area, no scanning → high throughput
  - Fast defect detection
  - Robust to external vibrations due to slope measurement
Latest Equipment Developments
Zero-Defect Resizing of Large Crystalline Silicon Wafers with TLS

Thermal Laser Separation (TLS)

- **Principle of TLS:** Crack guiding with thermally induced mechanical stress

  - **1. Step – Crack initiation:** With diamond tip or ablation laser
    → Predetermined cleaving point

  - **2. Step – Cleaving:** Laser-based heating, subsequent water cooling
    → High tensile stress inside the overlap zone between heating and cooling results in a complete cleaving of the substrate
Latest Equipment Developments
Zero-Defect Resizing of Large Crystalline Silicon Wafers with TLS

TLS for resizing large crystalline Si wafers
- Cleaving process is **not bound by lattice planes**
- Mounting on tape and frame is not necessary
- Single crystalline (100) Si wafers
- 200 W cw fiber coupled **fiber laser**
- **NIR** wavelength
- 7-9 ml/min water flow rate for cooling

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Latest Equipment Developments
Zero-Defect Resizing of Large Crystalline Silicon Wafers with TLS

Results of resizing large Si wafers with TLS

- **High edge quality**
  - Zero chipping
  - Smooth side walls
  - No residual mechanical stress
  → High bending strength

- **Short process time**
  - Feed rate 20-40mm/s
  - 3-5min/wafer (300mm → 200mm)
  → High throughput

- **TLS** is a promising technique for zero-defect resizing
Requirements for 450 mm and possible benefits for smaller diameters include:

- Improved equipment performance
- Lower defect generation
- Significantly better control
- Advanced sensors
- Faster handling and processing
- Higher equipment reliability
- Significantly better data processing
# 450 mm Tools

## Impact of 450 mm Wafer Diameter on Equipment and Metrology Tools

<table>
<thead>
<tr>
<th>Impacted Areas</th>
<th>Focus Items</th>
</tr>
</thead>
<tbody>
<tr>
<td>Processes</td>
<td>Process uniformity, contamination, thermal effects/uniformity, (cleaning, polishing, deposition, etch, anneal, ..)</td>
</tr>
<tr>
<td>Lithography</td>
<td>Increase of area by 2.25 times requires high performance – high speed litho</td>
</tr>
<tr>
<td>Handling</td>
<td>Deformation (stress), transport issues, wafer translation</td>
</tr>
<tr>
<td></td>
<td>(large distances, acceleration and settling times increase, vertical drift along the wafer)</td>
</tr>
<tr>
<td>Metrology</td>
<td>Stages and handling, mapping capabilities, increase of area by 2.25 times requires high performance – high speed metrology (inspection), dimensional change due to thermal expansion coefficient, ..</td>
</tr>
<tr>
<td>Data Management</td>
<td>Amount of data, data quality, ..</td>
</tr>
</tbody>
</table>

### Diameter and Thickness Comparisons

<table>
<thead>
<tr>
<th>Diameter</th>
<th>Thickness</th>
<th>Area</th>
</tr>
</thead>
<tbody>
<tr>
<td>300 mm</td>
<td>775 µm</td>
<td>706 cm²</td>
</tr>
<tr>
<td>450 mm</td>
<td>925 µm</td>
<td>1589 cm²</td>
</tr>
</tbody>
</table>
450 mm Activities - Material

- Wafer Manufacturing
- Important Wafer Parameters
- Required Metrology
IMPORTANT WAFER PARAMETERS/CHARACTERISTICS

- Specified wafer parameters are:
  - Resistivity
  - Oxygen concentration
  - Bulk defects (dislocations, COP, swirl, …)
  - Surface defects (LLS, particles, PID, …)
  - Metal contamination (bulk, surface)
  - Local flatness
  - Global Flatness, Nanotopography
  - Edge profile
  - Roughness
  - Backside conditions

All parameters have to be verified by adequate metrology!
Example: Bulk wafer metrology

Grinded wafer

Polished wafer

SIRD: Scanning Infra Red Depolarization

Stress measurements
Example: Bulk wafer metrology

Grinded wafer

Polished wafer

Interferometer Measurement:
Total Thickness Variation: 1.4 μm
ULE: Two chuck design options

support at 3 points (Bessel's radius)

Massive chuck: 19 mm max. thickness (by mass constraint)

Light-weight chuck: 32 mm max. thickness
bore holes unsymmetric (below centerplane)

massive: OPD=1250 nm

light-weight: OPD=397 nm
**Objective:**

Draw metrology nearer towards the process, to reduce the time between process, measurement and corrective actions.

<table>
<thead>
<tr>
<th>Offline Metrology</th>
<th>Metrology tool apart from process tool</th>
<th>Long time between process and measurement</th>
</tr>
</thead>
<tbody>
<tr>
<td>Inline Metrology</td>
<td>Metrology tool attached to process tool</td>
<td>Measurement immediately before/after processing</td>
</tr>
<tr>
<td>In situ Metrology</td>
<td>Metrology tool integrated in process chamber</td>
<td>Measurement during processing</td>
</tr>
<tr>
<td>Virtual Metrology</td>
<td>Wafer parameters derived from tool parameters (process state, additional sensors) by using physical models or from upstream metrology</td>
<td>“Measurement” during processing</td>
</tr>
</tbody>
</table>
Virtual Metrology (VM)

**VM definition**

- Technology of prediction of post process metrology variables (either measurable or non-measurable) using process and wafer state information that could include upstream metrology and/or sensor data.

**VM benefits**

- Support or replacement of stand-alone and in-line metrology operations
- Support of FDC, run-to-run control, and PdM
- Improved equipment control for VM running on equipment level
- Improved understanding of unit processes
Latest Developments in Manufacturing Science
Virtual Metrology (VM)

Virtual Equipment test bench for development and test of VM models
- Utilization of history fab data
- Simulation of relevant equipment and process behaviour
- Application of noise, typical faults, and process drifts

Comparison of prediction error for different VM models
Latest Developments in Manufacturing Science
Virtual Metrology (VM)

Prediction of etch-depth in a trench etch process

- Objective: Establish wafer-fine run-to-run control in deposition, etch, CMP module

- Precise predictions of etch-depth in a trench etch process by VM
- Consideration of multiple products, etch chambers and recipes
Summary and Outlook

- Metrology is a non-productive step: ideally ZERO metrology
- BUT reality:
  - Increasing number of non-product wafers during
    - Process development
    - Pilot production
    - Transfer into high-volume manufacturing
  - New developments needed
  - Advanced strategies needed
  - Advances required by
    - Technology nodes
    - Wafer diameters
    - Quality improvements
Acknowledgment

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