Advanced Metrology for Understanding Charge Transport Phenomena in Charge Trap Flash Memory

2013. 3. 26

Gyeong-Su Park, Ph.D.

Samsung Master/AS Group Leader
Samsung Advanced Institute of Technology
Outline

◆ Si technology trend & issues for semiconductor analysis

◆ Nanometrology for understanding charge transport phenomena of CTF memory
  - Analysis of charge trap distribution & charge injection
  - Measurements of band structure & defect states
  - Analysis of charge loss

◆ New metrology for the study of charge transport phenomena
  - *In-situ* probing inside TEM

◆ Conclusion
System performance forecast in 2020

Performances increase 50 to 64 times

- **CPU**
  - '20: 4.6 TIPS
  - '15: 639 GIPS
  - '10: 88 GIPS

- **DRAM**
  - '20: 256 GB
  - '15: 32 GB
  - '10: 4 GB

- **Flash**
  - '20: 2 TB
  - '15: 256 GB
  - '10: 32 GB

- **Mobile Network**
  - '20: 5 Gbps
  - '15: 100 Mbps
  - '10: 100 Mbps

※ Peak data rate
# Key Issues for Semiconductor Analysis

<table>
<thead>
<tr>
<th>Key Issues</th>
<th>Present → 2020</th>
<th>Analytical Evolution</th>
</tr>
</thead>
<tbody>
<tr>
<td>① Critical Dimension</td>
<td>32 → 14nm (2D → 3D)</td>
<td>In Line Resolution ↑, 3D</td>
</tr>
<tr>
<td>② Equivalent Oxide Thickness (EOT)</td>
<td>12.6 → 5.3 Å</td>
<td>High Resolution, Bonding Structure, 3D</td>
</tr>
<tr>
<td>③ Junction Profile (# of Dopants)</td>
<td>6x10⁵ → 6x10⁴</td>
<td>3D, Sensitivity, Spatial Resolution</td>
</tr>
<tr>
<td>④ Strain</td>
<td>~1% → ~?</td>
<td>Nondestructive, Spatial Resolution</td>
</tr>
<tr>
<td>⑤ Contamination (Defect size)</td>
<td>23 → 5nm</td>
<td>Spatial Resolution, Sensitivity</td>
</tr>
</tbody>
</table>

**Analytical Evolution**

- Critical Dimension: From 32nm to 14nm, the critical dimension is reduced from 2D to 3D, improving in-line resolution.
- Equivalent Oxide Thickness: From 12.6 Å to 5.3 Å, the thickness decreases, enhancing high resolution and bonding structure aspects.
- Junction Profile: The number of dopants decreases from 6x10⁵ to 6x10⁴, improving 3D sensitivity and spatial resolution.
- Strain: The strain decreases from ~1% to ~?, allowing nondestructive spatial resolution.
- Contamination: The defect size decreases from 23nm to 5nm, improving spatial resolution and sensitivity.
### Key issues for semiconductor analysis

#### Key Issues Present → 2020 Analytical Evolution

<table>
<thead>
<tr>
<th></th>
<th>Key Issues</th>
<th>Present → 2020</th>
<th>Analytical Evolution</th>
</tr>
</thead>
<tbody>
<tr>
<td>6</td>
<td>DRAM - Capacitor (Aspect ratio)</td>
<td>25 → ≥ 80</td>
<td>In Line Structure Monitoring, Composition of Dielectric Material</td>
</tr>
<tr>
<td>7</td>
<td>Flash - Cell structure (# of stack)</td>
<td>Single → ≥ 128</td>
<td>Nondestructive, In line Structure Monitoring, Grain Structure</td>
</tr>
<tr>
<td>8</td>
<td>Mechanism for new materials &amp; devices</td>
<td>N/A → ReRAM, PRAM STT-MRAM etc.</td>
<td>In situ observation</td>
</tr>
</tbody>
</table>

- **High-k & Simple structure**
- **30nm**
- **ReRAM**
<table>
<thead>
<tr>
<th>Key Issues</th>
<th>Challenges</th>
</tr>
</thead>
<tbody>
<tr>
<td>① Critical Dimension</td>
<td>In line SEM with BSE, Electron tomography(3D)</td>
</tr>
<tr>
<td>② Equivalent Oxide Thickness (EOT)</td>
<td>High Resolution EELS, Atomic scale 3D imaging</td>
</tr>
<tr>
<td>③ Junction Profile (# of Dopants)</td>
<td>SPM-based dopant profile, Atom probe tomography</td>
</tr>
<tr>
<td>④ Strain</td>
<td>Off line : NBD, In line : TERS</td>
</tr>
<tr>
<td>⑤ Contamination (Defect size)</td>
<td>EDS with microcalorimeter</td>
</tr>
<tr>
<td>⑥ DRAM - Capacitor (Aspect ratio)</td>
<td>In line 3D analysis of morphology (SEM/Optical method?)</td>
</tr>
<tr>
<td>⑦ Flash - Cell structure (# of stack)</td>
<td>In line 3D, EBSD</td>
</tr>
<tr>
<td>⑧ Mechanism for new materials &amp; devices</td>
<td><em>in situ</em> SPM/TEM, Low voltage, high resolution TEM/STEM</td>
</tr>
</tbody>
</table>

* BSE : Backscattered secondary electron, NBD: Nano beam diffraction , TERS: Tip-enhanced Raman spectroscopy, EBSD: Electron backscatter diffraction
Outline

◆ Si technology trend & issues for semiconductor analysis

◆ Nanometrology for understanding charge transport phenomena of CTF memory
  - Analysis of charge trap distribution & charge injection
  - Measurements of band structure & defect states
  - Analysis of charge loss

◆ New metrology for the study of charge phenomena
  - *In-situ* probing inside TEM

◆ Conclusion
What is a CTF memory?

- **Advantages of CTF memory**: better scaling capability, higher logic compatibility, and lower programming voltage
- **TANOS device has difficulties in controlling the trap density & trap distribution** → Si-NC based CTF structure

![Samsung 32GB CTF](image)

**Program**

- Write (gate voltage > 0)
- Trap
- Electron
- Charge storage region (silicon nitride)

**Erase**

- Erase (gate voltage < 0)
- Trap
- Hole
- Charge storage region (silicon nitride)

- TANOS (TaN-Al₂O₃-Nitride-Oxide-Silicon)
Key issues for Si-NC distribution

- Single layer of Si-NCs embedded in SiNx has problems
  - increase of C/L & degradation of ERS property
  → double layer of Si-NCs is available to obtain high density of charge trapping and good charge retention

C/L: Charge Loss, ERS: Erase, DT: Direct Tunneling, HTS: Hot Temperature Storage
1 Analysis of charge trap distribution

- HR-TEM image of Si-NCs in Si$_N$$_x$ obtainable only when Si-NCs are crystalline and tilted to a strong Bragg condition

- To see Si-NCs in SiO$_x$ or SiN$_x$, energy-filtered image at 17 eV (plasmon loss for Si) is very useful

![Plasmon loss energy-filtered image](image)

- HR-TEM image (Si NC/SiOx): only a strong Bragg condition

- Plasmon energy-filtered image (Si NC/SiOx)

### Analysis of charge trap distribution

- **Plasmon tomography can measure the morphology & 3D distribution of Si-NCs**
  - Si-NC number density: layer A is higher than layer B
  - additional Si-NC layer C was formed
  - size of Si-NCs is about 3~5 nm, but the Si-NCs in layer C exhibit irregular shape

![Diagram showing cross-sectional and plane views of Si-NCS](image)

- **Shape of Si-NCs (3~5 nm)**
  - 1NC : 3~5 e-trap
Key issues for SiO$_2$/SiN$_x$ interface

Dilemma between P/E speed & charge loss

- **Imperfect P/E speed**
  - Slow carrier recombination velocity:
    - Increase of electron & hole trap in the SiN$_x$/SiO$_2$ interface by the defective structure
    - thick T$_{ox}$ (SiO$_2$) layer → use of SiON layer for the increase of hole tunneling

- **Charge loss through tunnel oxide (T$_{ox}$) in the same E-field**
  - Lower tunnel barrier:
    - Barrier height change due to the compositional changes in the SiN$_x$ layer
    - thin T$_{ox}$ (SiO$_2$) layer

![Relative Energy vs N concentration](image-url)

![Charge Loss Graph](image-url)
Analysis of interface trap & charge injection

- Interface structure: aberration-corrected STEM/EELS with 0.5 nm probe
  - Si/SiON interface with suboxide bonding (dangling bonding): ~1 nm

Atomic-scale interface (Si/SiON) structure analysis

Spatial resolution: 0.5 nm

Si

Dangling bond: ~1 nm
Analysis of interface trap & charge injection

- In-situ electron holography enables to confirm the charge trap in Si/SiNx interface & charge injection from Si-NCs
  - black contrast at three regions (c): trap in the double Si-NC layers and the Si/SiNx (SiO₂) interface
  - electron injection starts from ~ 22 V
  - FN tunneling across the tunneling oxide layer
Outline

◆ Si technology trend & issues for semiconductor analysis

◆ Nanometrology for understanding charge transport phenomena of CTF memory
  - Analysis of charge trap distribution & charge injection
  - Measurements of band structure & defect states
  - Analysis of charge loss

◆ New metrology for the study of charge phenomena
  - *In-situ* probing inside TEM

◆ Conclusion
Measurements of band structure & defect states

- Band-gap engineering of a-Si$_3$N$_4$ and SiO$_2$ films: measurements of band-gap, band offset, and defect state are necessary
  - bandgap: REELS, valence band offset: XPS/UPS, defect states: TSEE & DLTS

**Diagram Notes:**
- REELS: Reflection electron energy loss spectroscopy
- XPS: X-ray photoelectron spectroscopy
- TSEE: Thermally stimulated exo-electron emission
- DLTS: Deep level transient spectroscopy
Monochromated STEM-EELS
- Energy resolution of monochromated EELS (Titan + Monochromator + Tridiem 865 ER): 0.15 eV

Comparison AES-EELS and STEM-EELS
- AES-REELS $\rightarrow$ larger scan area & higher energy resolution than STEM-EELS, surface charging effect (weak point)
- STEM-EELS $\rightarrow$ difficulty in reading the onset depending on the sample thickness, and Cerenkov loss effect for insulator

STEM-EELS at various thickness: 300 keV for a SiO$_2$ thin film

AES-REELS: 1 keV for a SiO$_2$ thin film

JC Park & G-S Park, Ultramicroscopy 109 (2009)
Bandgap of $a$-SiNx layers depending on the compositions

- as the nitrogen content increases, the bandgap energy of SiNx layer also increases
- small difference in the bandgap values between two metrology methods

<table>
<thead>
<tr>
<th></th>
<th>N</th>
<th>Si</th>
<th>N/Si</th>
</tr>
</thead>
<tbody>
<tr>
<td>SiNx1</td>
<td>59.1</td>
<td>40.9</td>
<td>1.46±0.07</td>
</tr>
<tr>
<td>SiNx2</td>
<td>54.5</td>
<td>45.5</td>
<td>1.20±0.06</td>
</tr>
<tr>
<td>SiNx3</td>
<td>47.9</td>
<td>52.1</td>
<td>0.92±0.05</td>
</tr>
</tbody>
</table>

Compositions of SiNx estimated by RBS
Outline

◆ Si technology trend & issues for semiconductor analysis

◆ Nanometrology for understanding charge transport phenomena of CTF memory
  - Analysis of charge trap distribution & charge injection
  - Measurements of band structure & defect states
  - Analysis of charge loss

◆ New metrology for the study of charge phenomena
  - *In-situ* probing inside TEM

◆ Conclusion
Key issues for blocking oxide (Box) layer

Retention/endurance: back tunneling & charge loss

- **Lower barrier height between CTL and Box layer**
  - Interface diffusion (Al, Si), Al$_2$O$_3$ structure (Eg)

- **Trap in Box layer**
  - Density of dangling bond
  - Trap energy level

![Graph showing retention/endurance characteristics](image)
5 Analysis of charge loss: SiNx/AIO interface

- **STEM-EELS in the SiNx/AIO(ALD) interface**
  - oxidation of SiNx generates silicon oxynitride (SiON) layer in the interface
  - SiON layer induces back tunneling by the conduction band offset of Box (AIO) layer
  - clean interface (SiNx/AIO) structure is required to reduce the retention & endurance problems
5 Analysis of charge loss: AlO layer

- Crystal structure of thin Al₂O₃ (Box) layer
  - wide-bandgap alumina (AlO) is desirable as the Box: $\alpha$-Al₂O₃ $\rightarrow$ 8.8 eV, $\gamma$-Al₂O₃ $\rightarrow$ 6.6~7.0 eV
  - NED/EELS results: $\gamma$-Al₂O₃ phase

(a) HR-TEM image
(b) Electron probe image
(c) NED

(d) Intensity profile of NED shown in (c)

(e) Core-EELS spectra in A

γ-alumina (cubic)
5 Analysis of charge loss: AlO layer

- **Eg and defect density of thin Al$_2$O$_3$ (Box) layer**
  - Eg of γ-Al$_2$O$_3$: 7.0 eV
  - Dangling bond density of γ-Al$_2$O$_3$ measured at 15 K → as-depo:1200 °C = 100:72.8 (27.2% ↓)

(a) XRD for the ALD grown-Al$_2$O$_3$ films

(b) REELS: bandgap

(c) ESR (Electron spin resonance)
Outline

◆ Si technology trend & issues for semiconductor analysis

◆ Nanometrology for understanding charge transport phenomena of CTF memory
  - Analysis of charge trap distribution & charge injection
  - Measurements of band structure & defect states
  - Analysis of charge loss

◆ New metrology for the study of charge transport phenomena
  - *In-situ* probing inside TEM

◆ Conclusion
**In-situ probing inside TEM**

- **SAIT TEM/TEM (Titan 300 kV, FEI)**
  - monochromated EELS: 0.15 eV, Cs-corrected STEM image: 0.8 Å
  - Piezo motor: fine displacement of probe $\rightarrow$ 0.2 nm
  - Bias modulation (<140 V)
  - High power, tunable laser irradiation ($\sim$150 mW, $\lambda$ : 400~800 nm)
**In-situ** probing inside TEM: core-shell NW (Ex. 1)

- **Electron transport properties of the core-shell (SRO/SiO$_2$) nanowire**
  - before Si nanodot formation: broad bump in current $\rightarrow$ electron accumulation in the NW
  - after Si nanodot formation (e-beam irradiation at 25 A/cm$^2$ for 5 min) : staircase-like behavior $\rightarrow$ Coulomb blockade effects

![Original SRO/SiO$_2$ nanowire (A)](image1)

![SRO/SiO$_2$ nanowire after Si Nandot formation (B)](image2)

![Graphs showing current-voltage characteristics](image3)
Mechanism for New Devices

- *In situ* / atomic scale analysis is essential to understand switching mechanism of new devices.

**ReRAM**
- Understanding of oxygen vacancy path of Ta$_2$O$_{5-x}$ in real time, different from existing memory mechanism.

**PRAM**
- Finding of the phase change mechanism between amorphous and crystalline GST.

**Graphene**
- Need for understanding of surface oxidation-reduction mechanism in atomic level.
**In-situ probing inside TEM: nanofilaments (Ex. 2)**

- **Direct measurements of I-V scan on nanofilaments**
  - HRTEM, SAED pattern, and FFT diffractogram confirm the Magnéli structure of a grain
  - Conductivity ratio \((\text{Ti}_4\text{O}_7/\text{TiO}_2)\) : \(\sim 1,000\)
  - Resistive switching mechanism in TiO\(_2\) thin film can be directly confirmed

Identification of Ti\(_4\)O\(_7\) (magnéli) structure

Outline

◆ Si technology trend & issues for semiconductor analysis

◆ Nanometrology for understanding charge transport phenomena of CTF memory
  - Analysis of charge trap distribution & charge injection
  - Measurements of band structure & defect states
  - Analysis of charge loss

◆ New metrology for the study of charge transport phenomena
  - *In-situ* probing inside TEM

◆ Conclusion
Conclusion

Developments of advanced analytical techniques for unveiling the nature of charge transport phenomena are essential to accomplish high performance nonvolatile CTF memories.

We introduced potential analytical approaches for examining the charge trapping, charge injection, and charge loss phenomena in Si nanocrystal-based CTF memory.

Charge trap distribution and charge injection behaviors in the Si NC-based memory can be analyzed, with plasmon tomography, aberration-corrected STEM/EELS, and in situ electron holography.

Recently developed REELS, monochromated STEM-EELS, TSEE, DLTS, and ESR methods allow the measurements of the bandgap, defect states, and defect density for the Tox layer, CTL, and Box layer with higher accuracy.