Overview of Next Generation Lithography, Advanced Patterning, EUV and Self Assembly

2013 International Conference on Frontiers of Characterization and Metrology
Gaithersburg, Maryland

Mark Neisser & Stefan Wurm
SEMATECH
March 28, 2013
INTRODUCTION
### ITRS Roadmap Requirements

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Minimum critical level half pitch</td>
<td>20</td>
<td>18</td>
<td>17</td>
<td>15</td>
<td>14</td>
<td>13</td>
<td>12</td>
<td>11</td>
<td>10</td>
<td>9</td>
<td>8</td>
</tr>
<tr>
<td>Minimum hole dimension</td>
<td>32</td>
<td>28</td>
<td>25</td>
<td>23</td>
<td>20</td>
<td>18</td>
<td>16</td>
<td>14</td>
<td>13</td>
<td>11</td>
<td>10</td>
</tr>
<tr>
<td>LWR</td>
<td>2.5</td>
<td>2.2</td>
<td>2.0</td>
<td>1.8</td>
<td>1.6</td>
<td>1.4</td>
<td>1.3</td>
<td>1.1</td>
<td>1.0</td>
<td>0.9</td>
<td>0.8</td>
</tr>
<tr>
<td>Minimum patterned defect size</td>
<td>20</td>
<td>20</td>
<td>20</td>
<td>10</td>
<td>10</td>
<td>10</td>
<td>10</td>
<td>10</td>
<td>10</td>
<td>10</td>
<td>10</td>
</tr>
<tr>
<td>Overlay</td>
<td>6.4</td>
<td>5.4</td>
<td>4.8</td>
<td>4.2</td>
<td>3.8</td>
<td>3.4</td>
<td>3.0</td>
<td>2.7</td>
<td>2.4</td>
<td>2.1</td>
<td>1.9</td>
</tr>
<tr>
<td>Minimum hole CD uniformity</td>
<td>1.2</td>
<td>1.0</td>
<td>0.8</td>
<td>0.6</td>
<td>0.5</td>
<td>0.5</td>
<td>0.4</td>
<td>0.4</td>
<td>0.3</td>
<td>0.3</td>
<td>0.3</td>
</tr>
<tr>
<td>Double patterning CD uniformity</td>
<td>0.6</td>
<td>0.4</td>
<td>0.3</td>
<td>0.3</td>
<td>0.3</td>
<td>0.2</td>
<td>0.2</td>
<td>0.2</td>
<td>0.2</td>
<td>0.2</td>
<td>0.2</td>
</tr>
<tr>
<td>Spacer defined CD uniformity</td>
<td>0.4</td>
<td>0.3</td>
<td>0.3</td>
<td>0.3</td>
<td>0.3</td>
<td>0.2</td>
<td>0.2</td>
<td>0.2</td>
<td>0.2</td>
<td>0.2</td>
<td>0.2</td>
</tr>
</tbody>
</table>
Conventional Lithography

- Improve Resolution by:
  - Shorter Wavelength
  - Higher NA
  - Improved tolerances and processing ($k_1$)

- But!
- Can’t go below $k_1 = 0.25$ in a single exposure (all light will diffract outside the lens)

Physics limits resolution

$$NA = \sin \theta$$

$$\text{resolution (half pitch)} = k_1 \frac{\lambda}{NA}$$
Improvement through Litho Wavelength and NA
(Historical data per Burn Lin)

Exposure Wavelength (nm)

Resolution range (nm)

G Line
I Line
Deep UV (KrF)
ArF
Dry
Immersion
Immersion and DP
In Production
In Development
EUV
EUV and DP

March 28, 2013
Improvement of $k_1$

- Better exposure tool tolerances
  - Aberrations
  - Flare
  - Control of wafer plane
  - Scan accuracy
  - Etc.

- Improvement of processing
  - Better resolving photoresists
  - Anti-reflective coatings
  - Planarized substrates
  - Ancillary coatings

- The $k_1$ resolution limit for single patterning with ArF immersion lithography is 36nm for 1.35 NA exposure tool (the highest NA available)

- Pitch Multiplication is used to go past this limit
The Aerial Image View Today
(with dipole illumination for 43nm)

Significant Material Improvement!

Image-able with today’s resists and processes

March 28, 2013
Metrology Challenges for Extending Conventional Lithography

- CD measurement including sidewall and profile
- LWR
- Overlay
  - Normally measured optically
  - Need accuracy with optics for <3 nm overlay budget
- Defects
  - Some specifications reflect tool capability rather than need.
DOUBLE AND MULTIPLE PATTERNING
Self Aligned Double Patterning (SADP) -- Pitch multiplication by process

- One exposure with substantial extra processing turns edges into lines and doubles the pitch
- Pattern types that can be produced after doubling are very limited
- Can come close to doubling the pitch. In practice, gives a 30% reduction in pitch (about one semiconductor generation’s worth).
Double Patterning -- Two exposures

- Two exposure used giving twice the information through the lens
- Pattern types that can be produced are more flexible than SADP, but still need complicated design
- Can come close to doubling the pitch. In practice, gives a 30% reduction in pitch (about one semiconductor generation’s worth).
Double Exposure Design Issues

- 1 D type designs split into two exposures easily

- 2 D type designs can be impossible and require design change
Multiple Patterning (MP)

• Needed for half pitches below roughly 22nm if ArF immersion lithography is to be extended

• Requires “Double” Double patterning
  – Many process options
  – All potential processes complicated and expensive processes

• Expect substantial design restrictions

• Overlay still shrinks with final feature size
  – Many more overlay parameters for multiple patterning
  – Interaction between CDs and OL
Triple Patterning Using Spacers

1. Resist-1 image (not shown) is used to delineate the spacer host pattern.
2. Conformable coating & anisotropic etching produce sidewall spacers.
3. Resist-2 image protects selected spacers.
4. Resist-3 image is the etch mask for features larger than the spacer width.
5. Final pattern from hardmask that was delineated with the composite spacer and resist-3 images.
Inspection Challenges with Multiple Patterning

• Many more targets per layer (3 to 6X)

• Exposure 2 to exposure 1 metrology

• Confounding of overlay and CD error

• Multiple CD distributions
EUV
Suppliers execute against roadmap

**EUV Product Roadmap**

**ADT**
- Resolution = 32 nm
- NA = 0.25, σ = 0.5
- Overlay < 7 nm
- Throughput 5 WPH @ 5mJ/cm² ~8W

**NXE:3100**
- Resolution = 27 nm
- NA = 0.25, σ = 0.8
- Overlay < 4.5 nm
- Throughput 60 WPH @ 10mJ/cm² >100W

**NXE:3300B**
- Resolution = 22 nm
- NA = 0.32, σ = 0.2-0.9
- Overlay < 3.5 nm
- Throughput 125 WPH @ 15mJ/cm² >350W

**NXE:3350C**
- Resolution = 16 nm
- NA = 0.32, OAI
- Overlay < 3 nm
- Throughput 150 WPH @ 15mJ/cm² >550W

**Main improvements**
1) New EUV platform :NXE
2) Improved low flare optics
3) New high σ illuminator
4) New high power LPP source
5) Dual stages

**Main improvements**
1) New high NA 6 mirror lens
2) New high efficiency illuminator
3) Off-Axis illumination option
4) Source power increase
5) Reduced footprint

**Platform enhancements**
1) Source power increase

* Requires <7nm resist diffusion length

ASML Roadmap, SPIE 2010
EUV Lithography Exposure System

- All Reflective Optics
- Optical train is in a vacuum
• Resolution of EUV has improved over time, both through resist and imaging tool improvements
EUV Metrology Challenges

• Same ones as for optical extensions
  – CD measurement including sidewall and profile
  – LWR
  – Overlay
  – Defects

• Plus:
  – Actinic substrate, blank, and mask inspection during mask manufacture
  – Defect review after mask cleaning
Typical current EUV mask structure

Patterned Absorbers
~ 50 to 70 nm thick
(typically Cr or TaN)

Ruthenium cap
2.5 nm thick

Reflective Multilayers
~ 280 nm thick
(Mo/Si pair = 7nm)
40 Pairs
Hard EUV Mask Blank Challenges

Substrate and Blank

• Absorber/ARC Stack
  – Optical Properties at EUV
  – Properties at Inspection Wavelengths
  – Particle Defects
  – Etch Performance

• Ru Cap
  – Particle Defects
  – Film Loss from Etch
  – Metrology

• Multilayer
  – Particle Defects
  – Uniformity
  – Reflectivity and Centroid Wavelength
  – Metrology (Defect Detection)

• Substrate
  – Thermal Properties
  – Particle and pit defects
  – Subsurface polishing damage
  – Flatness and Surface Roughness
  – Metrology (Defect Detection)

• Backside Coating
  – Electrical Properties
  – Defectivity

This is difficult!
EUV Mask Blank Defects and their Repair

Phase defect wafer plane image
Amplitude defect wafer plane image

Phase defect repair technique
Local thermal source (electron beam)

b) Phase defect
Mo/Si
Substrate

Amplitude defect repair technique
Remove damaged top layers locally with a FIB

b) Amplitude defect
Mo/Si
Substrate

Graphics courtesy to S.P. Hau-Riege, Lawrence Livermore National Labs
EUV Actinic Inspection issues

- Buried defects in masks and optics need actinic inspection to detect
  - Light sources are dim and give slow inspection
  - Defects much smaller than printed feature size can give unacceptable patterning

- Mask layers require atomic level precision
  - Pits and bumps in the substrate must be found and repaired or avoided
  - Flatness and smoothness of substrates are also issues

- Chemical nature of particles can matter
• Progress has been made but more progress is needed.
  – Defects come from both the mask substrate and from layer depositions
Need for Regular Mask Cleaning

- Pellicle for ArF lithography means small particles aren’t imaged.
- Lack of pellicle for EUV means very small particles are problems.
SELF ASSEMBLY
Block Copolymer Self-Assembly for Holes

- Polymer chains have “blocks” of each monomer
- Volume ratio of monomers drives the shape of the phase domains
- Overall polymer MW drives size of domains
Block Copolymer Morphologies

Phase diagram depends on molecular weight (number of molecules $N$) and strength of interaction ($\chi$ factor).

- Cylinder phase structures look similar to lithographic contact holes.
- Lamellar phase looks similar to lithographic line and space structures.

Mean field phase diagram for binary BCP

Thermodynamic driving force for phase separation of polymers

\[
\frac{\Delta G_{\text{mix}}}{kT} = \frac{f_A}{N_A} \ln(f_A) + \frac{f_B}{N_B} \ln(f_B) + f_A f_B \chi
\]
The Question: How Can We Make The BCP Phases Lithographically Useful?

The Answer: **Directed Self-Assembly**

- **Top-down** Lithographically patterned substrate
  - Sparse pattern = easy lithography
  - Limited spatial resolution
  - Large CD variation

- **Bottom-up** Self-assembling material
  - CD built into BCP material
  - High spatial resolution
  - No placement control

- **Directed Self-assembly**
  - High resolution pattern with easy lithography
  - Enhanced resolution
  - Reduced CD variation

March 28, 2013
Both types of directed self assembly can also be used for contact holes.
DSA Metrology Challenges

- Assembled Patterns are solid blocks of materials
  - Need inspection before etch
  - Three dimensional structure of the blocks is important
  - How to measure solid phase boundaries?

Conventional Resist

Assembled Block CoPolymer

Photoresist

Air

Block A

Block B
DSA Metrology Challenges

- Actual shape can be different from simple block diagram

Block Diagram

Example of Actual Shape
(per Small Angle X-ray Scattering (SAXS) done at NIST)

Actual Etched Shape

26.5nm Height

25nm Pitch
Simulated Good and Bad Annealed Structures -- how to tell the difference from above?

- Alignment features of incorrect size
- Alignment features of correct size

Work published by P. Nealey/J. DePablo
Other DSA Metrology Issues

• Overlay of annealed phases
  – Pitch multiplication results in several or more features spontaneously forming during anneal some distance for the guiding feature.
  – The exact position may vary with respect to guiding feature
  – This can be called “pattern registration”

• CD control
  – Need to check CDs before etching

• Defects
  – Defects could be buried
  – Defects that require rework could be present in annealed phase
  – Conceivably, defects in surface energy of the substrate could make be a problem, even without a physical particle

• The generally small size of the features is intrinsically hard to measure
OTHER ADVANCED PATTERNING APPROACHES
E Beam Direct Write

- Focused beam of electrons is scanned in a way to create the desired pattern in resist without a reticle
  - Has throughput issues
  - Difficult to scale to smaller sizes without losing throughput
- Tools are not available yet, but two companies are working on them
  - Each has multiple beams for writing
  - Scaling will require more and more beams
- Same metrology issues as conventional lithography except:
  - Every wafer probably needs much more inspection for defects and missing features
  - This is because there is no mask that can be inspected in advance
Nanoimprint

- A kind of microstamping and cure process
  - Uses a master template to make replicates
  - Replicates are used for wafer printing and then discarded
  - Masters and replicates are 1X, which makes them hard to make to spec.

- Tools are available for development work
  - Some work being done for disk drive master preparation
  - Some tools are used for semiconductor testing

- This is a contact printing technique
  - Physical contact creates worries about defects
  - The accumulation of particles over time needs to be worked on

- Wafer metrology similar to that of conventional metrology

- “Mask” Metrology is different, but doable
  - The masks 3-D template so position, size and depth have to be inspected
  - Mask vendor claims good progress on this
Conclusions

• Standard single exposure lithography with ArF does not meet future industry needs.

• The smaller and smaller size of the pattern creates metrology challenges just by itself

• All possible options for future patterning create additional metrology challenges
Acknowledgements

• Our thanks to Alain Diebold and Ralph Dammel for inputs