Characterization of Si/SiGe Heterostructures for Strained Si CMOS


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- Introduction
  why strained Si devices?

- Layer structures for strained Si CMOS
  graded buffer layers
  alternative approaches to relaxed SiGe
  SiGe-on-insulator and strained Si-on-insulator

- Nondestructive characterization of strained Si-on-SiGe structures
  thermal stability of strained Si on SiGe

- Conclusions
Strained Si Device Structures

modified band structure of Si under biaxial tensile strain ==> enhanced mobility

need relaxed Si$_{1-x}$Ge$_x$ with 0.15$<x<$0.35
Enhanced Mobility in Strained Si Devices

- Electron mobility is
  - 70% higher in $\text{Si}_{0.87}\text{Ge}_{0.13}$
  - 110% higher in $\text{Si}_{0.72}\text{Ge}_{0.28}$
  higher than theory predicted!

- Peak hole mobility is enhanced in $\text{Si}_{0.72}\text{Ge}_{0.28}$ and $\text{Si}_{0.65}\text{Ge}_{0.35}$
  but decreases at higher electric field

K. Rim, et al., ISTDM, Nagoya, Japan, January 15-17, 2003
Epitaxial SiGe Layers on Si(001)

Pseudomorphic layer:
in-plane: \( a_{\parallel} = a_{\text{Si}} \)
out-of-plane: \( a_{\perp} > a_{\text{SiGe}} \)

Partially relaxed layer:
\( a_{\text{Si}} < a_{\parallel} < a_{\text{SiGe}} \)
\( a_{\perp} > a_{\text{SiGe}} \)

100\% relaxed layer:
\( a_{\parallel} = a_{\perp} = a_{\text{SiGe}} \)
Strain Relaxation via $60^\circ$ Misfit Dislocations

misfit segment formed by glide of an existing dislocation
e.g. Si on relaxed SiGe


nucleation of a dislocation during epitaxial growth
e.g. SiGe on Si substrates


must minimize threading dislocation density for devices!
Compositionally Graded SiGe Buffer Layers for Devices

**Advantages:**
- Low threading dislocation densities \(10^5 - 10^8 \text{ cm}^{-2}\)
- Lower grading rates (thicker layers) \(\Rightarrow\) lower defect density

**Disadvantages:**
- Very thick SiGe layers (1-4 \(\mu\text{m}\))
  - Expensive
  - Poor heat conductivity
- Rough surface (cross hatch)
  - Can polish surface (CMP)
- Inhomogeneous distribution of threading dislocations

**Diagram:**
- Strained Si cap layer
- Uniform \(\text{Si}_{1-x}\text{Ge}_x\) layer
- Graded \(\text{Si}_{1-x}\text{Ge}_x\) layer
- Si substrate

Misfit dislocation network buried below devices

\(20 \mu\text{m} \times 20 \mu\text{m} -- \text{Si}_{0.85}\text{Ge}_{0.15}\)

Z-range = 40 nm, RMS = 6 nm
Thin Relaxed SiGe Layers on Si(001)

Alternatives to thick graded buffer layers:

-- Grow Si layer at low temperature underneath SiGe (MBE)
  "compliant layer" - high density of point defects in LT Si layer

-- Ion implantation of H or He
  extended defects (bubbles) formed during high temperature
  annealing in implanted wafer act as nucleation sources for
  dislocations
3 step process:

- grow 50-300 nm pseudomorphic (fully strained) SiGe layer on Si

- implant He\(^+\) at various doses and energies, \(R_p\) at or below SiGe/Si interface

- anneal at \(T>700\) °C depending on implant conditions platelets or bubbles form which are nucleation sources for misfit dislocations
Strain Relaxation by X-Ray Diffraction

188 nm-thick $\text{Si}_{0.8}\text{Ge}_{0.2}$

Intensity (cts/sec) vs. Bragg Angle (deg.)

Annealed 80% relaxed

He$^+$ implanted

As-grown

He$^+$ implantation enhances strain relaxation

% Relaxed vs. SiGe Layer Thickness (nm)

$x=0.15$

$x=0.20$

Solid: He implant
Open: no implant
Strain Relaxation Mechanisms

strain relaxation mechanism varies with implant conditions

Characterization of Implanted/Annealed Buffer Layers

AFM image of wafer surface
256 nm-thick Si$_{0.8}$Ge$_{0.2}$ layer
84% strain relaxation
RMS roughness = 0.52 nm

planar view TEM image of a 250 nm-thick, 80% relaxed Si$_{0.85}$Ge$_{0.15}$ layer
(arrow indicates a threading dislocation)
- threading dislocation density $<5\times10^7$ cm$^{-2}$
- defects are homogeneously distributed
SiGe-on-insulator (SGOI) substrates

Combine advantages of strained Si with SOI technology

Various approaches to get SGOI

-- oxygen implantation into thick relaxed SiGe buffer layer

-- high temperature annealing/oxidation of SiGe

-- wafer bonding and layer transfer methods
Wafer Bonding and Layer Transfer Process

L.J. Huang, et al., 2001 Symposium on VLSI Technology

1. H implantation
   - Relaxed Si$_{1-x}$Ge$_x$
   - Si substrate

2. Handle wafer
   - 300 nm LTO
   - Relaxed Si$_{1-x}$Ge$_x$
   - Bonding interface
   - H implant peak
   - Misfit dislocations

3. Handle wafer
   - 300 nm LTO
   - Transferred relaxed Si$_{1-x}$Ge$_x$
   - Bonding interface
   - Misfit dislocations

4. Strained Si
   - Si$_{1-x}$Ge$_x$ buffer
   - Transferred relaxed Si$_{1-x}$Ge$_x$
   - 300 nm LTO
   - Handle wafer

Layer splitting

Epi growth
Bonded SGOI Wafers

SGOI wafer

SiGe (15% Ge)

SiO₂

Si substr.

n-MODFET layer structure

device layers

SGOI substr.

- Successful layer transfer

- High quality epitaxial growth on SGOI
- Electron mobility same as on bulk Si

J.O. Chu, et al., Spring 2001 MRS Meeting, San Francisco
Bonded SSOI Wafer

need strained Si on oxide for future CMOS

(TEM -- J.A. Ott)
Thermal Stability of Strained Si/SiGe Structures

- high resolution x-ray diffraction (synchrotron source)
- planar view TEM
- Raman spectroscopy (Koester, et al., APL 72, 2148 (2001))
- spectroscopic ellipsometry

Is strained Si stable at device processing temperatures?

- rapid thermal annealing at 1000 °C for 5-300 sec.

- alloy composition, 0.19<x<0.30
- cap thickness, 7-21 nm
X-Ray Diffraction Measurements

-- triple-axis configuration, NSLS (X20), Brookhaven National Lab
-- 004 and 224 reflections to get composition and strain of Si$_{1-x}$Ge$_x$ layer
-- 004 data to get thickness and strain of Si cap layer

removed cap layer from some areas
took data from areas with/without Si layer

peak shift ==> strain in Si cap layer
fringe spacing ==> Si layer thickness

XRD Results for Annealed Wafer

- 21 nm strained Si/relaxed Si$_{0.72}$Ge$_{0.28}$

*Note that peak shifts towards Si substrate peak and fringe spacing increases with increased annealing time*

*$\Rightarrow$ interdiffusion at interface and strain relaxation occur*
Interdiffusion at Si/SiGe Interface -- X-ray

Si$_{1-x}$Ge$_x$
0.19$<x<$0.28

Initial cap thickness
14-23 nm

--- cap thickness decreases by 2 nm (+/-1.5 nm) after 30 sec.
--- no significant dependence on alloy composition or thickness over the ranges investigated!
Strain Relaxation (XRD and TEM)

-- strain relaxation expressed as percent of initial strain
-- good agreement between x-ray and TEM results
-- relaxation behavior as predicted by Matthews & Blakeslee
-- little strain relaxation occurs, but misfit dislocations are formed at Si/SiGe interface when Si layers exceed critical thickness
Planar View TEM Analysis

- look at near-surface region of the sample
- image misfit dislocations at Si/SiGe interface

21 nm Si cap / Si$_{0.72}$Ge$_{0.28}$, 1000 °C 30 sec average misfit dislocation spacing is 2.5/μm
Si-Si LO phonon peaks fit using double Lorentzian line shape.

- Renishaw 2000 Confocal Raman Microprobe at Miami University, Ohio,
- 488 nm excitation wavelength, 3600 mm\(^{-1}\) grating density,
- 4 mW incident power at sample.

Si\(_{1-x}\)Ge\(_x\) layer
Si cap layer

Si-Si LO phonon peaks fit using double Lorentzian line shape.
Determination of Si Thickness Change with Raman

Ratio of SS and SiGe peak areas used to determine thickness of Si cap. Use HRXRD value for as-grown sample as calibration.

\[ \Delta d_{1}(t) = d_{Si}(0) \cdot \left[ 1 - \frac{r(t)}{r(0)} \right] \]

where, \[ r(t) = \frac{A_{1}(t)}{A_{2}(t) + A_{1}(t)} \]

Determined value of \( d_{Si}(0) \) using HR-XRD.
Comparison of XRD and Raman Results

Average values of many samples are plotted for each method.

good agreement!

XRD values of initial layer thickness used to calibrate Raman data (488 nm)

Error bar is +/-1.5 nm for XRD and +/- 2 nm for Raman
Raman Data: Different Wavelengths

Si layers of different thickness on $\text{Si}_{0.77}\text{Ge}_{0.23}$

more surface sensitive at shorter wavelength

$\Rightarrow$ can detect thinner strained Si layers on SiGe layers with lower Ge
Comparison of Raman Results (442 nm) with SIMS Data

A: 31 nm Si on Si$_{0.77}$Ge$_{0.23}$
B: 18 nm Si on Si$_{0.70}$Ge$_{0.30}$

- data are consistent with earlier results
- scatter is within accuracy of measurements

SIMS confirms that Si thickness changes by interdiffusion!
Limitations of Two-Layer Assumption

- Simulated three-layer structure, but fit with double Lorentzian.

- Varied $d_{\text{int}}$, while keeping $d_{\text{Si}}$ constant. Compared extracted and input values.

- Increaseing $d_{\text{int}}$ causes Si peak to shift, broaden, and increase in area.

- Si thickness error > 5% when $d_{\text{int}}/d_{\text{Si}} > 0.67$. All samples in this study have $d_{\text{int}}/d_{\text{Si}} < 0.50$. 

![Graph showing extracted peak shift and extracted $d_{\text{Si}}$ values against $d_{\text{int}}/d_{\text{Si}}$.]
Raman Measurement of Strain in Si Layer

relaxation of strained Si-on-SiGe

strained Si-on-insulator

- Uncertainty in Raman data too large to detect the small degree (<5%) of strain relaxation in Si/SiGe samples!


- Strained Si layer transferred by wafer bonding
- Compare strained Si layer with bulk Si
- Si layer remains strained after annealing

Spectroscopic Ellipsometry

- proven method for characterization of dielectric films
- best results when there is a significant difference in $k$ and $n$ between materials
  e.g. oxide or nitride on Si, SOI, SGOI, SSOI
- requires many parameters to model structures having several layers
  need good values for optical constants for each material

- useful for thickness of strained Si on relaxed SiGe??
- poor results for graded buffer layers -- better for strained Si layer than for SiGe
  surface/interface roughness?
  poor optical data for dislocated SiGe layers?
- reasonable results for strained Si on implanted/annealed buffer layers
  example: - TEM 7.2 nm
  - XRD 7.9 nm agreement is within uncertainty
  - ellipsometry 6.5 nm of XRD measurement!

- what accuracy is needed??
Conclusions

Enhanced electron and hole mobility in strained Si devices demonstrated
-- standard fabrication processes, 200 mm wafers

Materials/Structures
-- graded buffer layers are standard
  >90% relaxation at any alloy composition
-- implanted/annealed buffer layers
  thinner/smoothers surfaces than graded layers
-- insulator substrates fabricated by wafer bonding methods
  SGOI and SSOI

Nondestructive characterization methods
-- x-ray diffraction good for composition/strain of SiGe layers,
  but strained Si cap layer is difficult
-- Raman spectroscopy is good for strain in SSOI, but strained
  Si on SiGe is difficult & need calibration to measure Si thickness
-- spectroscopic ellipsometry useful to measure layer thickness
  for SGOI and SSOI -- further work needed for structures with
  many layers, but likey to be useful for strained Si on SiGe