Metrology Challenges Associated With Gate Dielectric Scaling, Including the Vertical, Replacement-Gate MOSFET

Don Monroe
Jack Hergenrother
Rafi Kleiman
Outline

• Drivers for scaling
• Scaled gate oxide
• High-$\kappa$ gate dielectrics
• Replacement gate processes
• Vertical Replacement Gate
Outline

• Drivers for scaling
  – Density
  – Performance
  – Recent history: hyperscaling of gate oxide and gate length

• Scaled gate oxide
• High-k gate dielectrics
• Replacement gate processes
• Vertical Replacement Gate
Why Scale $T_{ox}$?

1. Better gate control of channel
   - thinner $T_{ox}$ helps for shorter gates
   - other “knobs” available

2. Increased drive through $C’_{ox}$

\[
\eta = \frac{C’_{ox}W}{C’_{ox}W + C_{ext}}
\]

Gate-loaded circuits ($\eta \sim 100\%$)
- no speed improvement

Interconnect-loaded circuits ($\eta << 100\%$)
- big speed improvement
  - But we could have scaled width $W$!
## 1999 ITRS*

**Memory and Logic Technology Requirements -- Near Term**

<table>
<thead>
<tr>
<th>YEAR TECHNOLOGY NODE</th>
<th>1999 180 nm</th>
<th>2000</th>
<th>2001</th>
<th>2002 130 nm</th>
<th>2003</th>
<th>2004</th>
<th>2005 100 nm</th>
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</thead>
<tbody>
<tr>
<td>MPU GATE LENGTH (nm)</td>
<td>140</td>
<td>120</td>
<td>100</td>
<td>85</td>
<td>80</td>
<td>70</td>
<td>65</td>
</tr>
<tr>
<td>Minimum Logic Vdd (V) (desktop)</td>
<td>1.5-1.8</td>
<td>1.5-1.8</td>
<td>1.2-1.5</td>
<td>1.2-1.5</td>
<td>1.2-1.5</td>
<td>0.9-1.2</td>
<td>0.9-1.2</td>
</tr>
<tr>
<td>$T_{ox}$ equivalent (nm)</td>
<td>1.9-2.5</td>
<td>1.9-2.5</td>
<td>1.5-1.9</td>
<td>1.5-1.9</td>
<td>1.5-1.9</td>
<td>1.2-1.5</td>
<td>1.0-1.5</td>
</tr>
<tr>
<td>Nominal $I_{on}$ @ 25°C ($\mu$A/$\mu$m) [NMOS/PMOS] high performance</td>
<td>750/350</td>
<td>750/350</td>
<td>750/350</td>
<td>750/350</td>
<td>750/350</td>
<td>750/350</td>
<td>750/350</td>
</tr>
<tr>
<td>Maximum $I_{off}$ @ 25°C ($\mu$A/$\mu$m) [NMOS/PMOS] high performance</td>
<td>5</td>
<td>7</td>
<td>8</td>
<td>10</td>
<td>13</td>
<td>16</td>
<td>20</td>
</tr>
<tr>
<td>Percent static power reduction necessary due to innovative circuit/system design</td>
<td>0</td>
<td>33</td>
<td>48</td>
<td>55</td>
<td>71</td>
<td>77</td>
<td>81</td>
</tr>
</tbody>
</table>

*International Technology Roadmap for Semiconductors December 1999*

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Difficult Challenge (before 2005): “Production worthy high k dielectrics and compatible gate materials will not be available.”
Moore Plot of Moore’s Law

Predicted gate oxide thickness, $T_{ox}$, in 2001

Year of Roadmap


Predicted gate oxide thickness, $T_{ox}$, in 2001
## 1999 ITRS*

*International Technology Roadmap for Semiconductors*

December 1999

<table>
<thead>
<tr>
<th>YEAR TECHNOLOGY NODE</th>
<th>2008 70 nm</th>
<th>2011 50 nm</th>
<th>2014 35 nm</th>
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<tbody>
<tr>
<td>MPU GATE LENGTH (nm)</td>
<td>45</td>
<td>32</td>
<td>22</td>
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<tr>
<td>Minimum Logic Vdd (V) (desktop)</td>
<td>0.6-0.9</td>
<td>0.5-0.6</td>
<td>0.3-0.6</td>
</tr>
<tr>
<td>$T_{ox}$ equivalent (nm)</td>
<td>0.8-1.2</td>
<td>0.6-0.8</td>
<td>0.5-0.6</td>
</tr>
<tr>
<td>Nominal $I_{on}$ @ 25°C ($\mu$A/$\mu$m) [NMOS/PMOS] high performance</td>
<td>750/350</td>
<td>750/350</td>
<td>750/350</td>
</tr>
<tr>
<td>Maximum $I_{off}$ @ 25°C ($\mu$A/$\mu$m) [NMOS/PMOS] high performance</td>
<td>40</td>
<td>80</td>
<td>100</td>
</tr>
<tr>
<td>Percent static power reduction necessary due to innovative circuit/system design</td>
<td>91</td>
<td>97</td>
<td>98</td>
</tr>
</tbody>
</table>

* International Technology Roadmap for Semiconductors

December 1999
Outline

• Drivers for scaling

• Scaled gate oxide
  – manufacturing yield
  – Boron penetration
  – reliability
  – tunneling current
  – diminishing returns in capacitance
  – degraded mobility

• High-k gate dielectrics

• Replacement gate processes

• Vertical Replacement Gate
Boron Penetration

- Boron from p-poly gate shifts pMOS threshold voltage
  - $10^{11}-10^{12}$ cm$^{-2}$ is a problem
  - Only *electrical* measurement is sensitive enough
- *Repeatability* is the key issue
- Depends sensitively on thermal cycle
- Depends sensitively on oxide thickness
- BF$_2$ assists boron transport
- *Nitrogen engineering can buy process margin*

Heavily B doped poly

Silicon substrate

Typical dopant-activation
RTA 1000°C, 5 sec
Anode Hole Injection Model

- Initial electron from tunneling or hot carriers
- 3.1 eV
- 4.6 eV
- Si
- SiO₂
- poly-Si
- Hole recombines with electron: interface state
- Hole trapped: oxide charge (electron trap)
- Lots of energy when electron reaches gate
- Recombination forms energetic hole
- This process depends on anode density of states and band structure

Chen et al. APL ’86
Updated Bude et al. IEDM ’98
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Fig. 7. Schematic illustration of the spheres model for intrinsic oxide breakdown simulation based on trap generation and conduction via traps. A breakdown path is indicated by the shaded spheres.

Degraeve et al, TED 45(4), 904(1998) (IMEC)
“Soft” Breakdown

• Sudden event
  – increase in current or current noise
  – *not* a resistive shunt afterwards

• More prevalent:
  – For thin oxides
  – At low voltages
  – For small areas (like transistors)

• New Model (Alam *et al.* ’99 IEDM)
  – Explains many features
  – Breakdown soft if power is below a threshold

• Circuit Implications
  – Some transistors still function
  – What can we live with?
Soft Breakdown Data

Weir et al, ’97 IEDM
The IBM “Doomsday Scenario”

1999 ITRS (high-performance):

n-FET, 0.1 cm²
10 year lifetime, 100 ppm fail rate

Stathis et al., IEDM ‘98, pp167 (IBM)
Reliability of SiO$_2$

- Reliability determines useful oxide thickness
- Time-dependent dielectric breakdown (TDDDB)
  - Not voltage for instantaneous breakdown
  - Need stressing of tens of samples for days or more
  - Depends on much more than electric field: electrode type, polarity, thickness, temperature, ...
- Breakdown is getting softer
- Other reliability issues (not discussed here)
  - Process-induced damage
  - Stress-induced leakage current
  - Negative Bias-Temperature Instability
  - Hot-carrier reliability at high $V_{DS}$

Current estimate of limit: $T_{ox, \, physical} \sim 1.5$nm
general agreement among Lucent, IBM, IMEC (see IRPS 2000)
SiO$_2$ Tunneling Current

Sorsch et al., '98 VLSI Symposium
What’s the Tunneling Current Limit?

- **Historical:** 34Å
- **Recent Past:** 1 A/cm² ⇒ 16Å SiO₂
- **Intel, AMD**: > 100 A/cm² ! ⇒ 11–12Å nitrided SiO₂
- **TSMC** ultra low power: < $10^{-3}$ A/cm² ! ⇒ 26Å

*VLSI Technology Symposium, June, 2000*
No charge in “bulk” of oxide: 

\[ F_{ox} = \frac{1}{\varepsilon \varepsilon_0 A} Q_{gate} = \frac{1}{\varepsilon \varepsilon_0 A} \int V C(V') dV' \]
Corrections depend only on $F_{ox}$
Calculated $\Delta T_{ox}$ in Substrate

$\Delta T_{ox} = \varepsilon_0 A/(\varepsilon_{ox} N_s) - T_{physical}$

Andrea Ghetti: Poisson and many-subband Schrodinger simulation
Scaling Oxide is Not Enough

- Quantum effects become significant
- Must scale $C_{\text{gate}}$, not $C_{\text{ox}}$

Kathy Krisch, 1997 VLSI Symposium
Mobility-limiting Mechanisms

\[ \mu_{\text{Lattice}} = 1500 \text{cm}^2/\text{V-s} \]

- Confined Acoustic Phonons
- Ionized Impurities \((N_A = 2 \times 10^{17} \text{ cm}^{-3})\)
- Roughness

Total Mobility = \(\Sigma \mu^{-1}\)
Mobility for $t_{ellips}$ 20.7Å
Oxide Scaling

• Difficulties
  – Boron penetration
  – Reliability
  – Tunneling current

• Diminishing returns
  – Capacitance corrections
  – Mobility degradation
Outline

• Drivers for scaling
• Scaled gate oxide
• High-κ gate dielectrics
  – materials and processing challenges
  – characterization challenges
• Replacement gate processes
• Vertical Replacement Gate
One View of Gate Dielectric Transition

thermal SiO₂

Nitrided SiO₂

“high-k”
to be named later

Si/SiO$_2$ Interface Properties

- Known preparation techniques (cleans+anneal)
- Low interface state density (<1/10,000 after H$_2$)
- Very low fixed charge
- No extrinsic scattering (?)
- Thermally stable
- Atomically abrupt
- Strained SiO$_2$ layer unless annealed above 900ºC

35 years of experience!

It’s not Si, it’s SiO$_2$ that makes CMOS work!
It’s not SiO$_2$, it’s the Si/SiO$_2$ interface!
High-κ Gate Stack Approaches

High-κ on Si Metal gate

<table>
<thead>
<tr>
<th>Al, Pt</th>
<th>Ta₂O₅, TiO₂</th>
<th>STO, BST</th>
</tr>
</thead>
<tbody>
<tr>
<td>Si</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Bottom Barrier

<table>
<thead>
<tr>
<th>Al, Pt</th>
<th>Ta₂O₅, TiO₂</th>
<th>STO, BST</th>
</tr>
</thead>
<tbody>
<tr>
<td>Si</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Top and Bottom Barrier

<table>
<thead>
<tr>
<th>Poly-Si</th>
<th>SiO₂</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ta₂O₅</td>
<td></td>
</tr>
<tr>
<td>SiO₂</td>
<td></td>
</tr>
<tr>
<td>Si</td>
<td></td>
</tr>
</tbody>
</table>
Metal-gate Improvement?

\[ T_{\text{ox,equiv}} = 2.0\text{nm} \quad 1.5\text{nm} \]

\[ V_{GS} - V_T = 1.0\text{V} \]

\[ N_A = 1.0 \times 10^{17} \text{cm}^{-3} \]

With Kathy Krisch and Jeff Bude, ‘97 VLSI Symp.
Possible High-κ Stacks

Metal gate with SiO₂ barrier. *Much of the electrical thickness “budget” is used by the SiO₂ layer.*

Si-compatible dielectric *Retains compatibility with poly-Si gate*
Stability of Silicates (700 - 900ºC)


• ZrO₂/ZrSiₓOᵧ stable next to Si; Ta and Ti oxide/silicate not stable

• Zr, Hf Silicates: no interfacial layer required AND can be used with poly-Si(Ge) gates
Stability of Hafnium Silicates on Si

As-Deposited
top Si at 25ºC

After Anneal
N₂/1050ºC/20 sec

Courtesy G. Wilk
formerly TI, now Bell Labs
**Metal-Gate Challenges**

### Single Midgap Metal

- Metals eliminate poly depletion and B penetration
- Midgap metals force $V_t \sim 0.5$ eV - **too high**
- Dual metals achieve low $V_t$, but difficult & costly processing

### Dual Metals

- Poly-Si allows same gate, only alter doping
- Poly depletion and B penetration must be addressed

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Don Monroe

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Outline

- Drivers for scaling
- Scaled gate oxide
- High-k gate dielectrics
- Replacement gate processes
  - Non-planar geometry
- Vertical Replacement Gate
Standard vs. Replacement Gate*

1. **Substrate with isolation**
2. **Clean; Grow gate oxide; Deposit undoped poly**
3. **Etch Gates; implants; anneal**

**Replacement Gate**

1. **Substrate with isolation**
2. **Deposit and Etch Gates; implants; anneal**
3. **Deposit interlayer dielectric; remove dummy gate**
4. **Deposit Gate Dielectric and Gate Metal**

*A. Chatterjee et al. (TI) ’97 IEDM*
Replacement-Gate Challenges

Standard high-κ challenges

- Ultra-conformal deposition
- Properties of film in corner

Risk of new process
Critical CMP process
Outline

• Drivers for scaling
• Scaled gate oxide
• High-k gate dielectrics
• Replacement gate processes

• Vertical Replacement Gate
  – Nonlithographic gate length control
  – Increased drive without scaling oxide
  – New knobs, new challenges
Comparison with Planar MOSFET

Planar MOSFET

Our Vertical MOSFET

Single-crystal silicon pillar
Vertical, Replacement-Gate Process

1. Implant bottom S/D
2. Deposit multilayer stack
3. Etch trench for device
4. Grow, CMP channel, deposit top S/D
5. Anneal to form S/D extensions
6. Remove sacrificial gate
7. Grow gate oxide, deposit gate
100 nm VRG MOSFET

Gate length controlled precisely through a deposited film thickness ⇒ can be scaled to sub 30 nm
Scanning Capacitance Image

Solid source diffusion provides self-aligned source/drain extensions

$L_G = 50$ nm
2-Input AND Comparison

Planar Layout (from 0.25µm ASIC Library)

SAME DENSITY
DOUBLE EFFECTIVE WIDTH

VRG Layout (using similar 0.25µm rules)
Layout Density and Drive Metrics

• Traditional Transistor Current Drive: $A/\mu m$
  – Useful for comparing planar transistors
  – Simple speed proxy if interconnect loaded

• VRG has (roughly) twice the width per area
  – Same \textit{coded} gate width
  – Two sides per pillar

\textbf{Need a new drive current metric}

\[ A/\mu m \Rightarrow A/\mu m^2 \]

VRG could be \textit{twice as good} as planar
(currently \textit{~20-40\%} better)
Can Extra Width Be Traded for $T_{ox}$?

- Extra width gives more drive, but also more loading
  - ALSO true of $T_{ox}$ scaling! (not all circuits benefit!)

- $T_{ox}$ scaling needed for short devices
  - BUT don’t need to worry about length variations

- $T_{ox}$ scaling has driven oxide fields very high
  - Leakage, reliability issues
  - Carrier velocity is degraded at high normal fields

- Electrical thickness of inversion layer limits effectiveness of $T_{ox}$ scaling

Some relaxation of oxide scaling should be possible!
Special VRG Metrology Needs

• **Gate Oxide**
  – The usual replacement-gate challenges
  – No blanket film area- sidewall is vertical
  – Stress in stack may change growth

• **Dopant distribution**
  – No planar structure for SIMS profiling
  – Solid-source diffusion may be sensitive to interlayers
  – The usual problem: interstitial distribution
    » Only indirect, post-mortem measurements
    » Critical for all shallow doping extensions
Summary

- **Gate oxide scaling**
  - Daunting challenges
  - Diminishing returns

- **Alternative gate dielectrics**
  - Similar diminishing returns
  - Many materials unknowns
  - New processes possible

- **Vertical, Replacement-Gate MOSFET**
  - Huge risks due to process and layout changes
  - No immediate materials changes
  - Provides an alternative to traditional oxide scaling
  - Non-lithographic gate-length control