2003 International Conference
Characterization & Metrology for ULSI Technology
CMOS Devices and Beyond
A Process Integration Perspective

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Primary barriers to MOSFET scaling are:
- High $I_{on}/I_{off}$ ratio ($I_{off} =$ Channel leakage current)
- Low Standby leakage current (Gate + Channel leakage)
  - Low channel leakage current (Electrostatic scaling)
  - Low gate leakage current
2001 ITRS Projections Vs. Simulations of Direct Tunneling Gate Leakage Current Density for Low Power Logic

Implementation of high-K will be driven by Low Power Logic in 2005.

(Simulations courtesy of C. Osburn, NCSU and ITRS and ISMT P. Zeitzoff)
2001 ITRS Projections Versus Simulations of Gate Leakage Current Density for High-Performance Logic

- Maximum $J_g$ ($\leq I_{sd,leak}$ per 2001 ITRS)
- Simulated $J_g$, oxynitride
- EOT
CMOS Devices and Beyond

Outline

◆ CMOS Devices ...
  ❖ MOSFET Scaling Issues
  ❖ Non-Classical CMOS Structures
    ■ Ultra-Thin Body MOSFETs
    ■ Channel Engineered Structures
    ■ FinFETs
    ■ Double Gate Structures

◆ ... And Beyond - Novel FET Structures and/or New Information Processing Architectures
  ❖ Potential of Molecular, Nanowire and Nanotube Electronics
    ■ MOSFET-like switches?
    ■ New Information Processing Technology?
  ❖ Limits on Integration Density - Device Size or Power?

◆ Conclusions
2003 International Conference
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CMOS Devices ....
A Process Integration Perspective
Maintaining historical CMOS performance trend requires new semiconductor materials and structures by 2008-2010... Earlier if current bulk-Si data do not improve significantly.
Nano-FET Scaling
Fundamental Issues

Electrostatic and quantum scaling ($I_{on}/I_{off}$)
- Increase carrier transport and ballistic efficiency.
- Reduce quantum tunneling of electrons and holes.
- Break the tyranny of the universal mobility curve.
  ☯ Bandgap engineered FET

New device architecture
Breaking the tyranny of the universal mobility: Alternative device structures & new Si-based materials

$E_y$ for constant inversion charge range for four device architectures

MIT - D. Antoniadis
Schematic cross section of planar bulk, UTB SOI, and DG SOI MOSFET

- **Bulk MOSFET**
  - Inversion Layer
  - Depletion Region

- **Ultra-Thin Body SOI**
  - Si Substrate
  - Ultra-thin silicon film
  - BOX

- **Double-Gate SOI MOSFET**
  - Si Substrate
  - Ultra-thin silicon film
  - BOX
  - G1
  - G2

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11
Ultra-Thin-Body MOSFET

**Advantages**
- Suppresses channel leakage
- Improves $V_t$ controllability
- Raised Si/Ge source/drain improves $I_{on}$

**Challenges**
- Requires ultra thin silicon channel
- Gate Stack
- Device characterization
- Compact model - parameter extraction
UTB SOI MOSFET Scaling

- Issues for bulk-Si MOSFET scaling obviated
  - Body does not need to be heavily doped
  - $T_{ox}$ does not need to be scaled as aggressively
    - EOT can be 5% lower for same $L_{gate}$ however (L. Chang et al., IEDM 2001)
  - Ultra-shallow S/D junction formation is not an issue

- Body thickness must be less than $\sim 1/3 \times L_{gate}$
  
  Scale length
  
  $$l = \sqrt{\frac{T_{ox} d \varepsilon_{si}}{\varepsilon_{ox} + d^2/2}}$$
  
  where $d = T_{Si}$

  Formation of uniformly thin body is primary challenge

U.C. Berkeley: S. - J. King
Theoretical mobility as function of silicon film. At $T_{SOI} = 3 - 5$ nm, mobility becomes higher than that in bulk Si MOSFET.

(S. Takagi et al.; SSDM ’97, p.154)
Advanced Gate Stack Materials for Thin-Body SOI MOSFETs

• **High-\(\kappa\) gate dielectrics**
  Desirable for reducing \(T_{ox,eq}\) to
  - improve \(I_{dsat}\)
  - reduce short-channel effects

❖ **Metal gate materials**
  Desirable to
  - eliminate gate depletion effect
  - reduce gate-line resistance

**Necessary to achieve proper \(V_t\) in UTB MOSFETs**
(due to low body doping \(N_{body}\))

U.C. Berkeley: S. - J. King
Thin-Body MOSFET $V_t$ Control
Gate Work-Function Engineering

- Low and symmetrical $V_t$’s are desirable
  - dual N+/P+ poly-Si
    \[ V_{tn} = -V_{tp} = -0.1V \leftarrow too\ low \]
  - mid-gap gate material
    \[ V_{tn} = -V_{tp} = 0.4V \leftarrow too\ high \]

\Rightarrow Need dual-work-function metal gates w/ tunable $\Phi_M$
\sim4.5V for NMOS; \sim4.9V for PMOS

L. Chang et al., *IEDM Technical Digest*, pp. 719-722, 2000

U.C. Berkeley: S. - J. King
Band Engineered Transistor
(Strained Si/SiGe Mobility Enhanced Channel)

Advantages
- Higher drive current ($I_{on}$)
- Compatible with bulk and SOI CMOS

Challenges
- High mobility channel film thickness for SOI
- Gate stack
- Integration process
- Device characterization

MIT - J. Hoyt
Mobility Enhancement in Strained-Si-Channel n-MOSFETs

\[ \nu_{\text{elec.}} = \frac{g_{\text{mi}}}{C_{\text{OX}}} \text{ (cm/sec)} \]

\[ \varepsilon_{\text{OX}} / C_{\text{OX}} = 67 \text{ A} \]

**Rim, Hoyt, Gibbons IEDM 1998**

Enhanced-mobility strained Si n-MOSFET test structure

**MIT - J. Hoyt**
FinFET Structure

Advantages
- Higher drive current ($I_{on}$)
- Improved subthreshold $V_t$ slope
- Improved short channel effect (electrostatics)
- Stacked NAND gate

Challenges
- Silicon film thickness
- Gate stack
- Process complexity
- Gate width available in integral steps
- Accurate TCAD
FinFET Scaling

- Compared with UTB-MOSFET:
  - Reduced short-channel effects => more scalable
  - Higher current drive due to
    - steeper subthreshold swing (60 mV/dec)
    - lower channel electric field => higher carrier mobilities

- Fin width must be less than \( \frac{2}{3} \times L_{\text{gate}} \)

Scale length \( l = \sqrt{T_{ox} d \frac{\varepsilon_{si}}{\varepsilon_{ox}} + \frac{d^2}{2}} \) where \( d = 0.5xT_{si} \)

Formation of narrow fin is primary challenge
  - sub-lithographic process needed

U.C. Berkeley: S. - J. King
FinFET $V_t$ Roll-Off Characteristics

Narrow $W_{\text{fin}}$ shows less $V_t$ roll-off.

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Subthreshold Swing and DIBL

When $L_g/W_{\text{fin}} > 1.5$, $S < 100\text{mV/dec}$ and $\text{DIBL} < 0.1\text{V/V}$.

U.C. Berkeley: S. - J. King
## Performance of Intel’s Tri-Gate p - and n - MOSFETs (Similar to the FinFET)

<table>
<thead>
<tr>
<th>Company</th>
<th>Channel Length (nm)</th>
<th>n- or p- Channel</th>
<th>Subthreshold Slope (mV/dec)</th>
<th>DIBL (mV/V)</th>
<th>Ion (mA/um)</th>
<th>Ioff (nA/um)</th>
<th>Vcc (V)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Intel</td>
<td>60</td>
<td>n-MOS</td>
<td>75</td>
<td>45</td>
<td>1.18</td>
<td>60</td>
<td>1.3</td>
</tr>
<tr>
<td>Intel</td>
<td>60</td>
<td>p-MOS</td>
<td>70</td>
<td>40</td>
<td>-0.65</td>
<td>-9</td>
<td>-1.3</td>
</tr>
</tbody>
</table>
Advantages

- Higher drive current ($I_{on}$)
- Improved subthreshold $V_t$ slope
- Improved short channel effect (electrostatics)
- Stacked NAND gate

Challenges

- Gate alignment
- Silicon film thickness
- Gate stack
- Process complexity
- Accurate TCAD
Technology Scaling & Challenges

- High-κ gate dielectrics not necessary to control short-channel effects, but will be helpful for achieving high $I_{dsat}$ (High-κ gate dielectrics will be necessary for low standby power applications)

- Parasitic resistance will be an issue for $T_{Si} < 10$nm
  - Raised S/D technology – but $C_{overlap}$ cannot be too high
  - Schottky S/D technology eventually needed

- Metal gate electrodes (different from those used for classical MOSFETs) will be needed
  - Multiple-$V_t$ technology will require tunable metal gate $\Phi_M$

- Structures which are provide for dynamic control of $V_t$ are desired by circuit designers

- Strained Si (for enhanced mobility) will be difficult to achieve
Fundamental Limits to Scaling Nanoelectronic Switch Elements
Scope of Emerging Research Devices

- Well doping
- Channel
- Depletion layer
- Isolation
- Halo
- Back-gate
- Channel
- Isolation
- Buried oxide
- Top-gate
- Double-Gate CMOS

Bulk CMOS

Double-Gate CMOS

New Memory Technologies

- Nanotubes
- Molecular devices

Emerging Information Processing Concepts

Quantum cellular automata

New Architecture Technologies
Ideal von Neumann’s Computer

- Highest possible integration density
- Highest possible speed
- Lowest possible energy consumption
Two Questions

1. What is the best direction to pursue for alternate information processing technologies (e.g., carbon nanotubes, molecular electronics, etc.)?
   - Replicate CMOS technology with new switches, gates, etc., directly one for one sustaining the von Neumann architecture? **Or**
   - Eventually invent and develop a completely new information processing technology and systems architecture?

2. What is the best application of CMOS *gate or switch replacement* technologies, e.g., carbon nanotube switches or molecular switches?
   - A completely new technology embodying not only the switch, but also the interconnect, I/O, etc. (completely replace CMOS) **Or**
   - Use of the CNT or molecular switch to replace the channel of a silicon MOSFET, thus extending the silicon MOSFET infrastructure process technology for a longer time?
Field Effect Transistor Electronic Switch

Gate Leakage

Source

Drain

Substrate

Gate

Channel Leakage

Thermionic Emission

QM Tunneling

BTB Tunneling

Sum = \( I_{\text{off}} \)

Channel Leakage

\( E_{\text{CB}} \)

\( E_{\text{VB}} \)

Source

Drain

\( L_{\text{gate}} \)
Distinguishability $D$ implies low probability $\Pi$ of spontaneous transitions between two wells (error probability)

$D=\max, \quad \Pi=0 \quad \Rightarrow \quad D=0, \quad \Pi=0.5 \ (50\%)$
Classic and Quantum Distinguishability

Classical

Quantum
Limit Performance of Charge Based Switch

Minimum Barrier Width

\[ a_{crit} = 0.6 \text{ nm} \]

Minimum Switch Width

\[ \text{Minimum Switch Width} \]

Maximum Gate Density

\[ n = 1 \times 10^{14} \, \text{gate/cm}^2 \]

Minimum state switching time

\[ t_{sc} = 2.3 \times 10^{-14} \text{ s} \]

Total Power Consumption

\[ P_{chip} = 2.0 \times 10^7 \, \frac{W}{\text{cm}^2} \]
Comparisons with 2001 ITRS (2016)

- **Gate density**
  - This analysis: $n = 1.0 \times 10^{14}$ gates/cm²
  - ITRS: $n = 1.4 \times 10^9$ gates/cm²

- **Switching time**
  - This analysis: $t = 23$ fs
  - ITRS: $t = 150$ fs (CV/I)

- **Power density**
  - This analysis: $P = 2.0 \times 10^7$ W/cm²
  - ITRS: $P = 93$ W/cm²

- **Power density normalized to density and switching time**
  - This analysis: $P = 43$ W/cm²
  - ITRS: $P = 93$ W/cm²
Comparisons with 2001 ITRS (2016)

Observations

- Transistor critical dimension limited to ~ 1 nm (In the 2001 ITRS physical gate length = 9 nm for 2016)
- Power density, not critical dimension, limits gate density to ~ 1 x 10^9 gates/cm²
- For the ITRS density and switching time, CMOS is approaching the maximum power efficiency
Are the most attractive directions for research?

**Near term**

Exploration of materials and structures for integration of alternate channels in an otherwise silicon MOSFET structure.

**Long term**

Synergistic exploration of new materials, structures and information processing architectures.
CMOS Devices and Beyond

Conclusions

◆ CMOS Devices ...
  ❖ MOSFET Scaling Issues
    - Low Power MOSFETs WILL need High-K Dielectric in 2005
    - High Performance may stay with SiON Gate Dielectric
  ❖ Non-Classical CMOS Structures
    - Ultra-Thin Body MOSFETs
    - Channel Engineered Structures
    - FinFETs (Good advancement by several laboratories)
    - Double Gate Structures

◆ … And Beyond
  ❖ Potential of Molecular, Nanowire and Nanotube Electronics
    - Near Term - MOSFET-like Switches
    - Long Term - New Information Processing Technology
  ❖ Limits on Integration Density - Power.
FinFET I-V Characteristics

\[ L_g = 15\text{nm}, \quad W_{\text{fin}} = 10\text{nm} \]

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