MATERIAL ISSUES AND IMPACT ON RELIABILITY OF Cu/LOW k INTERCONNECTS

Paul S. Ho
Microelectronics Research Center
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APS March Meeting 2003
• Technology challenges for low k dielectrics
• Chemical bond and polarizability
• Impact of low k dielectrics on reliability of Cu interconnects
  Dielectric confinement effects
  Electromigration characteristics
• Summary
Effect of Scaling on Gate and Interconnect Delays

Interconnect delay dominates IC speed
Implementation of low $k$ dielectrics reduces RC delay
Power dissipation
Crosstalk noise
Number of metal level

Mark Bohr, IEEE IEDM Proc. 1995
Cost and Manufacturability Issue

Sematech 1998

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### Table 1: Technology Trends and the Need for Low-Dielectric Constant Materials

<table>
<thead>
<tr>
<th></th>
<th></th>
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<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Metal Levels</td>
<td>4 - 5</td>
<td>5</td>
<td>5 - 6</td>
<td>6 - 7</td>
<td>7 - 8</td>
</tr>
<tr>
<td>Device Frequency (MHz)</td>
<td>200</td>
<td>350</td>
<td>500</td>
<td>750</td>
<td>1,000</td>
</tr>
<tr>
<td>Interconnect Length (m/chip)</td>
<td>380</td>
<td>840</td>
<td>2,100</td>
<td>4,100</td>
<td>6,300</td>
</tr>
<tr>
<td>Capacitance (fF/mm)</td>
<td>0.17</td>
<td>0.19</td>
<td>0.21</td>
<td>0.24</td>
<td>0.27</td>
</tr>
<tr>
<td>Resistance (metal1)(ohm/µm)</td>
<td>0.15</td>
<td>0.19</td>
<td>0.29</td>
<td>0.82</td>
<td>1.34</td>
</tr>
<tr>
<td>Dielectric Constant (k)</td>
<td>4.0</td>
<td>2.9</td>
<td>2.3</td>
<td>&lt;2</td>
<td>2 - 1</td>
</tr>
</tbody>
</table>

*Based on the National Technology Roadmap for Semiconductors, 1994*
## Interconnect Technology Requirements for MPU

### Table: Interconnect Technology Requirements

<table>
<thead>
<tr>
<th></th>
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<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>MPU ½ pitch</td>
<td>230</td>
<td>210</td>
<td>180</td>
<td>160</td>
<td>145</td>
<td>130</td>
<td>115</td>
</tr>
<tr>
<td>Minimum metal effective resistivity (µΩ-cm) Al wiring*</td>
<td>3.3</td>
<td>3.3</td>
<td>3.3</td>
<td>3.3</td>
<td>3.3</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Minimum metal effective resistivity (µΩ-cm) Cu wiring*</td>
<td>2.2</td>
<td>2.2</td>
<td>2.2</td>
<td>2.2</td>
<td>2.2</td>
<td>2.2</td>
<td>2.2</td>
</tr>
<tr>
<td>Barrier/cladding thickness (conformal) (nm)</td>
<td>17</td>
<td>16</td>
<td>14</td>
<td>13</td>
<td>12</td>
<td>11</td>
<td>10</td>
</tr>
<tr>
<td>Interlevel metal insulator- effective dielectric constant (κ)</td>
<td>3.5-4.0</td>
<td>3.5-4.0</td>
<td>2.7-3.5</td>
<td>2.7-3.5</td>
<td>2.2-2.7</td>
<td>2.2-2.7</td>
<td>1.6-2.2</td>
</tr>
</tbody>
</table>

Solutions Exist: [Blank]
Solutions Being Pursued: [Green]
No Known Solutions: [Red]

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*International Technology Roadmap for Semiconductors, 1999*
## Interconnects Technology Requirements for MPU

<table>
<thead>
<tr>
<th></th>
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<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>MPU ½ pitch</td>
<td>150</td>
<td>130</td>
<td>107</td>
<td>90</td>
<td>80</td>
<td>70</td>
<td>65</td>
</tr>
<tr>
<td>Minimum metal effective resistivity (µΩ-cm) Al wiring*</td>
<td>3.3</td>
<td>3.3</td>
<td></td>
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<td></td>
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<td>16</td>
<td>14</td>
<td>12</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Interlevel metal insulator- effective dielectric constant (κ)</td>
<td>3.0-3.6</td>
<td>3.0-3.6</td>
<td>3.0-3.6</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Solutions Exist
Manufacturing Solutions known
No Known Solutions

International Technology Roadmap for Semiconductors, 2001

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IBM CMOS9S0 Technology

9S BEOL Stack
8 Level Metal
(4@1x, 2@2x, 2@4x)

<table>
<thead>
<tr>
<th></th>
<th>0.13 µm</th>
<th>0.18 µm</th>
</tr>
</thead>
<tbody>
<tr>
<td>MDR shrink</td>
<td>0.25x</td>
<td>0.35x</td>
</tr>
<tr>
<td>Supply Voltage</td>
<td>1.2V</td>
<td>1.5V</td>
</tr>
<tr>
<td>Gate Length (drawn)</td>
<td>0.125 µm</td>
<td>0.175 µm</td>
</tr>
<tr>
<td>M1 pitch</td>
<td>0.35 µm</td>
<td>0.49 µm</td>
</tr>
<tr>
<td>M2 pitch</td>
<td>0.40 µm</td>
<td>0.63 µm</td>
</tr>
<tr>
<td>Mx pitch</td>
<td>0.45 µm</td>
<td>0.63 µm</td>
</tr>
<tr>
<td>2x pitch FW</td>
<td>0.90 µm</td>
<td>1.26 µm</td>
</tr>
<tr>
<td>4x pitch FW</td>
<td>1.80 µm</td>
<td>NA</td>
</tr>
<tr>
<td>Metal Levels</td>
<td>8</td>
<td>7</td>
</tr>
<tr>
<td>ILD</td>
<td>SiLK</td>
<td>USG/FSG</td>
</tr>
<tr>
<td>K_{eff}</td>
<td>3.0</td>
<td>4.0</td>
</tr>
</tbody>
</table>

R. Goldblatt et al., IITC 2000

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Intel 90nm Interconnect Technology

7 metal levels on 300mm wafer
Low k CDO, Capacitance improved by 18%
M. Bohr, Intel Developer Forum 9/2002
Contributions to Dielectric Constant

\[ \varepsilon = 1 + 4 \pi P/E \]

- Electronic polarizability
  - optical frequency \((10^{14-15} \text{ S}^{-1})\)
- Vibrational (atomic)
  - IR \((10^{12-13} \text{ S}^{-1})\)
- Rotational (orientation of permanent dipoles)
  - microwave \((10^9 \text{ S}^{-1})\)
Microscopic Origins of Polarization

3 Sources of Polarization

Electronic (Induced)
Visible - UV

Atomic (Induced)
Infrared

Orientational (Permanent)
μw - infrared

K. Taylor, IRPS Tutorial 2000
Basic Approaches to Reduce Dielectric Constant

• Optimization of molecular structure
  Minimize configurational and dipole polarizability, e.g. use of C-C and C-F bonds

• Reduce density and incorporation of porosity
  Add uniform and microscopic pores with k of 1

• Limitation: both approaches degrade the thermomechanical properties
  Proper tradeoff of dielectric constant and thermomechanical properties important
## Electronic Polarizability vs. Strength of Chemical Bonds

<table>
<thead>
<tr>
<th>Bond</th>
<th>Polarizability* (angstrom$^3$)</th>
<th>Ave. Bond Energy# (Kcal/mole)</th>
</tr>
</thead>
<tbody>
<tr>
<td>C-C</td>
<td>0.531</td>
<td>83</td>
</tr>
<tr>
<td>C-F</td>
<td>0.555</td>
<td>116</td>
</tr>
<tr>
<td>C-O</td>
<td>0.584</td>
<td>84</td>
</tr>
<tr>
<td>C-H</td>
<td>0.652</td>
<td>99</td>
</tr>
<tr>
<td>O-H</td>
<td>0.706</td>
<td>102</td>
</tr>
<tr>
<td>C=O</td>
<td>1.020</td>
<td>176</td>
</tr>
<tr>
<td>C=C</td>
<td>1.643</td>
<td>146</td>
</tr>
<tr>
<td>C≡C</td>
<td>2.036</td>
<td>200</td>
</tr>
<tr>
<td>C≡N</td>
<td>2.239</td>
<td>213</td>
</tr>
</tbody>
</table>

## Recent Low k Dielectric Materials

<table>
<thead>
<tr>
<th>Material</th>
<th>Type</th>
<th>Manufacture</th>
<th>k</th>
</tr>
</thead>
<tbody>
<tr>
<td>SiLk</td>
<td>Organic themoset</td>
<td>Dow Chemical</td>
<td>2.65</td>
</tr>
<tr>
<td>FLARE 2.0</td>
<td>Poly aryl ether</td>
<td>Allied Signal</td>
<td>2.8-2.9</td>
</tr>
<tr>
<td>Black Diam. Corel</td>
<td>MSQ type CVD</td>
<td>Applied Mat. Novellus</td>
<td>2.7</td>
</tr>
<tr>
<td>P SiLk Orion LKD 5109 XPX</td>
<td>Porous spin on material</td>
<td>Dow Trikon JSR Asahi</td>
<td>2.0-2.3</td>
</tr>
</tbody>
</table>
Molecular Structure of SiLK

Formation of polyphenylene polymer structure


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Crosslinked Silica-Based Materials

- Si-O network provides rigidity
- Organic groups lower $k$ to 2.5-3.3

silsesquioxane $RSiO_{1.5}$

<table>
<thead>
<tr>
<th></th>
<th>HSQ</th>
<th>MSQ</th>
</tr>
</thead>
<tbody>
<tr>
<td>$k$</td>
<td>2.9-3.0</td>
<td>2.7-2.8</td>
</tr>
</tbody>
</table>

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## Dielectric and Thermomechanical Properties of Low k Films

M. Kiene et al., Handbook of Si Semicond. Metrology, Marcel Dekker Inc. 2001

<table>
<thead>
<tr>
<th>Material</th>
<th>k</th>
<th>Young’s Modulus (GPa)</th>
<th>Lateral TEC 25-225°C (ppm/°C)</th>
<th>Tg (°C)</th>
<th>TGA % weight loss (425°C, 8 hrs.)</th>
</tr>
</thead>
<tbody>
<tr>
<td>PTFE</td>
<td>1.92</td>
<td>0.5</td>
<td>135</td>
<td>250</td>
<td>0.6</td>
</tr>
<tr>
<td>BPDA-PDA</td>
<td>3.12</td>
<td>8.3</td>
<td>3.8</td>
<td>360</td>
<td>0.4</td>
</tr>
<tr>
<td>crosslinked PAE</td>
<td>2.8-3.0</td>
<td>2.7</td>
<td>52</td>
<td>350</td>
<td>2.5</td>
</tr>
<tr>
<td>Fluorinated PAE</td>
<td>2.64</td>
<td>1.9</td>
<td>52</td>
<td>&gt;400</td>
<td>x</td>
</tr>
<tr>
<td>BCB</td>
<td>2.65</td>
<td>2.2</td>
<td>62</td>
<td>-</td>
<td>30</td>
</tr>
<tr>
<td>SiLK</td>
<td>2.65</td>
<td>2.3</td>
<td>54</td>
<td>-</td>
<td>2.1</td>
</tr>
<tr>
<td>Parylene-N</td>
<td>2.58</td>
<td>2.9</td>
<td>55-100+</td>
<td>425 (melt)</td>
<td>30</td>
</tr>
<tr>
<td>Parylene-F</td>
<td>2.18</td>
<td>4.9</td>
<td>33</td>
<td>-</td>
<td>0.8</td>
</tr>
<tr>
<td>HSQ</td>
<td>2.8-3.0</td>
<td>7.1*</td>
<td>20.5</td>
<td>-</td>
<td>x</td>
</tr>
</tbody>
</table>

* Biaxial modulus
x Not measured
- None observed
Integration of Cu Damascene Structure

1. Deposit Low $\kappa$
2. Deposit Cap (350 - 400°C)
3. Pattern and etch Low $\kappa$
4. Deposit barrier (< 200°C)
5. Deposit Cu seed (< 200°C)
6. Electroplated Cu fills trench
7. Cu anneal (250 - 350°C)
8. CMP Cu
9. Deposit cap (350 - 400°C)
EFFECT OF QUARTZ CONFINEMENT ON THERMAL STRESS OF AL LINE STRUCTURES

ESHELBY’S MODEL OF ELASTIC INCLUSIONS
M. Korhonen et al., MRS Bulletin, 1992)
EM Damage Formation in Damascene Structure
Damage formation due to flux divergence in dual-damascene interconnect.

Possible regions of Flux Divergence

Grain Boundary Pathway

Interface Pathways

Extrusion

Cathode Voiding: M2 Trench and Via Bottom

Anode Hillock: Extrusion


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Blech effect and $jL_c$ threshold product

The average drift of metal ions under EM is balanced by a back flow stress as:

$$v_d = v_{EM} + v_{BF} = \mu (Z^* e \rho j - \Omega \Delta \sigma / L)$$

There is a threshold or critical product $jL_c$, when $v_d = 0$,

$$jL_c = \Omega \Delta \sigma / Z^* e \rho \propto \Delta \sigma$$

$\Delta \sigma$ changes the net drift rate, hence the EM lifetime. It depends on the dielectric confinement and $(jL)_c$ provides a measure for $\Delta \sigma$
Stress evolution in confined metal lines under EM

No void formation
No metal extrusion
Applicable to AlCu

M.A. Korhonen et al., JAP 73, 3790, 1993

Stress generation in lines with clusters of blocking grains

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With void formation, local stress relaxation leads to a compressive stress state.

Voids can form under a low tensile stress, the case is applicable to Cu.

With mass transport dominated by interfacial diffusion, microstructure effect is reduced but $\sigma_{\text{max}}$ depends on interfacial adhesion.
Effective Modulus for Interconnects under EM

Stress more tensile

(cross sections)

Stress more compressive

- Restoring force from surrounding dielectric determines hydrostatic stress

\[
\frac{dC}{C} = -\frac{d\sigma}{B}
\]  
(Korhonen 93)

B is a function of dielectric, geometry, and metallization.

M.A. Korhonen et al., JAP 73, 3790, 1993; S. Hau-Riege, UC Berkeley Short Course 2002

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Finite element analysis of effective modulus B

For Cu interconnects, \( \varepsilon_1 = \varepsilon_2 = 0 \) but \( \varepsilon_3 \neq 0 \) to account for mass transport via interfacial diffusion

Modeling:
- 3 Dimensional
- 1 MA/cm\(^2\)
- Test at 325°C
- ILD
  - SiO\(_2\)
  - Organic Polymer
  - CVD MSQ
  - Porous MSQ
Effective Modulus of Cu Dual Damascene Interconnects

Reduced Effective Modulus on M2

B: $\varepsilon_1 = \varepsilon_2 = 0$, only $\varepsilon_3 \neq 0$

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Void formation in Cu interconnect

Void can be nucleated at interface with a relatively low stress\(^1\)

Maximum void volume at steady state \(^2\)

\[
V_{\text{max}} = \frac{\sigma^T L}{B} + \frac{J \rho e Z^* L^2}{2 \Omega B}
\]

\(V_{\text{max}} \propto 1/B\)

Void volume depends not only on \(j\) but also on \(\sigma^T\), thermal stress.

If line failure by the same void volume, EM lifetime will be proportional to \(B\) under similar test conditions.

But lifetime will be reduced if interfacial delaminates before reaching the steady state \(V_{\text{max}}\).

2. M.A. Korhonen et al., JAP *73*, 3790, 1993
EM Cu/low k test structure

- Low-k dielectric materials are implemented in all levels
- Oxide etch stop layer is deposited on low-k material.
- The low k ILD and CMP etch stop layer introduce new interfaces in Cu/low k interconnects.
**EM Lifetime Characteristics**

The EM lifetime of Cu/low k interconnects is shorter than Cu/oxide. This can be attributed to the thermomechanical properties of low k ILDs.

![Graph showing t50 vs. 1/KT with data points for different materials: Cu/Oxide, Cu/CVD Low k, Cu/Porous MSQ, Cu/Org. Pol., Cu/CVD Low k.]

Drift velocity for a confined structure:

\[ v_d = v_{EM} + v_{BF} = \mu (Z*e\rho j - \Omega \Delta\sigma/L) \]

Decrease in \( \Delta\sigma/L \) due to less confinement increases \( v_d \) and reduces EM lifetime.

** I. A. Blech, *JAP* 47, 1203 (1976)

<table>
<thead>
<tr>
<th>Material</th>
<th>Org. Pol.</th>
<th>Por. MSQ</th>
<th>CVD Low k</th>
<th>Oxide</th>
</tr>
</thead>
<tbody>
<tr>
<td>Modulus (GPa)</td>
<td>2.5</td>
<td>3.6</td>
<td>6</td>
<td>71.4</td>
</tr>
<tr>
<td>B (GPa)</td>
<td>7.2</td>
<td>7.3</td>
<td>7.6</td>
<td>13.7</td>
</tr>
</tbody>
</table>

\[ t_{50} \propto B \]

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Temperature dependence of $jL_c$ was not observed. $jL_c$ values of organic polymer are below that estimated from B due to interfacial delamination.
EM Failure Analysis in Cu/Oxide Structure

- At the anode end, extrusion occurs through the SiNx cap layer due to EM induced Cu mass transport. (Anode Extrusion)
- After extrusion, back stress in the line will decrease to enhance void formation at the cathode.
EM Failure in Cu/Low k Interconnect

- A hydrostatic compressive stress at anode breaks the interface of organic polymer and cap layer.
- Cu extrudes through interface between organic polymer and cap layer; failure due to interfacial delamination.

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Failure Analysis - Cu/Organic polymer

- A high compressive stress at anode caused interfacial delamination as well as anode extrusion.
Summary

- Low k dielectrics are required for development of Cu interconnects for 130 nm technology node and beyond.
- Thermal stress behavior indicates that barrier and cap layers are important in sustaining structural integrity of low k interconnects. Local stress concentration can lead to delamination and failure of structure.
- EM results show mechanical properties can significantly affect lifetime and distinct failure modes are observed due to interfacial delamination in low k structures.
- Implementation of surface coating to reduce the interfacial mass transport and enhance adhesion is important for reliability improvement for Cu/low k interconnects.
Acknowledgement

• Low k material characterization
  M. Morgen (Lucent), M. Kiene (AMD), C. Hu (Intel), J. Zhao (Motorola), J. Liu

• Electromigration
  E. Ogawa (TI), K. D. Lee, X. Lu

• Thermal Stress
  Y. Du (AMD), S. H. Rhee (AMD), D. Gan, G. Wang

• Financial Support
  Semiconductor Research Corp (SRC, H. Hosack)
  International Sematech (J. Wetzel, J. Iacoponi)
  Texas Advanced Research and Technology Program

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Summary

• Low $k$ dielectrics are required for development of Cu interconnects for 130 nm technology node and beyond.

• Dielectric confinement is important in controlling EM reliability of Cu interconnects. The effect depends on material properties, interconnect geometry and structures.

• The activation energies of Cu/oxide and Cu/low $k$ interconnects are in the range from 0.81 to 0.93 eV, indicating that interfacial diffusion dominates mass transport for Cu interconnects.

• There is a good correlation between the effective elastic modulus $B$ and EM characteristics of Cu/lowk structures. Results is affected by damage formation due to interfacial delamination or metal extrusion.