In-line, Non-destructive Electrical Metrology of Nitrided Silicon Dioxide and High-k Gate Dielectric Layers


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Pittsburgh, PA

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Austin, TX
Electrical Characterization for MOS

- Device performance depends heavily on electrical properties of MOS structure
  - Bias dependence
  - Current dependence

- Atomic Profiles (SIMS), physical measurements (TEM) and optical measurements (Ellipsometry) do not correlate to final device behavior as well as electrical measurements

- Electrical data can be used for
  - Rapid monitoring of semiconductor processes
  - Monitoring Product Wafers
  - Predicting device performance
  - Determining reliability issues
Primary Parameters

- Gate Engineering
  - On-state Drive Current
    - Capacitance Effective Thickness (CET)
    - Equivalent Oxide Thickness (EOT)
    - Effective Dielectric Constant
  - Off-state Leakage Current
    - Gate Leakage Current ($I_{LK}$)
  - Interface Trap Density ($D_{IT}$)
  - Gate Dielectric Charge and Stability
  - Current-Voltage Behavior
    - Current Transport Mechanisms
      - Current-Voltage (IV) Profile
    - Stress Induced Leakage Current (SILC)
  - Reliability
    - Time Dependent Dielectric Breakdown (TDDDB)
    - Time Zero Dielectric Breakdown and Defect Density
  - Alternate High-k Dielectrics
Ultra-thin (<3 nm) Leakage Effects on CV

- Modeling Approach:
  - Henson, EDL-20, Apr (1999)
  - Choi, EDL-20, June (1999)

- Dual Frequency Approach:
  - Yang, TED-46, July (1999)
Multi-frequency CV Dispersion

EM-gate Multi-frequency Comparison
Thin High K HfO$_2$

Frequency Range: 5 KHz to 1 MHz

Note: HP-4284A Used
Series/Parallel Model Comparison

EM-gate MOS CV Parallel / Series Model Comparison

- Gate Voltage (V)
- C (pF)

Parallel Model
Series Model
Evolution of Alternate Gate Formations

Poly Gate

| SiO₂ | Si |

Conventional Method:
1. MOS gate formed by depositing polysilicon
2. Gate formation time: 6 hours to days
3. Processing required to form gate
4. For monitor wafers only

Corona Biasing

| SiO₂ | Si |

Introduced in 1995:
1. COS gate formed through deposition of corona charge
2. Charge formation time: 5 min. for 1 Q-V sweep.
3. Smallest test area: 5 mm diameter
4. For monitor wafers only

EM-gate

| SiO₂ | Si |

1. MOS gate formed through elastic deformation of non-invasive probe.
2. Gate Formation Time: 2 seconds
3. Small diameter gate for scribe line positioning
4. Measures Product Wafers
High Frequency MOS CV Curve

- $C_{OX}$
- $V_{FB}$
- $V_T$
- Capacitance vs. Gate Voltage
- Delta $V_{FB}$

[Reverse CV]
[Forward CV]
Conductance-Voltage (GV) Curve

- Sensitive to Leakage and Series Resistance
- Sensitive to Interface Trap Density ($D_{IT}$)
- Series Resistance Corrected G

Gate Voltage (V)
Calibration: Contact Models

Series/Parallel Model

\[ C_M = C_{OX1} + \frac{1}{(1/C_{OX2}) + (1/C_1)} \]

Series Model

\[ C_M = \frac{1}{(1/C_{OX}) + (1/C_1)} \]
EM-gate Short Term Repeatability Test
8 Angstrom SiON Wafer

- Mean = 9.83 Ang.
- Sigma = 0.051 Ang.
EM-gate Repeatability

- **Short Term**
  - CET: <0.1 Ang.
  - VFB: ~6 mV
  - DIT: ~1%

- **Multiple Day**
  - CET: ~0.1 Ang.
  - VFB: ~12 mV
  - DIT: ~2%

### EM-gate CET 3 Day repeatability

<table>
<thead>
<tr>
<th>Day 1</th>
<th>Day 2</th>
<th>Day 3</th>
<th>Std DEv</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
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</tr>
<tr>
<td>CET (Å)</td>
<td>19.43</td>
<td>19.40</td>
<td>19.40</td>
</tr>
<tr>
<td></td>
<td>19.38</td>
<td>19.63</td>
<td>19.98</td>
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<tr>
<td></td>
<td>19.97</td>
<td>19.81</td>
<td>19.86</td>
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<tr>
<td></td>
<td>19.87</td>
<td>20.07</td>
<td>19.99</td>
</tr>
<tr>
<td></td>
<td>20.42</td>
<td>20.56</td>
<td>20.36</td>
</tr>
<tr>
<td></td>
<td>19.82</td>
<td>19.63</td>
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<td>19.71</td>
<td>19.65</td>
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</tr>
<tr>
<td></td>
<td>19.03</td>
<td>19.22</td>
<td>19.40</td>
</tr>
</tbody>
</table>

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EM-gate CV and GV: ~13.5 Ang. SiO₂

- Un-annealed Oxides Exhibit lower $C_{OX}$, Higher $D_{IT}$ and $V_{FB}$ Shift
- No Leakage Effects Present
EM-gate CV and GV: < 20 Ang. SiON

- Un-annealed Oxides Exhibit lower $C_{OX}$, Higher $D_{IT}$, $V_{FB}$ Shift and Distortion in CV Curve
- No Leakage Effects Present
EM-gate CV: EOT Comparison

Annealed SiON Tox Comparison

- Specified OTox
- EM-gate EOT

<table>
<thead>
<tr>
<th>Wafer #</th>
<th>Specified OTox</th>
<th>EM-gate EOT</th>
</tr>
</thead>
<tbody>
<tr>
<td>13</td>
<td>18</td>
<td>16</td>
</tr>
<tr>
<td>14</td>
<td>17</td>
<td>16</td>
</tr>
<tr>
<td>15</td>
<td>18</td>
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<td>20</td>
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<tr>
<td>21</td>
<td>18</td>
<td>16</td>
</tr>
<tr>
<td>25</td>
<td>12</td>
<td>16</td>
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</table>
EM-gate GV Comparison: 21 Ang. Oxides

EM-gate Series GV
21 Ang. SiO₂ Gate Ox Preclean Matrix

Clean 1 (Std): Dit = 1.11E11 cm⁻² eV⁻¹
Clean 2: Dit = 3.81E11 cm⁻² eV⁻¹
Clean 3: Dit = 4.89E11 cm⁻² eV⁻¹
Clean 4: Dit = 7.00E11 cm⁻² eV⁻¹
Effects of Electrical Stress on Vfb

**Vfb** Sigma

<table>
<thead>
<tr>
<th>Recipe</th>
<th>Partial CV, Fixed CFB (-1.1 to -0.5 V)</th>
<th>Partial CV, No PB, 0 sec light delays</th>
<th>Partial CV (-0.95 to -0.7 V), Fixed CFB</th>
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<tr>
<td>Standard Recipe</td>
<td>Purple bar</td>
<td>Blue bar</td>
<td>Yellow bar</td>
</tr>
<tr>
<td>Nb PB</td>
<td>Orange bar</td>
<td>Green bar</td>
<td>Red bar</td>
</tr>
<tr>
<td>Use Fixed Nb</td>
<td>Pink bar</td>
<td>Brown bar</td>
<td>Cyan bar</td>
</tr>
<tr>
<td>R = 300 mV/s</td>
<td>White bar</td>
<td>Light blue bar</td>
<td>Lilac bar</td>
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**DIT**

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**Partial GV: EL17**

<table>
<thead>
<tr>
<th>Vg(V)</th>
<th>G(uS)</th>
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<tbody>
<tr>
<td>-1.9</td>
<td>14</td>
</tr>
<tr>
<td>-1.4</td>
<td>12</td>
</tr>
<tr>
<td>-0.9</td>
<td>10</td>
</tr>
<tr>
<td>-0.4</td>
<td>8</td>
</tr>
<tr>
<td>0.1</td>
<td>6</td>
</tr>
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</table>

**Partial CV: EL17**

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<th>C(pF)</th>
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<td>8</td>
</tr>
<tr>
<td>-0.4</td>
<td>6</td>
</tr>
<tr>
<td>0.1</td>
<td>2</td>
</tr>
</tbody>
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MOSCAP IV: SiON Leakage Current Comparison

1000 C Anneal SiON Wafers

Leakage Current (A) vs. Nitridization Time (sec)

- Vg = -2.0 V
- Vg = -1.0 V

Un-annealed Leakage Current (Vg = -1.0 V)
EM-gate IV Example A: 8 to 17 Ang. SiO₂ & SiON

EM-gate Leakage Current, (Vg = -1.8 V)
50 % Cumulative Probability for SiO₂ & SiON groups

- SiO₂:
y = 0.0269e^{-0.6921x}  
R² = 0.9988
(3.33 Ang./Decade)

- SiON:
y = 0.0388e^{-0.6548x}  
R² = 0.9975
(3.52 Ang./Decade)
EM-gate vs Polysilicon Gate IV Leakage Correlation

\[ y = 0.0038 x^{0.5231} \]

\[ R^2 = 0.9929 \]

- Pure oxide
- RTN

EM-gate
\[ \log_{10} @ V_g = 1.8 \text{V} \]

Polysilicon Gate
\[ \log_{10} @ V_g = -1.8 \text{V} \]
EM-gate CV, GV: Scribe Line Test Areas on Patterned Wafer

CMOS Product Wafer

CV and GV Measurements

80 µm x 120 µm Test Area

CG-V curve of patterned wafer

- Capacitance in pF
- Conductance in µS
EM-gate MOS CV: High k Dielectrics

Elastic Probe CV Curve Comparison
High K Dielectrics (25 to 200 Angstroms)

- 25 Å HfO$_2$
- 50 Å HfO$_2$
- 30 Å Al$_2$O$_3$
- 50 Å Al$_2$O$_3$
- 200 Å ZrO$_2$

Gate Voltage (V)

C (pF)
Summary

◆ FastGate™ Technology
  • Is Rapid (60 Wafers/Hr)
  • Is Repeatable
  • is Non-damaging and non-contaminating
  • Can measure Oxides and Oxynitrides as thin as 7 Ang.
  • Can measure Product Wafers

◆ EM-gate CV and IV Capability Includes
  • CET, EOT
  • $V_{FB}$ and $V_{T,CV}$
  • $D_{IT}$
  • Delta $V_{FB}$ Hysteresis
  • $N_{SURF}$ and Carrier Density Profile
  • Leakage Current
  • IV Profile

◆ Applications on thin SiO$_2$, SiON with EOT values between 8 Ang. and 20 Ang. have been shown