Nanoelectronics and More-than-Moore at IMEC

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IMEC Fellow
Moore’s Law

In 1965, Intel co-founder Gordon Moore predicted that the number of transistors on a piece of silicon would double every couple of years—an insight later dubbed “Moore’s Law.” His prediction has held true, as ever-shrinking transistor sizes have allowed exponential growth in the number of transistors on a single chip.

Moore’s Law is now a basic principle in the electronics industry, and Intel applies its principles literally to products. Whole new ways for people to play, learn, and work have come about as the company has doubled its capacity every 18 months since the introduction of the microprocessor.

Cost scaling

Improved performance
Node-to-Node Transistor scaling requires:

- 50% area reduction
- 25% performance increase @ scaled $V_{dd}$
- 20% power reduction
- Repeats every 2-3 years
Moore's law & transistor scaling

Lithography Enabled Scaling

Gate Oxide Thickness (nm)


0.35 um
0.25 um
0.18 um
0.13 um
90nm

2002-2003
~ 90 nm
Rayleigh equation defines litho roadmap

\[ \text{resolution} = k_1 \cdot \frac{\lambda}{NA} \]

Exposure wavelength (\( \lambda \))
- 436nm: g-line
- 365nm: i-line
- 248nm: Deep-UV (KrF)
- 193nm: Deep-UV (ArF)
- 157nm: Vacuum UV (F2)
- 13.5nm: Extreme UV (EUV)

Low \( k_1 \) lithography (\( k_1 \geq 0.25 \))
Resolution enhancement techniques, process control.

Dry lithography: \( \leq 0.93 \)
Immersion lithography: \( \leq 1.35 \)
EUV lithography: 0.25 – 0.32NA
What is EUV lithography?

The EUV radiation (13.5nm) is strongly absorbed by all known materials and gases. As a consequence:

- The **optics** must be **reflective** and fully contained in **vacuum**

- The **reticle** must be **reflective** too, and **no pellicle** can be used to keep the possible defects out of focus.

- All mirrors (including the reticle) use an alternating stack of Mo/Si layers with a theoretical maximum reflectivity (under normal incidence) of only 74%. Keeping the mirror count to a minimum is a priority.

- Lots of EUV **intensity** is **lost** (high power is needed).

CRITICAL ISSUES: source power, masks and resists
EUV performance

- **28nm L/S**
  - 12.4mJ/cm²
  - LER = 4.2nm

- **30nm IL**
  - 11.8mJ/cm²

- **32nm LES**
  - LES = 15nm

- **32nm CH**
  - 14.8mJ/cm²

Local CDU: 1.2nm

Good process window for 28nm L/S
Good photo speed and good resist profiles
EUV extendability
Self-aligned double patterning

30 nm L/S

15 nm L/S

30/30 nm

20 nm UL

30 nm CVD Nitride

a-C 100 nm

Poly 66 nm

Substrate

15 nm L/S

Poly 66 nm

Substrate
Moore’s law & transistor scaling

Lithography Enabled Scaling

Materials Enabled Scaling

Gate Oxide Thickness (nm)


0.35 um

0.25 um

0.18 um

0.13 um

90 nm

65 nm

45 nm

~ 90 nm

~ 16 - 14 nm
Research challenges

Technology complexity increases
- Many options still to be researched
- Combination of new materials & architectures
- System/Circuit-level implications

Technology complexity increases over the years:
- MOSFET
  - SiN Passivation
  - ‘60
- LOCOS
  - Ion implant
  - Plasma Etch
  - ‘70
- i-line Steppers
  - LDD
  - Silicide
  - ‘80
- KrF scanners
  - CMP
  - Ext / HALO
  - Cu metal
  - ‘90
- ArF scanners
  - SiON
  - Spike RTA
  - Channel strain
  - USJ co-I/I
  - Immersion litho
  - GL: HK / MG
  - ‘00

- HK / MG
  - Multi-Gate
  - SMO
  - TSV
  - EUV scanner
  - FBRAM
  - Super-HK
  - VFET
  - III-V channel
  - Mask-less
  - Air-gap
  - RRAM
  - 3D-NAND
  - TANOS
  - SAM
  - HTFET
  - CNT
  - Graphene
  - System/Circuit
  - ‘10
Transistor scaling
Power... Performance... Area
Device power
From switch to dimmer

Gate oxide leakage or tunneling current
- As oxide thins down leakage increases exponentially

Need new materials and/or new architectures!
Device power
How to tackle the problem?

Solution → new materials
e.g. high-K dielectric

Constant Capacitance Density
\[ C = \frac{\varepsilon_0 \varepsilon_{\text{SiO}_2}}{t_{\text{SiO}_2}} = \frac{\varepsilon_0 \varepsilon_{\text{hk}}}{t_{\text{hk}}} \]
\[ t_{\text{high-k}} = \frac{\varepsilon_{\text{hk}}}{\varepsilon_{\text{SiO}_2}} \times t_{\text{SiO}_2} \]

Direct tunneling
Oxides < 3 nm

Year

Atomic Layers
~ 90 Layers
~ 5 nm
~ 1 nm
3 Layers
1 nm
(schematic)
High-\(\kappa\) / metal gate

Gate **First** High-\(\kappa\)/Metal Gate

Gate **Last** High-\(\kappa\)/Metal Gate

\[ \text{EWF (eV)} \]

\[ \text{GF} \]

\[ \text{EOT (Å)} \]

- AlO-cap (p-EWF)
- uncapped high-k dielectric
- La-cap (n-EWF)

RMG

P-EWF

N-EWF
**Device power**

*From switch to dimmer*

Sub-threshold leakage

- Short channel forms no effective barrier
- Threshold voltage not scaling as fast as $V_{DD}$

Need new materials and/or new architectures!
Fully depleted devices

Solution → New Architecture
e.g., Fully Depleted Devices
for better short-channel control
Transistor scaling
Power... Performance... Area
Device scaling roadmap

Performance
(power x delay)

- Strain, USJ (F,C co-implant, …)
- 90-65-45
- 32-22/20
- 22/20-15 Multi-gate
- 11-7
- High-k, Metal Gate
- Ge/III-V, VFET, TFET, NW, Graphene…

Gate-first
Gate-last
FinFET
FUSI
SiGe strain
USJ silicide

Gate Spacing
Active Area
Gate Field
Spacers

>130

imec
Device performance
Strain engineering and high-mobility channels

<table>
<thead>
<tr>
<th>Material</th>
<th>Hole mobility (cm²/Vs)</th>
<th>Electron mobility (cm²/Vs)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Si</td>
<td>430</td>
<td>1600</td>
</tr>
<tr>
<td>Ge</td>
<td>3900</td>
<td>3900</td>
</tr>
<tr>
<td>GaAs</td>
<td>400</td>
<td>9200</td>
</tr>
<tr>
<td>InAs</td>
<td>500</td>
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Hole mobility (cm²/Vs)
Electron mobility (cm²/Vs)

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**Graphical Representation:**
- **Device performance chart:** Showing various performance metrics like DIBL and LG_physical for different channel materials.
- **Table with material properties:** Highlighting the mobility values for Si, Ge, GaAs, and InAs.
- **Graph with data points:** Illustrating the performance of SiGe-45% with implants, REF IFQW SiGe 45%, and IFQW SiGe 45% + eSiGe under specific conditions.

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**Key Points:**
- **Hole and Electron Mobilities:**
  - Si: 430 cm²/V·s, 1600 cm²/V·s
  - Ge: 3900 cm²/V·s, 3900 cm²/V·s
  - GaAs: 400 cm²/V·s, 9200 cm²/V·s
  - InAs: 500 cm²/V·s, 40000 cm²/V·s
- **Graphical Data:**
  - DIBL [mV/V] vs. LG_physical [nm]
  - Ioff_drain [µA/µm] @ VG=0V
  - Ion [µA/µm] @ VG=-1V
- **Performance Metrics:**
  - REF. SiGe-45% with implants
  - REF. IFQW SiGe 45%
  - IFQW SiGe 45% + eSiGe

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**Legend:**
- REF. SiGe-45% with implants
- REF. IFQW SiGe 45%
- IFQW SiGe 45% + eSiGe

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**Additional Information:**
- W=10um, V_DD=-1V
- DIBL [mV/V] vs. LG_physical [nm]
- Ioff_drain [µA/µm] @ VG=0V
- Ion [µA/µm] @ VG=-1V

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**Graphical Analysis:**
- The graph shows a comparison of performance metrics for different channel materials and modifications.
- The table provides a clear overview of mobility values for various materials.

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**Conclusion:**
- The chart and table together provide a comprehensive view of device performance under strain engineering and high-mobility conditions.
Device performance
Strain engineering and high-mobility channels

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<td>InAs</td>
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Hole mobility
Electron mobility

- IFQW SiGe 45%
- REF IFQW SiGe 45%
- IFQW SiGe 45% + epi S/D booster 25%

Device performance

W=10um, VDD=-1V
I_{on} = 1mA/um

\[ I_{off\_drain} @ V_G=0V (\mu A/\mu m) \]
\[ I_{on} @ V_G=-1V (\mu A/\mu m) \]
Selective (in STI trenches) III/V QW MOSFET

Key Characteristics

“ART” (Aspect-Ratio-Trapping) with InP-on-Si buffer
MOCVD 8” Epi (AIXTRON), with raised (n+)-InGaAs S/D

First functional transistor characteristics!
Work on-going for further improvement in buffer defectivity and doping (insulation)
High mobility channel materials
Co-integration with standard Si CMOS

1. **Selective growth** of (Si)Ge and/or III/V in STI trenches
2. **High-κ gate stack** for low EOT
3. Self-aligned **doped raised S/D** for contacts
4. Further **strain engineering** for mobility boost
High hole mobility for III-Sb p-channel

InSb followed by GaSb has the largest hole mobility compared to Ge, InGaAs and GaAs

Optimized structural stack quality

The **AISb interfacial layer** plays a key role in the growth of high quality QW stack.
What’s next?

- **Gate stack**:
  - Poly SiON Si-subst.
  - MG High-k Si-subst.
  - MG High-k Si substrate

- **Electrostatic control**:
  - bulk

- **Transport enhanced**:
  - stressors

- **Node**
  - 45nm (2003)
  - 32nm (2005)
  - 22nm (2007)
  - 15nm (2009)
  - 11nm (2011)
  - 7nm (2013)
  - 5nm (2015)

- **Year (in production)**
  - 2005 (2009)
  - 2007 (2011)
  - 2009 (2013)
  - 2011 (2015)
  - 2013 (2017)
  - 2015 (2019)

- **What's next?**
  - MTJ logic Switch
  - Spintronics BIFSET
  - Pinch-Off FET
  - Ge TFET
  - InAs TFET
  - Graphene FET
  - Spin Torque

**Node**

- **Poly**
  - SiON
  - Si-subst.

- **MG**
  - High-k
  - Si substrate

- **Si substrate**
  - 5 nm

- **Gate**
  - Hard mask
  - 16nm In
  - 40nm gate

- **Fin**
  - Multi-gate

- **Si substrate**
  - MG High-k
  - III/V ch.
  - Si-subst.

- **III/V & Ge channels**

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Exploratory devices: TunnelFETs

Heterojunction TFET boosts the ON current by increasing the source tunneling efficiency by using low bandgap material in the source.

Tunnel-FET basic idea: use the band-to-band tunneling in p-i-n device as an energy filter to overcome the 60mV/decade subthreshold slope limitation.

ON/OFF switching determined by band-to-band tunneling at source side.
Exploratory devices: TunnelFETs

- Extensive modeling effort to calibrate tunneling efficiency (using P-i-N diodes)
- Enable exploration of new device concepts
- Integration of demonstrators (vertical & horizontal) in progress

Drain-source current vs. Drain voltage:
- $E_{\text{max}} \approx 10^6 \text{ V/cm}$
- $E_{\text{max}} \approx 3 \times 10^6 \text{ V/cm}$
The pinch-off nanowire MOSFET
A junctionless device

- Negative gate voltage will push the majority carriers (electrons) to the middle of the wire. For sufficient negative gate voltage the channel is pinched off.
- No source and drain needed

Bulk (volume) transport vs interface transport
Difference in charge density leads to difference in transport type

DIBL (nPOFET) ≈ DIBL (nMOSFET) ≈ 177 mV/V
SS (nPOFET) ≈ SS (nMOSFET) ≈ 60 mV/dec
Integration of CVD graphene

~1x1 cm² die w/TaN markers
E-beam lithography
Liftoff metallisation
O₂ plasma etching
Integration of CNTs in interconnects

Demonstration of CNT interconnects in VIAs and contacts

DRAM Capacitor scaling: EOT and physical thickness scaling at target leakage current

New high-k dielectrics with $k > 100$ and noble metal electrodes with large WF required to enable DRAM scaling below 20 nm node
FLASH scaling challenges

Floating Gate scaling: cell interference and coupling ratio (CR) reduction are the major issues when scaling and planarizing the floating gate (FG) Flash memory cell.

High-k dielectrics for Inter Poly Dielectric to increase CR & FG stack engineering required to enable Flash scaling below 20 nm
Memory program: some achievements

**DRAM**

- Best in class EOT/Jg with IMEC's engineered stack

**RRAM**

- Applying TDDB know how to RRAM filament formation

**FBRAM**

- V<sub>DS</sub>=1.5v demonstrated with double wordline cell architecture

**3D- FLASH**

- 10k cycles and retention on 22nm Si diameter demonstrated
Moore’s law & transistor scaling

1965

2002-2003
~ 90 nm

~ 16-14 nm

Lithography Enabled Scaling

Materials Enabled Scaling

3D Enabled Scaling
3D stacked interconnect
Impact TSV proximity on transistor

Keep-Out-Zone determined to minimize TSV impact on CMOS device using TCAD model in combination with experimental data.

Single TSV at 1.7um

- pMOS
  - ~ 4% Ion variation near TSV, causes DAC disfunctions

- nMOS
  - ~ 0.6% Ion variation near TSV, limited impact on DAC

Transverse Direction

Delta Ion, %

Distance From TSV Along Y, um

AR 8:1 TSV

P @Si
P @model
N @Si
N @model
3D Design path finding tool

Path-finding

- Fast prototyping tool trades accuracy for rapid turn-around
- Based on early compact models and design rules
- Output spatially aware estimate of performance and power
- Output data for cost and thermal evaluation
- Output specs for design authoring tools
Optical interconnects roadmap

Transition driven by:
- Signal integrity
- Power
- Form factor
- Cost

OPTICAL BACKBONE
Optical interconnects roadmap

Silicon Interposer:
- Chips Stacking
- Optical Connectivity
Si photonics

E-O-E transceiver: Key Features

- Single platform integrating all optical functionalities
- CMOS-like fabrication processes
- Small photonics component footprint
- 3D connectivity to CMOS wafers for improved O-E performance
Si photonics
Passive components library

All devices are fabricated on the same platform
More Moore vs More than Moore

CMOS Scaling

CMORE
Multi-functional SOC/SIP

Interconnects

FEOL Device roadmap

Low k

FinFET

HfO$_2$

strain

metal gate

SiGe

NiSi

25 nm

FUSI

optical detectors

Thermal sensors

Chemical sensors

Micro Mirrors

Bio-Electronic interface

Battery

MEMS

RF Chip

DNA Chip

Image Sensor

Processor

Memory

Source: SAMSUNG

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## MEMS technology options

For tight integration with driver IC

<table>
<thead>
<tr>
<th>SIP: Stacked die</th>
<th>SIP: F2F</th>
<th>SIP: 3D vias</th>
<th>SoC: monolithic</th>
</tr>
</thead>
<tbody>
<tr>
<td>Interconnect pitch</td>
<td>~ 50 um</td>
<td>~10um</td>
<td>~10um</td>
</tr>
<tr>
<td>Interconnect parasitics</td>
<td>few pF</td>
<td>&gt;100fF</td>
<td>&lt;100fF</td>
</tr>
</tbody>
</table>

**Monolithic approach:**
- Most compact solution
- Best solution when needing high density interconnect and low parasitics
- Requires compatible die sizes

**3D stacking**
- Wirebond, flip chip, TSV depending on interconnect density and parasitics
- Offers more choices in MEMS technologies and die size combinations
### Poly-SiGe:
- better mechanical properties than Al: higher strength and Q factor
- better reliability properties than Al: less creep and fatigue

### Different above CMOS MEMS approaches

<table>
<thead>
<tr>
<th></th>
<th>Al</th>
<th>Poly-SiGe</th>
</tr>
</thead>
<tbody>
<tr>
<td>Post CMOS integration</td>
<td>yes</td>
<td>yes</td>
</tr>
<tr>
<td>Fracture strength [GPa]</td>
<td>0.2</td>
<td>&gt; 2</td>
</tr>
<tr>
<td>Mechanical Q</td>
<td>low</td>
<td>&gt; 10,000</td>
</tr>
<tr>
<td>Reliability</td>
<td>creep: hinge memory effect</td>
<td>No creep</td>
</tr>
</tbody>
</table>
11 Mega pixel micro mirror chip

- 11M pixel MEMS + CMOS integration
- 8x8 µm pitch on SiGe platform (Al coating)
- 6 kHz update rate
- Analog tilt angle control
- Extreme mirror flatness <10 nm
- No mirror fatigue & creep

No fatigue!

3.10^{12} cycles

No Creep!

4.6 cm

2.2 cm

0.18um HV CMOS
Sensors everywhere

The 2010 Trend Watch Sensor Survey Results

HOT SENSOR TECHNOLOGIES

<table>
<thead>
<tr>
<th>Technology</th>
<th>Percentage</th>
</tr>
</thead>
<tbody>
<tr>
<td>Wireless sensor networks</td>
<td>60%</td>
</tr>
<tr>
<td>Ultra-low-power sensors</td>
<td>46%</td>
</tr>
<tr>
<td>Plug-and-play sensors</td>
<td>42%</td>
</tr>
<tr>
<td>MEMs sensors</td>
<td>35%</td>
</tr>
<tr>
<td>Energy harvesting sensor networks</td>
<td>31%</td>
</tr>
<tr>
<td>Pulse-width-modulated output sensors</td>
<td>14%</td>
</tr>
<tr>
<td>Sensor fusion</td>
<td>13%</td>
</tr>
<tr>
<td>Other</td>
<td>5%</td>
</tr>
</tbody>
</table>


Underlying the Internet of Things are technologies such as RFID, sensors and smart-phones
Vision for sensor development

Mission statement:

Development of ultra-low power micro/nanosensors for (bio-) chemical detection including the required read-out and driver circuits implemented in standard cleanroom environment

Main targets

- Increased sensitivity and/or selectivity
- Ultra-low-power (< 20mW)
  → energy autonomous
- Miniaturized integrated sensors
- Cost-effective fabrication
Body area networks examples
Personal healthcare & lifestyle solutions

Necklaces/patches  Watch-type  Headsets  Base Stations
e-Nose
Advanced sensing in complex environments

Human olfactory system

e-nose: array of non-specific, cross-reactive sensors combined with an information processing system

Target Agent | Sensor Array | Agent Identification

\[
\frac{\Delta f_n}{f_n} = \frac{1}{2} \left( -\frac{\Delta m}{m} + \frac{\Delta k}{k} + \frac{\alpha_n \Delta \sigma}{1 + \alpha_n \sigma} \right)
\]

Adsorption | Extra mass | Swelling | Stress | Lower Frequency

Beam vapors polymer
e-Nose: low power is the key

Die = 8.8 mm x 8.8 mm, 160 resonators

w = 65 µm
L = 750 µm
h = 500 nm
Coating: PMMA
Transduction: Piezoelectric actuation/detection
Power = 0.00017 mW
(170 nW)

10⁻⁵ frequency shift / %EtOH

2.6 10⁻³ frequency shift / %EtOH

10,000 times more power efficient
260 times responsivity increase
Energy storage

Storage for micro systems:
- All Solid-State devices (integrated systems)
- Microelectronic fabrication techniques

Size determines total capacity:
- High energy density even more important for small form systems
Module development:

- 3D-TF Ucap
- 3D-TF battery half-cell (wet)
- Solid electrolytes
- SS 3D-TFB
- Integrated batteries

Application drivers:

- Decaps on interposer (3D)
- Solid-State Ultracapitors
- Prismatic Battery cells targeting high-P with competitive E-density
- Battery cells targeting durability and safety (extended temperature window)
- Battery on foil (large area)
- Small-form batteries, micro batteries
- Smart solar modules
- Microsystems
- Autonomous wireless sensors (WATS)
Conclusions

Nano-electronics will continue to drive innovation in many fields.

Societal progress will be enabled by the merger of nano-electronics, nano-technologies, bio sciences and energy efficient technologies.

Global collaboration including entire value chain is required to address the huge R&D challenges.