Semiconductor Technology Research, Development, & Manufacturing: Status, Challenges, & Solutions

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A New Paradigm in the Making?

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Agenda

- Semiconductor Revenue Growth: Yes!
- Realize Which Roadmap?
- Technology Challenges
- R&D Cost
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- **Semiconductor Revenue Growth: Yes!**
  - Historical Perspective & Extrapolation

- **Realize Which Roadmap?**
  - End Equipment & Product
  - Cost per Function

- **Technology Challenges**
  - Mask Availability, Cost, Cycletime
  - Post – 193nm Exposure Technology
  - New Materials

- **R&D Cost**
  - How Many Si Tech R&D Centers Can the Industry Support?
  - R&D Foundries, Partnerships, & Alliances Win!
Semiconductor Industry Revenue Growth Summary

- 17% CAGR in the 70’s and 80’s
- Drove High Rates of Capital Investment and R&D
  - In Turn Drove Better Penetration of Existing Markets and the Opening of New Ones
    - In Turn Drove Revenue Growth
- This is a Cyclical Growth Industry with a 5-Year Period
- Maturation is Occurring
  - But not that Fast!
Projections from a Historical Study of Industry Growth Trends

Models Based on Growth of Auto Industry 1900 - 2000

Revenue ($B)


Year

Models

History

Pessimistic

Optimistic

Cyclical Model

14%

10%

16%

20+%
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End Equipment (PCs, DVDs, Hand-helds, Wireless)

Products (µPU, DRAM, DSP, Baseband)

Modules (Logic, Memory, Analog)

Specifications (V_{DD}, Freq., Pwr., Cost, Lifetime)

Layout/Architecture (Random, Gate Array, Logic-Based, Memory-Based)

Materials/ Structures (Cu, Low K, SOI, ½ Pitch)

Processes/Tools (193nm, CMP)

Requirements

Solutions

ITRS
Too Much Focus on the Lower Level “REQUIREMENTS” can Drive Unprofitable Investments, i.e. Low K Interconnects
Commodity DRAM Product Roadmap

- Capacity (MBits)
- Year

- Commodity DRAM Doubles Every 24 Mos.
- Doubles Every 18 Mos.
Commodity DRAM & Embedded SRAM Product Roadmap

- **Commodity DRAM**
  - Doubles Every 24 Mos.
  - Doubles Every 18 Mos.

- **Embedded SRAM**
  - Doubles Every 24 Mos.
  - Doubles Every 18 Mos.
Manufacturing Cost per Function Roadmaps

- Driven by Transistors per Area and Cost per Area

<table>
<thead>
<tr>
<th></th>
<th>2-Year Cycle</th>
<th>3-Year Cycle</th>
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<tbody>
<tr>
<td>Annual Transistor</td>
<td></td>
<td></td>
</tr>
<tr>
<td>per Unit Area Increase</td>
<td>40%</td>
<td>25%</td>
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<tr>
<td>Average Cost per</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Unit Area Increase</td>
<td>8%</td>
<td>4%</td>
</tr>
<tr>
<td>– Constant Wafer Size</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Average Cost</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Reduction for Wafer Size Conversion</td>
<td>4%</td>
<td>4%</td>
</tr>
<tr>
<td>Every 10 Years</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Predicted Annual Cost per Function Decrease</td>
<td>27%</td>
<td>21%</td>
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2-Year Cycle Wins!
Validated ISMT Cost per Function Model

Slope Change in 1998 due to 2-Year Cycle
300mm Cross-Over Predicted in 2004

Graph showing the cost per function over years with points indicating a 20% per year reduction and 27% per year reduction. Key points are 0.35 µm Y3, 0.25 µm Y2, 0.18 µm Y2, 0.13 µm 300mm, and 0.13 µm Y3.
Major Technology Challenge: The Sub – \( \frac{1}{2} \) Wavelength Red Zone

Driving High Mask Cost
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Mask Issues

• Phase Shift & OPC Requires 2x+ Resolution Improvement

• Infrastructure Development Cost not Supported by Revenue

• Database Size Exploding

• Cost Going up 2x per Generation
  – Manufacturing 130nm $ 600K
  – 90nm $1200K
  – 65nm $2400K?
Mask Cost Analysis 130nm to 90nm
Only Manufacturing Considered

Cost per Equivalent AT Wafer

Cross-Over at 500 Wafers
Smart Gate Arrays Become More Attractive

Cost per Equivalent AT Wafer

Advanced Technology Equivalent Wafers

Cross-Over at 1500 Wafers
Summary of Top Technical Challenges

- Mask Availability, Cost, and Cycletime
  - Especially for Custom Products

- Post 193nm Litho Exposure Tools
  - 157nm in Mainstream Production in 2006/2007
  - EUV in Mainstream Production in 2009/2010

- New Materials
  - Low K’s
  - High K’s
  - Memory Materials
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The New Economy for Microelectronics

- A New Factory (Fab) Runs 130nm Technology with Cu Wiring at 300mm
- **At a Capital Cost of $2B - $4B**
  - *Increasing at a Rate of 15% per Year*
- Technology R&D to Support 2-Year Major & 1-Year Minor Product Cycles
- **At a Cost of > $500M per Year for a Tier 1 Logic Manufacturer**
  - *Increasing at a Rate of > 20% per Year*
Table Stakes for Independent Semiconductor Manufacturer

- Cap Ex of $1B per Year or Min. of 20% of Revenues
  - Implies Revenues of $5B/yr

- Technology R&D Investment of $500M per Year
  - If Requirement of <5% of Revenues for IDM Implies Revenues of $10B/yr
R&D Partnership Risks & Rewards

• **Rewards**
  – Faster Speed of Execution
  – Lower Costs

• **Risks**
  – Sacrifice of IP & Potential Competitive Advantage
  – Cultural, Geographic, and NIH Factors can Slow Progress
  – Divergence of Interests
Summary

• **Semiconductor Revenue Growth: Yes!**
  – > 10% CAGR Through the Decade

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• **R&D Cost**
  – Consolidation of Si Tech R&D Centers Required
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Addenda
Killer App for the Future?

- **Enabler Products**
  - Broadband
  - 3+G Wireless

- **Voice Recognition**
  - No Keyboards

- **BioMedical Electronics**
  - Reduced Cost of Health Care

- **Enabler Technologies**
  - MEMS (MicroElectroMechanical Systems)
  - NanoTechnology - NanoElectronics
  - Biotechnology - BioElectronics