Recent advances in lithography and high level metrology needs for lithography

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Acknowledge: Ben Bunday Andrew Grenville, Stefan Wurm, Kim Dean, Jonathan Cobb, and Sergei Postnikov
Outline

- Future lithography in next five years
  - Overview of immersion lithography
  - Overview of EUV lithography
- CD and LWR control for lithography
- DFM and metrology needs
Resolution of Optical Lithography

\[ HP_{\text{MIN}} = k_1 \left( \frac{\lambda}{NA} \right) \]

Finer resolution can be achieved by:
- Shorter wavelength (436 nm…365 nm …248 nm…193 nm…13.5 nm)
- Increased numerical aperture
  - Immersion with NA>1
- Reduced \( k_1 \)
  - Improved masks (CD control, Phase Shift masks)
  - Improved lenses (aberrations)
  - Better photoresists
  - Better process controls
  - Resolution Enhancement Techniques (RET)
General requirements for lithography

• Critical dimension (CD) control
  – Size of many features in a design needs to be accurate and precise
  – CD control needs to be maintained within each exposure field, over each wafer and from wafer to wafer

• Overlay
  – The placement of the image with respect to underlying layers needs to be accurate on each integrated circuit in all locations

• Defect control
  – The desired pattern must be present in all locations, and no additional patterns should be present.
  – No particles should be added to the wafer during the lithography process.

• Low cost
  – The cost of tools and masks needs to be as low as possible while still meeting the CD control, overlay and defect control requirements
  – The lithography step should be performed as quickly as possible
  – Masks should be used to expose as many wafers as possible
  – Equipment needs to be reliable and ready to expose wafers when needed

Metrology plays a critical role in all of these requirements.
Notes: EPL is a potential solution at the 65, 45 and 32-nm nodes for one geographical region, and PEL is a potential solution at the 32-nm node for one geographical region. RET will be used with all optical lithography solutions, including with immersion; therefore, it is not explicitly noted.

Unofficial version of Figure 34; Not for publication
Resolution Improvement by Immersion

\[ HP_{MIN,DRY} = \frac{1}{4} \frac{\lambda_{RESIST}}{\sin \alpha_{RESIST}} \]
\[ = \frac{1}{4} \frac{\lambda_{AIR}/n_{RESIST}}{\sin \theta/n_{RESIST}} \]
\[ = \frac{1}{4} \frac{\lambda_{AIR}}{\sin \theta} \]

\[ HP_{MIN,WET} = \frac{1}{4} \frac{\lambda_{RESIST}}{\sin \beta_{RESIST}} \]
\[ = \frac{1}{4} \frac{\lambda_{AIR}/n_{RESIST}}{n_{LIQUID} \sin \theta/n_{RESIST}} \]
\[ = \frac{1}{4} \frac{\lambda_{AIR}}{\sin \theta/n_{LIQUID}} \]
Earlier increase in index of fluid and/or resist yields process latitude improvement.
193i Technology (45nm Half Pitch)

- **High Index Fluid**: Fluid Standards, Immersion Defectivity, Fluid Handling, Thermal Control
- **Enabling NA>1.45**: Hyper NA, CaF2, Fused Silica, Final Optic Durability / Contamination
- **Laser**, **Overlay**, **Productivity**
- **Pattern Generator**, **Pattern Transfer**, **Mask CD Metrology**, **Placement Metrology**
- **Mask Defect Control**: Defect Inspection, Repair, Defect Review, Cleaning, Pellicle
- **Leaching**, **Resolution**, **LWR**, **Sensitivity**, **Process Capability**
- **Double Exposure**, **Layout / DFM**
- **CDSEM**, **Overlay**
- **EXPOSURE TOOL**
- **MASK**
- **RESIST**
- **LOW k_1**
- **METROLOGY**

**Platform**

- Addressed in part by ISMT
- Addressed by others
- Potential Showstopper / Requires Invention
- Critical Issue / Development Required
- Solution Known

**193i**
Extreme Ultraviolet Lithography (EUV)

- All optics surfaces coated with multilayer reflectors (40-80 layer pairs, each layer approx \( \lambda/4 \) thick, Control \( \sim 0.1 \) Å)
- Ring Field Illumination
- Scanning mask and wafer stages
- Flat, square mask with multilayers

Reflective Reticle

Laser Produced Plasma

Condenser Optics

4X Reduction Optics

EUV imaging with ultrathin resist (UTR)

Reflective Optical Surfaces are Aspheric with Surface Figures & Roughness < 3 Å

\( \lambda = 13.5 \) nm
EUV Mask Technology

Patterned Absorbers
~ 50-100 nm thick (e.g. Al, Cr, TaN, W)

Buffer Layer
~ 30-50 nm thick (e.g. SiO₂)

Capping Layer
Ru (2nm) or Si (11nm)

Reflective Multilayers
~ 300 nm thick (Mo - Si = 13.5nm)
40 - 50 Pairs

Low thermal expansion material (LTEM) substrate

Full Field 6” EUV Mask with 100-nm node CMOS
Multilayers: Mo - Si
Absorber Stack: Cr/SiON
120 mm x 104 mm field size
(Courtesy of P. Mangat & S. Hector, Motorola)

• Key challenges for EUV mask multilayers
  – High uniformity of thickness
  – No printable defects
  – Temperature stability
### Immersion and EUV Tool Timing

#### 193 Immersion

<table>
<thead>
<tr>
<th>Year</th>
<th>Q1</th>
<th>Q2</th>
<th>Q3</th>
<th>Q4</th>
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<td>2003</td>
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<tr>
<td>2008</td>
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</table>

- **Exitexh**: 0.85NA (RIT), 1.05NA (RIT), 1.3NA (ISMT), >1.4NA
- **ASML**: 0.75NA, 0.85NA, >0.9NA, >1NA
- **Canon**: 0.75NA, 0.85NA, 0.92NA, >1NA
- **Nikon**: 0.85NA, 0.92NA, >1NA, >> 1NA

#### EUV

<table>
<thead>
<tr>
<th>Year</th>
<th>Q1</th>
<th>Q2</th>
<th>Q3</th>
<th>Q4</th>
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<tr>
<td>2004</td>
<td>Exitech MET</td>
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<tr>
<td>2005</td>
<td>ASML &lt; 10 wph</td>
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<tr>
<td>2006</td>
<td>ASML 30 wph</td>
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<tr>
<td>2007</td>
<td>ASML 80 wph</td>
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<td>2008</td>
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<td></td>
<td></td>
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<tr>
<td>2009</td>
<td></td>
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</table>

- **Exitech MET**
- **ASML < 10 wph**
- **ASML 30 wph**
- **ASML 80 wph**
- **Nikon High NA set 3**
- **Nikon Beta**
- **Canon < 10wph**
- **Canon 60wph**
2004 ITRS lithography requirements are challenging

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<td>Technology Node</td>
<td>hp90</td>
<td>hp65</td>
<td>hp45</td>
<td>hp32</td>
<td>hp22</td>
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<tr>
<td>DRAM ½ Pitch (nm)</td>
<td>90</td>
<td>65</td>
<td>45</td>
<td>32</td>
<td>22</td>
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<tr>
<td>MPU/ASIC Metal 1 (M1) ½ Pitch (nm)</td>
<td>107</td>
<td>76</td>
<td>54</td>
<td>38</td>
<td>27</td>
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<tr>
<td>MPU Gate in resist Length (nm)</td>
<td>53</td>
<td>35</td>
<td>25</td>
<td>18</td>
<td>13</td>
</tr>
<tr>
<td>MPU Gate Length after etch (nm)</td>
<td>37</td>
<td>25</td>
<td>18</td>
<td>13</td>
<td>9</td>
</tr>
<tr>
<td>Gate CD control (3 sigma) (nm)</td>
<td>3.3</td>
<td>2.2</td>
<td>1.6</td>
<td>1.2</td>
<td>0.8</td>
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<tr>
<td>Overlay</td>
<td>32</td>
<td>23</td>
<td>18</td>
<td>13</td>
<td>8.8</td>
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<tr>
<td>Mask CD uniformity (nm, 3 sigma) isolated lines (MPU gates), binary mask</td>
<td>3.8</td>
<td>2.2</td>
<td>2</td>
<td>1.3</td>
<td>0.5</td>
</tr>
<tr>
<td>Line Width Roughness (nm, 3 sigma) &lt;8% of CD</td>
<td>4.2</td>
<td>2.8</td>
<td>2</td>
<td>1.4</td>
<td>1</td>
</tr>
</tbody>
</table>

- Gate CD control is intended to represent total CD variation
  - Is it possible to meet the desired gate CD control values?

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known
Manufacturable solutions are NOT known

Accelerating the next technology revolution.
Major CD error sources

• Intrafield
  – Dose uniformity
  – Focus uniformity
  – Aberration variation within the field
  – Mask CD uniformity
  – Imperfect optical proximity correction (OPC)
  – Flare variation for EUV

• Interfield
  – PEB temperature variations
  – Dose variation
  – Mean focus variation

Metrology critical to identifying and reducing systematic errors
Calculated CD variation at 45nm half pitch

- Both 193nm immersion and EUV ($k_1=0.83$) will probably not meet ITRS requirements.
- Under near ideal optical lithography conditions, 193nm immersion at near maximum NA with water ($k_1=0.31$) with AltPSM may provide better CD control if EUV flare variation is not fully compensated.
Importance of Line Edge and Width Roughness

- **Line Edge Roughness (LER)** (High frequency roughness)
  - Can affect dopant concentration profiles
  - Probably affects interconnect resistance

- **Line Width Roughness (LWR)** (Mid-frequency roughness)
  - Leakage of transistors affected
  - Affects device speed of individual transistors
  - Leads to IC timing issues

Example: poly-silicon line

Edge assignment from SEM algorithm

Fourier PSD, averaged

Ben Bunday, SEMATECH
Areas of potential device impact

- Front end patterning
  - LWR after etch is what matters, not LWR in resist
  - LWR affects leakage current more strongly than drive current

Eric Verret, Aaron Thean and Jonathan Cobb; Freescale Semiconductor
Trends to manage CD control and yield

• Present approaches are not enough
  – More stringent design rule restrictions
  – Single orientation, pitch restrictions
  – Larger CD on resist
  – Relaxed minimum half pitch
  – Use of resolution enhancement technology (RET)
  – Field by field and within field dose corrections

• Further actions--DFM
  – Automation of software analysis of weak spots in design and feedback to physical layout of cells
    • RET applied to library cell layouts
  – Coordinates of weak points provided to mask and wafer CD metrology tools
    • Focus and exposure are optimized for printing hot spot regions with maximum process latitude rather than for CD of CD bars.
  – Identification of critical timing paths to locally specify CD control
  – Test programs optimized to detect electrical effects at weak points
  – Local corrections of mask to account for variations of scanner—mask specification to particular scanners
  – Software for reduction of slivers in design data is also being developed to reduce mask CD error and writing time.

Based on IBM, Intel, ASML and Toshiba presentations at SPIE and PMJ
Present mode of operation for circuit design and fabrication

Organizational, corporate cultural and geographical barriers

Circuit architecture

Device models

Design rules

Masks

Packaged IC

Test data

Wafer fab
Incorporating design intent in new ways

- Vary intensity of RET based on location in circuit with respect to critical timing paths
- Increase metrology and decrease allowed tolerances where most needed

Mark shapes in layout that affect critical circuit timing (shown in red)

Without DFM (RET applied uniformly)

With DFM (RET applied where needed)
Incorporating design intent in new ways

- Optimize floor plan based on critical timing paths
- Place and route optimized based on critical timing paths

Known contours of CD, topography or overlay error with mfg. process

Potential problems areas marked where critical timing paths exist in regions with large variations

Change layout to move critical timing paths to areas without smallest errors

Accelerating the next technology revolution.
New mode of operation with design for manufacturing (DFM) practices

Circuit architecture

Device models

Design rules

Process variation distributions

Known contours of CD, topography or overlay error with mfg. process

Test data

Packaged IC

Wafer fab
Conclusions

• 193nm immersion and EUV lithography are promising candidate technologies for 45-nm and 32-nm half-pitch patterning
  – Significant challenges remain in developing either technology to provide a timely, economical manufacturing solution

• Maintaining ±10% CD control doesn’t appear to be possible
  – Metrology precision improvements critical to reducing systematic errors

• Measuring and controlling LWR and LER becoming increasingly important

• Increasing integration of design, lithographic resolution enhancement techniques and extensive metrology will be needed to maintain expected circuit performance
  – DFM drives need for improved precision and throughput