Metrology Requirements and the Limits of Measurement Technology for the Semiconductor Industry

Based on the International Technology Roadmap for Semiconductors

Alain C. Diebold
Measurements Today
Atomic Dimensions
Nanowire Transistor & Interconnection

Opportunity for cross-work between industry and university
AGENDA

• The ITRS Challenge
• Litho Metrology
• FEP Metrology
• Interconnect Metrology
• Materials Characterization
ITRS Challenge

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>DRAM ½ Pitch</td>
<td>130 nm</td>
<td>115 nm</td>
<td>90 nm</td>
<td>65 nm</td>
<td>45 nm</td>
<td>32 nm</td>
<td>22 nm</td>
</tr>
<tr>
<td>MPU / ASIC ½ Pitch (nm)</td>
<td>150</td>
<td>130</td>
<td>90</td>
<td>65</td>
<td>45</td>
<td>32</td>
<td>22</td>
</tr>
<tr>
<td>MPU Printed Gate Length (nm)</td>
<td>90</td>
<td>75</td>
<td>53</td>
<td>35</td>
<td>25</td>
<td>18</td>
<td>13</td>
</tr>
<tr>
<td>MPU Physical Gate Length (nm)</td>
<td>65</td>
<td>53</td>
<td>37</td>
<td>25</td>
<td>18</td>
<td>13</td>
<td>9</td>
</tr>
</tbody>
</table>

Leading Edge Tool Specifications set

45 nm Node Metrology R&D
Materials available
10 nm structures difficult to obtain
Process control is based on Statistical Significance.

If Distribution is Centered

\[ CP = CP_k \]

\[ CP < 1 \]

\[ CP = 1 \]

\[ CP > 1 \]

EFFECT OF P/T ON MEASURED Cp

<table>
<thead>
<tr>
<th>ACTUAL Cp</th>
<th>MEASURED Cp/ACTUAL Cp</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.75</td>
<td>100%</td>
</tr>
<tr>
<td>1</td>
<td>90%</td>
</tr>
<tr>
<td>1.25</td>
<td>80%</td>
</tr>
<tr>
<td>1.5</td>
<td>70%</td>
</tr>
<tr>
<td>1.75</td>
<td>60%</td>
</tr>
<tr>
<td>2</td>
<td>50%</td>
</tr>
<tr>
<td>2.25</td>
<td>40%</td>
</tr>
<tr>
<td>2.5</td>
<td>30%</td>
</tr>
</tbody>
</table>

- P/T=0.1
- P/T=0.2
- P/T=0.3
- P/T=0.5
- P/T=0.7
- P/T=0.8
- P/T=1.0

Process control is based on Statistical Significance.
What are you Measuring?

- single value from distribution
- average

Distribution of linewidths inside test structure

test structure inside a die
One Aspect of the Solution:
Average over large area & Amplify Signal from Microscopic Changes

- e.g.
  - 150 nm lines
  - 300 nm pitch

Optical CD using Overlay System

Rapid Sampling of test structures
AGENDA

• How to control microscopic features
• Litho Metrology
• FEP Metrology
• Interconnect Metrology
• Materials Characterization
Litho Metrology

CD Control Starts at the Mask

Overlay and CD Control after Exposure

22 nm Node - 2016

52 nm mask line width
26 nm scattering bars

CD Control after Etch

13 nm printed line width

9 nm physical line width
## Litho Metrology

### Technology Node

<table>
<thead>
<tr>
<th>Technology Node</th>
<th>130 nm</th>
<th>90 nm</th>
<th>65 nm</th>
<th>45 nm</th>
<th>32 nm</th>
<th>22 nm</th>
<th>Driver</th>
</tr>
</thead>
</table>

#### Lithography Metrology

<table>
<thead>
<tr>
<th>Printed Gate CD Control (nm)</th>
<th>5.3</th>
<th>3</th>
<th>2</th>
<th>1.5</th>
<th>1.1</th>
<th>0.7</th>
<th>MPU</th>
</tr>
</thead>
<tbody>
<tr>
<td>Wafer CD 3σ Precision P/T=0.2</td>
<td>1.1</td>
<td>0.6</td>
<td>0.4</td>
<td>0.3</td>
<td>0.2</td>
<td>0.1</td>
<td>MPU</td>
</tr>
<tr>
<td>Line Edge Roughness (nm)</td>
<td>4.5</td>
<td>2.7</td>
<td>1.8</td>
<td>1.3</td>
<td>0.9</td>
<td>0.65</td>
<td>MPU</td>
</tr>
<tr>
<td>Precision for LER</td>
<td>0.9</td>
<td>0.54</td>
<td>0.36</td>
<td>0.26</td>
<td>0.18</td>
<td>0.13</td>
<td></td>
</tr>
</tbody>
</table>

---

**Image:**
- **193 and 157 nm**
- **EUV**
- **Litho Metrology Diagram**
- **EUV System Components:**
  - Drive laser beam
  - C1 collector
  - Gas jet assembly
  - Laser-produced plasma
  - C2, C3 pupil optics
  - Spectral purity filter
  - Reticle stage
  - C4 element
  - Projection optics
  - Wafer stage
Low Energy SEM for CD Measurements

Thanks to David Joy

INTERNATIONAL SEMATECH
Limits of SEM for CD Measurements

Loss of Depth of Field

\[ \text{DoF} = \frac{\text{resolution}}{\text{(convergence angle)}} \]

Thanks to David Joy
Challenges: Round Top Resist & LER

Line Edge Roughness Requires Better Dimensional Precision

Issue facing 50 nm lines from 130 nm node in 2001
Comparison of conventional SE (left) and Low Loss (right) images of copper interconnects. Note the greatly enhanced surface detail and lack of edge brightness in the Low Loss image.

Micrograph courtesy of O C Wells

Figures from David Joy
3D CD Metrology

SEM – Scatterometry – CD-AFM

Commerially available

Software comparison of top down line scan of edge to golden image

Tilt Beam SEM

Scatterometry

CD-AFM

Dual Beam FIB (destructive)

Software to convert top down image to 3D image

R&D
Scatterometry for CD Measurements

- Incident Polarized White Light
- Multi-wavelength Light Source
- Mirror
- Polarization Sensitive Detector
- Real Time Calculation of line width & shape
- Eliminates Libraries

Graph showing line width and shape.
CD-AFM Limited by Probe Tip

Carbon Nanotube Probe tips
Average vs Individual

- CD-SEM measures one line at a time
- Scatterometry gives an average over many lines
- Reports indicate a large number (80 different lines) CD-SEM measurements in test area required to match scatterometry average
- Lose individual line information
# Hi-thruput CD Potential Solutions

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>MPU / ASIC ½ Pitch (nm)</td>
<td>150</td>
<td>130</td>
<td>90</td>
<td>65</td>
<td>45</td>
<td>32</td>
<td>22</td>
<td>MPU / ASIC</td>
</tr>
<tr>
<td>MPU Printed Gate Length (nm)</td>
<td>90</td>
<td>75</td>
<td>53</td>
<td>35</td>
<td>25</td>
<td>18</td>
<td>13</td>
<td>MPU Printed Gate</td>
</tr>
<tr>
<td>MPU Physical Gate Length (nm)</td>
<td>65</td>
<td>53</td>
<td>37</td>
<td>25</td>
<td>18</td>
<td>13</td>
<td>9</td>
<td>MPU Physical Gate</td>
</tr>
</tbody>
</table>

- **CD-SEM**
- **High Voltage CD-SEM**
- **Scatterometry**
- **CD-AFM**
- **Point Projection Microscope e - holography**

**R&D Required**

**Meets ITRS Precision w/o tool matching**
AGENDA

• How to control microscopic features
• Litho Metrology
• FEP Metrology
• Interconnect Metrology
• Materials Characterization
Front End Metrology

- Shallow Trench Isolation
- Pattern & Gate Dielectric
- Pattern Poly/metal Implant LDD
- Pattern & Implant S/D
- Pattern & Implant Wells
- Pattern Wells

Electrode Material
Dopant Activation Grain Structure
Sidewall Profile
Upper Interfacial Layer
Lower Interfacial Layer
High K Dielectric
Silicon Interface
Etch Rate Selectivity
Barrier Height Gate Leakage Interfaces Contamination $V_{fb}$
Metal Diffusion
SOURCE
DRAIN
FEP: High \( \kappa \) Metrology

<table>
<thead>
<tr>
<th>Technology Node</th>
<th>130 nm</th>
<th>90 nm</th>
<th>65 nm</th>
<th>45 nm</th>
<th>32 nm</th>
<th>22 nm</th>
<th>Driver</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Front End Processes Metrology</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>High Performance Logic EOT equivalent oxide thickness (EOT) nm</td>
<td>1.3-1.6</td>
<td>0.9-1.4</td>
<td>0.6-1.1</td>
<td>0.5–0.8</td>
<td>0.4–0.6</td>
<td>0.4–0.5</td>
<td>MPU</td>
</tr>
<tr>
<td>Logic Dielectric EOT Precision 3( \sigma ) (nm)</td>
<td>0.005</td>
<td>0.004</td>
<td>0.0024</td>
<td>0.0024</td>
<td>0.0016</td>
<td>0.0016</td>
<td>MPU</td>
</tr>
<tr>
<td>Metrology for Ultra-Shallow Junctions at Channel Xj (nm)</td>
<td>26</td>
<td>14.8</td>
<td>10</td>
<td>7.2</td>
<td>5.2</td>
<td>3.6</td>
<td>MPU</td>
</tr>
</tbody>
</table>

High \( \kappa \) near UV light absorption
Makes thin interfacial layer difficult to measure

“Out of the Furnace”
High \( D_{it} \)
\( = \) Error in EOT

Light source: (Xe, D\(_2\), lasers)

\[ E(\tau) \]

Polarization before sample

\[ E \]

Polarization after sample

\[ \text{Si} \]

\[ C (F/cm^2) \]

\[ V_g (V) \]

tox=3nm,Nsub=1e17,Npoly=1e20

SeMATech
Optical/X-ray vs Electrical Measurement

C-V Structures receive Further Processing
Optical thickness vs electrical EOT
Capacitance of a very thin interface can have big effect

\[
t_{\text{optical}} = t_{\text{int}} + t_{\text{high}} \kappa
\]

\[
EOT = t_{\text{int}} + (3.9/\kappa)t_{\text{high}} \kappa
\]

See also: C Richter in Char & Met for ULSI 2000
SPC requires measurement to Average Gate Dielectric over large area

Light source (Xe, D₂, lasers)

monochromator

polarizer

analyzer

Polarization after sample

2002 ALMC consensus method for TEM
New Optical Models for higher $\kappa$

In-Line Metrology Suppliers continue to use older damped oscillator models.
Simplified X-ray Path for X-ray reflectometer

X-ray source → slits → sample → speculally reflected beam → detector

Models can include interface layer

Phase shift = \( \frac{2d \sin \theta}{\lambda} \)

Intensity (counts s\(^{-1}\))

4 nm HfO\(_2\)

Thanks to Rich Matyi
NIST + ISMT: C-V Full Curve Fits for Tox=1nm

Tox=1nm, Dit=1e10, Full Curve Fit

Tox=1.19+/-.03
RMS Error = 3.0%

Dit = 1 e 10

Tox=0.78+/-.05
RMS Error = 10.8%

Metal Dot
oxide
silicon

Bias

Capacitance

Voltage

NIST 'Data'
CVC Fit

NIST 'Data'
CVC Fit
Extra reflection from SOI Wafers Impacts Optical Measurements and Light Scattering

Quantum confinement for sub 20 nm silicon
Need SOI Optical Constants
Beyond Classical CMOS

Bulk MOSFET

Ultra-Thin Body SOI

Partially-Depleted SOI

Double-Gate MOSFET
AGENDA

• How to control microscopic features
• Litho Metrology
• FEP Metrology
• Interconnect Metrology
• Materials Characterization
Interconnect Metrology

- Pattern Low $\kappa$
- Control Line width/depth and shape
- Deposit barrier and copper
- Control barrier/copper & voiding
- Chemical Mechanical Polishing
- Control Flatness

Low $k$ / barrier etch stop / low $k$
### Gaps in Interconnect Metrology

<table>
<thead>
<tr>
<th>Technology Node</th>
<th>130 nm</th>
<th>90 nm</th>
<th>65 nm</th>
<th>45 nm</th>
<th>32 nm</th>
<th>22 nm</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Interconnect Metrology</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Barrier layer thick (nm) process range ($\pm 3\sigma$)</td>
<td>13</td>
<td>10</td>
<td>7</td>
<td>5</td>
<td>4</td>
<td></td>
</tr>
<tr>
<td>Precision $1\sigma$ (nm)</td>
<td>0.04</td>
<td>0.03</td>
<td>0.02</td>
<td>0.016</td>
<td>0.013</td>
<td></td>
</tr>
<tr>
<td>Void Size for 1% Voiding in Cu Lines</td>
<td>87</td>
<td>52</td>
<td>37</td>
<td>26</td>
<td>18</td>
<td>12</td>
</tr>
<tr>
<td>Detection of Killer Pores at (nm) size</td>
<td>6.5</td>
<td>4.5</td>
<td>3.25</td>
<td>2.25</td>
<td>1.6</td>
<td>1.1</td>
</tr>
</tbody>
</table>

- VOID Detection in Copper lines
- Killer Pore Detection in Low $\kappa$
- Barrier / Seed Cu on sidewalls
- Control of each new Low $\kappa$
R-C test structures of new low $\kappa$
Prior to manufacture

Resistance Test

Capacitance Test
XRR for low $\kappa$ process control

Reflectivity

Scattering Angle $\theta$ /Deg.

<table>
<thead>
<tr>
<th>Porous Low-k</th>
<th>391.1 nm</th>
</tr>
</thead>
<tbody>
<tr>
<td>SiNC 15 nm (density 1.89g/cm$^3$)</td>
<td></td>
</tr>
<tr>
<td>SiNC 3 nm (density 1.70g/cm$^3$)</td>
<td></td>
</tr>
<tr>
<td>SiNC 15 nm (density 1.89g/cm$^3$)</td>
<td></td>
</tr>
<tr>
<td>SiNC 3 nm (density 1.70g/cm$^3$)</td>
<td></td>
</tr>
</tbody>
</table>

6 periods

18 nm

SiO$_2$ (density 2.14 g/cm$^3$)

550 nm

Si substrate

0.2 $\mu$m
Pore Size Distribution
Diffuse (small angle) x-ray scattering

Average pore diameter = 50 Å
AGENDA

• How to control microscopic features
• Litho Metrology
• FEP Metrology
• Interconnect Metrology
• Materials Characterization
Method Dependent Observation of Film Properties

Local information
HRTEM of SiO2 Thickness

Silicon Wafer on a Wafer Chuck
TEM Imaging of the Interface
TEM of thin gate dielectric

Simulation and Experimental Data show ADF-STEM and HR-TEM give same thickness

Consensus method uses 50 nm thick sample & ADF-STEM

Thanks to Dave Muller
Local Electrode Atom Probe

Atom Distribution: < 100% detection
# Metrology & New Structures

## Memory

<table>
<thead>
<tr>
<th>STORAGE MECHANISM</th>
<th>BASELINE 2002 TECHNOLOGIES</th>
<th>MAGNETIC RAM</th>
<th>PHASE CHANGE MEMORY</th>
<th>NANO FLOATING GATE MEMORY</th>
<th>SINGLE/FEW ELECTRON MEMORIES</th>
<th>MOLECULAR MEMORIES</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

- **DEVICE TYPES**
  - DRAM
  - NOR FLASH
  - PSEUDO-SPIN-VALVE
  - MAGNETIC TUNNEL JUNCTION
  - OUM
  - -ENGINEERED TUNNEL BARRIER
  - -NANOCRYSTAL
  - SET

## Logic

<table>
<thead>
<tr>
<th>DEVICE</th>
<th>RESONANT TUNNELING DIODE – FET</th>
<th>SINGLE ELECTRON TRANSISTOR</th>
<th>RAPID SINGLE QUANTUM FLUX LOGIC</th>
<th>QUANTUM CELLULAR AUTOMATA</th>
<th>NANOTUBE DEVICES</th>
<th>MOLECULAR DEVICES</th>
</tr>
</thead>
<tbody>
<tr>
<td>TYPES</td>
<td>3-terminal</td>
<td>3-terminal</td>
<td>Josephson Junction +inductance loop</td>
<td>-Electronic QCA -Magnetic QCA</td>
<td>FET</td>
<td>2-terminal and 3-terminal</td>
</tr>
</tbody>
</table>

- **TYPES**
  - 3-terminal
  - 3-terminal
  - Josephson Junction +inductance loop
  - -Electronic QCA -Magnetic QCA
  - FET
  - 2-terminal and 3-terminal
Metrology & Molecular Electronics

James Heath, Fraser Stoddart, and Anthony Pease
Nanowire Transistors and Interconnect

5 nm layer of Ge on top of 4 nm SiOx

10 nm p-Si core diameter & 10 nm i-Ge layer

L.J. LAUHON, M.S. GUDIKSEN, D. WANG & CHARLES M. LIEBER
Conclusions

• Measure Microscopic Features
  – New Methods
  – Look for a Signal that reflects Microscopic Change

• Improve Statistical Significance
  – Average over Large AREAS
  – Use Statistical Metrology When Possible

• Do these trends Conflict with smaller scribe line?
# Metrology Roadmap 2002 Update

**Europe**
- Ulrich Mantz (Infineon)
- Alec Reader (Philips Analytical)
- Mauro Vasconi (ST)

**Japan**
- Masahiko Ikeno (Mitsubishi)
- Fumio Mizuno (Meisei University)
- Toshihiko Osada (Fujitsu)
- Akira Okamoto (SONY)
- Yuichiro Yamazaki (Toshiba)

**Korea**
- DH Cho (Samsung)

**Taiwan**
- Henry Ma (EPISIL)

**US**
- Steve Knight (NIST)
- Alain Diebold (Int. SEMATECH)
# Metrology Roadmap 2002 Update

**US**
- John Allgair, Motorola
- Alain Diebold, Int. SEMATECH
- Drew Evan, CEA
- David Joy, Univ. of Tenn
- Steve Knight, NIST
- Kevin Monahan, KLA-Tencor
- Noel Poduje, ADE
- Heath Pois, Thermawave
- Bhanwar Singh, AMD
- Andras Vladar, NIST

**Speakers**
- Michael Gostein, Philips Analytical
- PY Hung, Int. SEMATECH
- Tom Kelly, Amigo
- Heath Pois, Thermawave
- Benzi Sender, Applied Materials

---

International Technology Roadmap for Semiconductors
New Methods

Objective lens

Detail in wafer

Junction

Beam

Excess carriers

Probe laser

Generation laser

Beam splitter

Detector

Vision system

Objective lens

Excess carriers

Junction

Beam

Detector
1 - Probe beam strikes surface

2 - Form grating and excite acoustic wave

3 - Probe beam diffracted as wave travels parallel to surface

Excitation Laser Pulse

Signal (mV)

Time (ns)

Cu 270 MHz

1 / Acoustic Frequency
Pulsed Laser (200 fsec; 90 MHz)  
800nm

Ti sapphire laser

Servo delay

Wavelength Selector

Frequency Doubler

Lens

photocell

sampling speed (2 to 4 secs/pt)
less than a 10 mm diameter spot size
X-Ray Tube

Thin-Film Sample

Monochromator

X-Ray Sensor

Spatially Resolving

Reflectivity

Angle

16Å ± 2Å rms

969Å ± 1Å Cu

250Å ± 1Å Ta

Silicon

Fit from SB-Code
Metrology & Molecular Electronics

1. $Z = \text{SCOCH}_3$

$\text{NH}_4\text{OH}$

$1', Z = \text{S}^-, 4,4'$-di(ethynylphenyl)-1-benzenethiolate

2. $Z = \text{SCOCH}_3$

$\text{NH}_4\text{OH}$

$2', Z = \text{S}^-, 4,4'$-di(ethynylphenyl)-2'-nitro-1-benzenethiolate

3. $Z = \text{SCOCH}_3$

$\text{NH}_4\text{OH}$

$3', Z = \text{S}^-, 2'$-amino-4,4'-di(ethynylphenyl)-5'-nitro-1-benzenethiolate
## Use of HRTEM for Calibration

High Resolution TEM (Phase Contrast) has a ~10% error for Thickness Determination Due to Cs.

<table>
<thead>
<tr>
<th>Specimen Thickness A</th>
<th>Specimen Tilt (mrad)</th>
<th>Defocus</th>
<th>Cs (mm)</th>
<th>Oxide Model Thickness</th>
<th>Oxide Measured Thickness</th>
<th>% Error</th>
</tr>
</thead>
<tbody>
<tr>
<td>154</td>
<td>0</td>
<td>-425</td>
<td>0.5</td>
<td>10.56</td>
<td>9.84</td>
<td>-6.8</td>
</tr>
<tr>
<td>154</td>
<td>0</td>
<td>-156</td>
<td>0.5</td>
<td>10.56</td>
<td>11.4</td>
<td>8</td>
</tr>
<tr>
<td>154</td>
<td>0</td>
<td>-20</td>
<td>0.5</td>
<td>10.56</td>
<td>10.44</td>
<td>-1.1</td>
</tr>
<tr>
<td>154</td>
<td>12.6</td>
<td>-425</td>
<td>0.5</td>
<td>10.56</td>
<td>9.12</td>
<td>-13.6</td>
</tr>
<tr>
<td>154</td>
<td>25</td>
<td>-425</td>
<td>0.5</td>
<td>10.56</td>
<td>10.68</td>
<td>1.1</td>
</tr>
<tr>
<td>154</td>
<td>0</td>
<td>-425</td>
<td>0.5</td>
<td>10.56</td>
<td>8.88</td>
<td>-15.9</td>
</tr>
</tbody>
</table>

HRTEM Image Simulations for Gate Oxide Metrology

S. Taylor, J. Mardinly, M.A. O’Keefe, and R. Gronsky

Characterization and Metrology for ULSI Technology 2000