Overview of Optical Metrology for Ultra-thin Oxide and High-K Gate Dielectrics

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OUTLINE:

1. Current Gate Dielectric Metrology Challenges

2. Implementation of Spectroscopic Ellipsometry to High K/ Ultrathin Oxide Stacked Gate Dielectric Metrology

3. Characterization of Gate Oxide on Silicon-On-Insulator substrates

4. Future Gate Stack Metrology Challenges
1. Current Gate Dielectric Metrology Challenges:

*High K* gate dielectric films exhibit sensitive dependence on material composition—need to control material composition

Also *High K* may be stacked on Ultra-thin Oxide interface to preserve channel mobility—need to control interfacial thickness in “EOT” measurement

Gate Oxide Metrology:

\[
\frac{1}{C_{\text{total}}} = \frac{1}{C_{\text{oxide}}} + \frac{1}{C_{pd}} + \frac{1}{C_{inv}}
\]

Relies on correlation of physical thickness of oxide and device electrical thickness

\[
C = \frac{\varepsilon \times A}{t} \quad \text{CET} = EOT + \text{offset}
\]

"y = mx + b"

\[
EOT = 3.92 \times T_{\text{oxide}}
\]

• Poly-depletion and inversion layer capacitance treated as fixed offset

Ellipsometry for Gate Dielectric Metrology:

- Ellipsometric thickness measurement provides acceptable precision for Gate Oxide
- However, high K stack is more complex...

Light source: (Xe, D₂, lasers)

\[
\rho = \frac{r_p}{r_s} = \tan(\Psi)e^{i\Delta}
\]

- Monochromator
- Polarizer
- Analyzer

Si substrate

Polarization before sample

E(t)

Polarization after sample
Ellipsometric approach for High K gate dielectric metrology:

“If ideal” high K ⇒ \[ EOT = \frac{\varepsilon_{\text{oxide}}}{\varepsilon_{\text{highK}}} \times T_{\text{highK}} \]

If dielectric constant of film is known, then only need high K film physical thickness— conclusion in this case is that ellipsometric approach will work

However, high k composition has proven notoriously difficult to control in practice ⇒ now must also track high K film material properties in ellipsometric approach

Need to limit number of fit parameters ⇒ improved precision
Need appropriate dispersion functional form (\(\varepsilon_2 \neq 0\)) ⇒ improved precision
Typical optical response of Hi-K films:

- Index tracks K value—normally will exhibit approximate linearity over process range.
ALCVD High K alloy dielectric functions: Optical Constants

- Tauc-Lorentz Optical models
Spectroscopic Ellipsometry of ALCVD High K alloys
Effective medium approach:

Medium 1
  e.g: Silicon Dioxide

Medium 2
  e.g: Silicon Nitride

Effective medium
  e.g. Oxynitride

Advantages
  • may combine known material dispersions
  • allows calibration to material composition
Nitrogen content determination in oxynitrides via spectroscopic ellipsometry:

Optical Constants

- Real(Dielectric Constant), $\varepsilon_1$

- Photon Energy (eV)

- Oxide
- 5% nitrogen
- 8% nitrogen
- 10% nitrogen
- 13% nitrogen
- 15% nitrogen
EMA with Tauc-Lorentz constituents for fitting High K process window:
High-K Gate Dielectric Metrology:

*Real High K has ultra-thin interfacial oxide ⇒*

**Potentially Requires:**
1. Hi-K film physical thickness
2. K value
3. Interfacial oxide thickness

**Reduced correlation to device performance**

**Will SE work for Ultra-thin Oxide layers below high K?**

- Ellipsometry: sensitive to “total” dielectric physical thickness, but limited sensitivity to interfacial thickness
Gate Dielectric Modeling Approach:

1. Gate Oxide - Single Wavelength Ellipsometry (laser based) for $T_{ox}$ ⇒ acceptable “EOT” precision

2. “Ideal” High K- Spectroscopic Ellipsometry (lamp based) for material content and $T_{hi-K}$, ⇒ precision too large by ~4x

3. High K/ Ultra-thin Oxide Stack - No Best Known Method established to date
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Hi-K/ Interfacial Oxide Stacked for SE Calibration:

A. High K silicates with Ultra-thin interface ~5Å: 2 high K compositions with & w/o Post Deposition Anneal— 4 wafers

B. High-K silicates with Rapid Thermal Oxide underlayer ~25 Å: 2 high K compositions with & w/o PDA— 4 wafers

C. High-K silicates with Rapid Thermal Oxide underlayer ~20 Å: 2 high K compositions with & w/o PDA— 4 wafers
HRTEM—Hi-K #2/ Oxide #1

2.7 – 3.3 nm high-k
2.3 nm SiO2

2.9 – 3.4 nm high-k
2.0 – 2.3 nm SiO2

Courtesy Brendan Foran, ISMT
HRTEM—Hi-K #1/ Oxide #2 with Post Deposition Anneal

3.2 – 3.6 nm high-k
2.3 nm SiO2

3.3 – 3.7 nm high-k
2.0 – 2.2 nm SiO2

Courtesy Brendan Foran, ISMT
Hi-K/ oxide stack VASE™ results:

- Rapid Thermal Oxide— independent of PDA
Hi-K/oxide stack VASE™ results:

MOCVD High K silicates w/ post deposition anneal

Optical Constants

Shift seen w/ PDA

Higher metal content

Lower metal content

Table:

<table>
<thead>
<tr>
<th>Photon Energy (eV)</th>
<th>$\varepsilon_1$</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>3.0</td>
</tr>
<tr>
<td>2</td>
<td>4.0</td>
</tr>
<tr>
<td>4</td>
<td>5.0</td>
</tr>
<tr>
<td>6</td>
<td>6.0</td>
</tr>
<tr>
<td>8</td>
<td>7.0</td>
</tr>
</tbody>
</table>
## Hi-K/ interfacial wafer calibration table:

<table>
<thead>
<tr>
<th>Filmstack/ process info</th>
<th>T oxide [Å]</th>
<th>T hi-K [Å]</th>
<th>Index hi-K</th>
<th>MSE</th>
</tr>
</thead>
<tbody>
<tr>
<td>Si/ interface/ hi-K #1</td>
<td>10.34</td>
<td>30.59</td>
<td>1.961</td>
<td>1.183</td>
</tr>
<tr>
<td>Si/ interface/ hi-K #1 (PDA)</td>
<td>12.43</td>
<td>24.26</td>
<td>2.097</td>
<td>0.8838</td>
</tr>
<tr>
<td>Si/ interface/ hi-K #2</td>
<td>5.84</td>
<td>25.67</td>
<td>1.841</td>
<td>0.9884</td>
</tr>
<tr>
<td>Si/ interface/ hi-K#2 (PDA)</td>
<td>6.68</td>
<td>26.61</td>
<td>1.933</td>
<td>1.59</td>
</tr>
<tr>
<td>Si/ oxide #1/ hi-K #1</td>
<td>24.94</td>
<td>24.97</td>
<td>1.961</td>
<td>0.6863</td>
</tr>
<tr>
<td>Si/ oxide #1/ hi-K #1 (PDA)</td>
<td>24.94</td>
<td>23.01</td>
<td>2.097</td>
<td>0.6827</td>
</tr>
<tr>
<td>Si/ oxide #2/ hi-K #1</td>
<td>26.02</td>
<td>23.86</td>
<td>1.961</td>
<td>0.6862</td>
</tr>
<tr>
<td>Si/ oxide #2/ hi-K #1 (PDA)</td>
<td>25.76</td>
<td>22.86</td>
<td>2.097</td>
<td>0.6806</td>
</tr>
<tr>
<td>Si/ oxide #1/ hi-K #2</td>
<td>21.84</td>
<td>24.25</td>
<td>1.841</td>
<td>0.6616</td>
</tr>
<tr>
<td>Si/ oxide #1/ hi-K #2 (PDA)</td>
<td>21.84</td>
<td>23.76</td>
<td>1.933</td>
<td>0.6595</td>
</tr>
<tr>
<td>Si/ oxide #2/ hi-K #2</td>
<td>22.8</td>
<td>25.72</td>
<td>1.841</td>
<td>0.6521</td>
</tr>
<tr>
<td>Si/ oxide #2/ hi-K #2 (PDA)</td>
<td>22.94</td>
<td>24.4</td>
<td>1.933</td>
<td>0.6563</td>
</tr>
</tbody>
</table>
High K/interfacial layer optical metrology summary…

Standard spectroscopic ellipsometric approach parameters strongly coupled—not quite enough precision for interfacial layer thickness or material content.

Approach also suffers from decreasing correlation with device characteristics—must account for process step induced changes present.

Need to develop interface specific techniques.
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Extra reflection from SOI Wafers Impacts Ellipsometric Measurements

Si Wafer

SOI Wafer

Gate Dielectric on Si Wafer

Gate Dielectric on SOI Wafer
Optical models for Gate Oxide on SOI:

Generated and Experimental

Extra reflection may impact Gate Oxide on SOI precision
Optical models for Gate Oxide on SOI:

MSE ~1.6 (~200Å top Si)
Gate Oxide on SOI substrate optical metrology summary…

Standard spectroscopic ellipsometric approach appears acceptable— excellent fitting seen, impact of extra-reflection needs evaluation

Future High K stack on strained SOI appears likely…

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4. Future Gate Dielectric Metrology Challenges:

SE at limits- to characterize:

1. High K gate dielectric on Si substrate
2. High K/ interfacial oxide stack on Si
3. Gate Oxide on SOI
4. Gate Oxide on SiGe
5. Gate Oxide on SiGe-on-Insulator
Ultra-thin Oxide on Graded SiGe substrate:
Extraction of Graded SiGe layer thickness—wVASE™ results:

<table>
<thead>
<tr>
<th>Layer Description</th>
<th>Thickness</th>
</tr>
</thead>
<tbody>
<tr>
<td>0 si substrate</td>
<td>1 mm</td>
</tr>
<tr>
<td>1 epi</td>
<td>3.0234 µm</td>
</tr>
<tr>
<td>2 epi #2</td>
<td>0.16599 µm</td>
</tr>
<tr>
<td>3 sige graded si_jaw/ge</td>
<td>1.8177 µm</td>
</tr>
<tr>
<td>4 sige x=0.920</td>
<td>2.6326 µm</td>
</tr>
<tr>
<td>5 epi cap</td>
<td>0.012328 µm</td>
</tr>
<tr>
<td>6 native oxide</td>
<td>0.00099613 µm</td>
</tr>
</tbody>
</table>

- Increase in number of required parameters
Timeline for Fully Depleted Ultra-thin body SOI–

- 115nm node (2002)  SOI ~16-27 nm  BOX ~40-66 nm
- 65nm node (2007)   SOI ~8-13 nm   BOX ~19-31 nm
- 45nm node (2010)   SOI ~5-9 nm    BOX ~14-23 nm
- 32nm node (2013)   SOI ~4-7 nm    BOX ~10-16 nm
- 22nm node (2016)   SOI: 3-5 nm    BOX ~7-11 nm

BOX may stay at ~100nm
Ultra-thin Si layer has altered optical response:

1. Critical Point SHIFT:

\[
E_{cp\ SOI} = E_{cp\ "bulk"} + \Delta E_{confinement}
\]

\[
\Delta E \cong \frac{\hbar^2 \pi^2}{2m^* L^2} = \frac{\hbar^2}{8m^* L^2} \cong \frac{(4.136 \times 10^{-15} \text{ eV} \cdot \text{s})^2}{8(m^*/m_e)(.511 \times 10^6 \text{ eV})L^2} \cdot \frac{(3 \times 10^8 m)^2}{s^2}
\]

\[m^* = 0.2m_e, \ L = 10 \text{ nm} \Rightarrow \Delta E \cong .02\text{eV}\ldots \text{(fairly small)}\]

However, if \( L = 5 \text{ nm} \Rightarrow \Delta E \cong .08\text{eV}\ldots \text{(becoming significant... shift scales as } 1/L^2)\]
Ultra-thin Si layer optical response (con’t):

2. Critical point SHAPE:

<table>
<thead>
<tr>
<th>DOS:</th>
<th>Direct:</th>
<th>Indirect:</th>
</tr>
</thead>
<tbody>
<tr>
<td>“bulk”</td>
<td>$\varepsilon_2 \propto \frac{(\hbar \omega - E_g)^{1/2}}{\omega^2}$</td>
<td>$\varepsilon_2 \propto \frac{(\hbar \omega - E_g)^2}{\omega^2}$</td>
</tr>
<tr>
<td>“well”</td>
<td>$\varepsilon_2 \propto \frac{\Theta(\hbar \omega - E_g)}{\omega^2}$</td>
<td>$\varepsilon_2 \propto \frac{(\hbar \omega - E_g)^{1}}{\omega^2}$</td>
</tr>
<tr>
<td>“wire”</td>
<td>$\varepsilon_2 \propto \frac{(\hbar \omega - E_g)^{-1/2}}{\omega^2}$</td>
<td>$\varepsilon_2 \propto \frac{\Theta(\hbar \omega - E_g)}{\omega^2}$</td>
</tr>
</tbody>
</table>

Describes $\Delta k_z = 0$
Absorption, e.g. Si CP at $\sim 3.3\text{eV}$

Describes $\Delta k_z \neq 0$
Absorption, e.g. Si indirect band edge at $\sim 1.1\text{eV}$
Schematic change in dielectric function of 5nm Si (no shape change):

Optical Constants

Imag(Dielectric Constant), $\varepsilon_2$

“bulk”

Photon Energy (eV)

SOI
Schematic difference in dielectric function of 50Å Si (vs. “bulk”):

Biggest differences occur at structural features (CP shape change critical)
Extraction of Ultrathin body SOI optical response:

\[ \varepsilon_2 \approx 1 = 2nk \]
\[ \alpha = \frac{4\pi k}{\lambda} \]
\[ \frac{I}{I_o} = \exp(-\alpha z) \]

\[ \Delta \langle \varepsilon_2 \rangle \approx 1, \ n \approx 6.9, \ \lambda \approx 3760 \ \text{Å}, \ z \approx 50 \ \text{Å} \]

\[ \frac{I}{I_o} \approx \exp \left\{ - \frac{4\pi \cdot 50}{2 \cdot 6.9 \cdot 3760} \right\} \approx 99\% \]

⇒ Need ~1% differential intensity resolution, with resolution in photon energy of <.01eV, on a strongly absorbing background...
Future Gate Dielectric Metrology:

- Future gate stack projected to be High-K on SiGe-on-Insulator
- For High K/oxide gate stack SE approach will need to be enhanced
- Optical Metrology for correlation to substrate characteristics may also be required
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... and many others