Recent Developments in Electrical Metrology for MOS Fabrication

Gate Engineering
Channel Engineering
Source-Drain Extension Engineering

George A. Brown
SEMATECH
Mark C. Benjamin
Solid State Measurements, Inc.
Gate Engineering

George A. Brown
SEMATECH
Introduction – Gate Dielectrics

- Brief Roadmap Review
- Traditional Gate Dielectric Electrical Metrology
  - Measurements, analysis, and limitations
- Improved Methods and Recent Developments
  - Critical C-V measurement parameters
    - High frequency
    - Low series resistance test structures
    - Adequate area resolution
  - UHFCAP structure
  - Multi-frequency C-V, $D_{\infty}$ characteristics
  - Interface State ($D_{it}$) Measurement: charge pumping
  - In-line C-V Measurements

- Summary
Beyond this point of cross over, oxynitride is incapable of meeting the limit (Jg,limit) on gate leakage current density.

- Scaling beyond 1 nm, $10^3$ A/cm² is almost upon us!
## Evolution of gate dielectric electrical metrology

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Traditional Measurement Technique</th>
<th>Traditional Analysis Technique</th>
<th>Shortcomings for Advanced Devices</th>
<th>Improved Measurement Technique</th>
<th>Improved Analysis Technique</th>
</tr>
</thead>
<tbody>
<tr>
<td>Oxide thickness, CET</td>
<td>100 kHz/1 MHz MOS C-V</td>
<td>Classical Poisson's Law Models</td>
<td>C-V distortion from high gate leakage</td>
<td>Low-Rs test structures, UHF C-V</td>
<td>Multi-element equivalent circuits</td>
</tr>
<tr>
<td>Oxide thickness, EOT</td>
<td>100 kHz/1 MHz MOS C-V</td>
<td>Classical Poisson's Law Models</td>
<td>Failure to account for quantum confinement, poly depletion</td>
<td>Schrodinger solvers for EOT</td>
<td></td>
</tr>
<tr>
<td>Interface State Density, Dit</td>
<td>Quasi-static C-V</td>
<td>Classical Poisson's Law Models</td>
<td>Gate leakage dominates quasi-static data</td>
<td>Charge pumping Brew's Dit</td>
<td></td>
</tr>
<tr>
<td>Oxide Charge Tgrapping</td>
<td>MOS C-V Hysteresis</td>
<td>$\Delta V_{fb}$</td>
<td>inaccurate, poorly defined for high-k</td>
<td>Pulsed transient Id-Vg</td>
<td></td>
</tr>
</tbody>
</table>

New methodologies must be developed to deal with the characteristics of radically scaled gate dielectric stacks.
High leakage gate stacks are modeled as parallel RC equivalent circuits.

To resolve the capacitance, use of higher frequencies will reduce the capacitive impedance, making that element dominate the parallel resistance/conductance.

But this only works if there is negligible parasitic series resistance in the test structure. Use of higher frequencies if series resistance is present only makes the capacitive impedance of interest negligible in comparison with $R_s$. 

\[ Q = \frac{\omega C_p}{G_p} \]
1. Capacitor test structure design with minimum series resistance.
   • Topside electrical contact to the capacitor substrate is required to eliminate the wafer chuck from the measurement circuit.

2. Use of measurement frequencies high enough to reduce the effect of the parallel conductance of the gate stack. *Dissipation factor must be reduced sufficiently to permit accurate measurements.*

3. Geometric resolution of the test structure effective area must be adequate to assure accurate and precise definition of EOT.
1-Port Philips UHF MOSCAP Design

- Designed for low series resistance
- Uses 3-point (G-S-G) UHF probe head
- 720 - 1.0x2.6 µm capacitor elements
- Right and left ground pads connect p-well to S/D.
Multi-Frequency MIS C-V Measurements on the Philips UHF MOSCAP

2 nm SiO₂ – TiN gate electrode

0.7 nm EOT HfO₂ – poly gate

Measurement: Agilent 4294A Precision Impedance Analyzer – IV Probe mode

- Frequency-invariant C-V data can be obtained in wafer form on 2 nm SiO₂ films with properly designed test structures.
- Some frequency dispersion is seen on more highly scaled high-k devices.

CVC Model Parameters
EOT = 7.35 Å
Nsurf = 9.7E17 /cc
Vfb = -0.252 V
RMS fit error = +/-0.8%

Effective Area = 8.7x10⁻⁶ cm²
Three-element Equivalent Circuit Parameter Analysis from Dissipation Factor-Frequency Characteristics

Dissipation Factor vs. Frequency Plot
Lot-wafer 3073102-07: STI HfSiO

EOT = 17.2 Å

Ro = 1.4E4 ohms
Rs = 18.4 ohms

D = \frac{1}{\omega R_o C_o}
D = \omega R_s C_o

For low frequencies, D \sim \frac{1}{f}:
D = \frac{G_o (1 + R_s G_o)}{\omega C_o} = \frac{1}{\omega R_o C_o} \left(1 + \frac{R_s}{R_o}\right) \approx \frac{1}{\omega R_o C_o}

In the high frequency limit, D \sim f:
D = \omega R_s C_o

Extraction of Ro, Rs from D-\omega Plots

\[ D = \frac{G_o (1 + R_s G_o)}{\omega C_o} \approx \frac{1}{\omega R_o C_o} \left(1 + \frac{R_s}{R_o}\right) \approx \frac{1}{\omega R_o C_o} \]

RoCo
RsCo

\[ D = \omega R_s C_o \]

\[ G_o = \frac{1}{R_o} \]

R_s

C_o

SEMATECH
Fixed Base, Variable Amplitude Charge Pumping (into accumulation)

- These techniques provide alternative ways to characterize traps and trapping processes in high-k films.
- Information on energy and depth distribution of the traps may be obtained from these curves.

Fixed Base, Variable Amplitude Charge Pumping (into inversion)

3.5 nm HfSiO / polySi

nFET W/L=10/1μm

V_{peak} = 1.2V

V_{base} = 1.0V

V_{base} = -1.0V

N_{it} [#/cycle*cm^2]

10^{12}

10^{11}

10^{10}

10^{9}

V_{base} [V] or V_{peak} [V]

1MHz Nit

100kHz Nit

10kHz Nit

Fixed Amplitude, Variable Base Charge Pumping
EM-probe Description

Small contact area provides superior performance for ultra-thin dielectrics

Stray capacitance compensated via software

Interface Layer associated with tip contact ~10 to 20 Å

AFM Indicates No Surface Damage

©2005 Solid State Measurements, Inc. ALL RIGHTS RESERVED
In-line Measurement of CET/EOT with EM-probe

- Device-correlatable CET/EOT measurements can be made in-line for real-time process control down to ~1 nm.
Relationship Between Dose and $N_{\text{SURF}}$

$N_{\text{SURF}} = \text{Average Dopant Density within } W_{\text{EQ}}$

Equilibrium Dose = $\text{EQD} = \int N(w)dw \text{ from the surface to } W_{\text{EQ}}$

$= N_{\text{SURF}}W_{\text{EQ}} = \sqrt{2\varepsilon k_s \psi_{\text{SL,INV}} N_{\text{SURF}} / q}$
EM-gate Equilibrium CV Comparison

SSM-6100 EM-probe CV versus Implant Dose

C (pF)

Vg (V)

Slot 1 1E11 cm-2
Slot 3 2E11 cm-2
Slot 5 5E11 cm-2
Slot 7 1E12 cm-2
Slot 9 1E13 cm-2
Slot 11 5E13 cm-2
Slot 13 8E13 cm-2
Slot 15 1E14 cm-2
SSM-6100 Nsurf Sensitivity Comparison

SSM®

Sensitivity: Nsurf versus Implant Dose

©2005 Solid State Measurements, Inc. ALL RIGHTS RESERVED
Major Device and Materials Issues with USJ S/D Structures

- Goal: Increase Electrically Active $N$ and Decrease $W$

- Ideal ► BOX Profile!!

- Sheet Resistance ($R_S$)

- Surface Carrier Density ($N_{SURF}$)

- Junction Depth ($X_J$)

- Carrier Density Profile Shape

- Junction Leakage
  - Sensitive to Implant EOR Damage
**4pp: Conventional vs EM-Probe**

**Conventional Four Point Probe**

- Sheet Resistance: $R_S = CF(V/I)$

**EM-probe Four Point Probe**

- Sheet Resistance: $R_S = CF(V/I)$
EM-probe Description

Stray capacitance compensated via software

~~Tip Shaft~~

Interface Layer associated with tip contact ~10 to 20 Å

Small contact area provides superior performance for ultra-thin dielectrics

© 2005 Solid State Microtechnologies

AFM Indicates No Surface Damage
EM-Probe CV and IV is used extensively to measure dielectrics with thicknesses less than 1 nm.
Basic Principle of Four Point Probe (4pp) Method for \( R_S \)

**Voltmeter:** Requires High \( Z_{in} \), low Input Offset Current

\[
\rho = \left[ q \mu p \right]^{-1} = \frac{R_{Area}}{l}
\]

Resistance = \( \frac{V_M}{I_A} \)

Sheet Resistance = \( \frac{\rho}{t} = CF \left( \frac{V_M}{I_A} \right) = \left[ q \mu \int N(x)dx \right]^{-1} \)

For Probes located far from Edge of Circular Sample, \( CF = 4.532 \)

**Irvin’s Curves**

\( R_S = \frac{V/I}{L/W} \), Units \( \Omega/\text{Square} \)

To eliminate Contact Resistance, *Kelvin* or Transmission Line (TLM) Structures are Used
Conventional versus EM-Probe 4pp $R_S$ Case 1: P+ USJ Structures

Graph showing the comparison of $R_S$ values for Conventional 4pp and EM-gate 4pp for different cases. The graph includes a bar chart and a ratio plot for $R_S$ vs $x_j$. The cases are labeled #1-1, #1-2, #1-6, and #1-4, with 16 nm and 28 nm features. The y-axis represents $R_S$ in Ohms/square, and the x-axis represents $x_j$ in Angstroms. The graph also includes a legend for the methods used.

©2005 Solid State Measurements, Inc. ALL RIGHTS RESERVED
RS – \( N_{\text{SURF}} \) Correlation: General Considerations

- Correlation Depends on Activation and \( x_j \)

**Good Rs – Nsurf Correlation**
- Nsurf Increasing;
- Higher Activation

**Poor Rs – Nsurf Correlation**
- Nsurf ~ Constant
- \( x_j \) increasing

\[ W \quad N \]

\[ x_j \sim \text{Constant, Diffusionless} \]

\[ W \quad N \]

\[ x_j \sim \text{Constant} \]
Summary

- Gate Engineering requires new measurement and analysis techniques
- Channel engineering requires new measurement techniques for in-line metrology
  - Equilibrium Nsurf extends usefulness
- Source-Drain Extensions (USJ) require new measurement techniques
  - Junction leakage requires thought -> Nsurf ?