Non-destructive USJ characterization using Carrier Illumination™ measurements

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Outline

Description of measurement
- Motivation
- Method

Results on full NMOS and PMOS process flows
- NMOS on blanket and patterned wafers
- PMOS dose matrix
- Extension to PAI implant amorphous layer depth measurement

Gage capability (reproducibility, stability, system matching)
Acknowledgements

The Doping Group at International Sematech, under the direction of Dr. Larry Larson, including Dr. Billy Covington, Dr. David Sing, Clarence Ferguson, Dr. Bob Murto and Billy Nguyen

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Dr. Wilfried Vander Voorst, IMEC

The Development and Applications Groups at Boxer Cross Inc
Source/Drain layers test limits of doping technology

USJ processes will be limited to a very narrow process window for depth, active dose, and uniformity

Source: ITRS’99
**Metrology gap for activated shallow junctions**

<table>
<thead>
<tr>
<th>Measures:</th>
<th>Dose</th>
<th>Profile</th>
<th>Depth, dose</th>
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<tbody>
<tr>
<td>Need</td>
<td>All nodes</td>
<td>&lt;250 nm</td>
<td>&lt;180 nm</td>
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<tr>
<td>Where used:</td>
<td>In-fab</td>
<td>Analysis lab</td>
<td>In fab</td>
</tr>
</tbody>
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- **4-point probe**
- **SRP**
- **SIMS**
- **Carrier Illumination**

*Carrier Illumination (CI) measurement shortens control loop to tighten process control*
Characterize Source/Drain processes in the fab

- 2 µm spot size, nondestructive measurement for use on product
- Short measurement time allows high throughput, uniformity mapping

Aim: In-line characterization and control of USJ processes
Carrier Illumination™ method - adding contrast to see the invisible

Optically generated carriers make transparent junction visible

Quasi-static measurement obtains high signal-to-noise ratio
Simulation shows excess carriers build-up at junction

Steep rise in excess carrier concentration at junction edge.
Reflection signal comes mainly from this region, where gradient is largest.
Red laser induces excess carriers

IR laser is used to measure wafer reflectance

DC carrier distribution deduced from reflectance signal

Patents issued and pending
Measurement matches theory: As implants

Following theory, data fits cosine using 980 nm laser wavelength

1e16/cm² 25 keV As
Annealed 950 to 1100 C
Source: Sematech.
Measurement matches theory: B doped CVD Si layers

CVD layers form well defined, box-like junctions of known depth. Signal follows cosine fit predicted by theory to <20 nm.

Source: IMEC, Sematech and Boxer Cross
Characterization experiments

- As Source/Drain optimization, energy matrix
- As LDD optimization, retained dose matrix (180 nm NMOS)
- As Source/Drain DOE: energy, dose, anneal time, temp (patterns)
- B LDD optimization, implanted dose matrix
- Ge and Si PAI layers
- Gage study
As S/D implants vs. energy with and without p-well

Depth trends as expected with energy, correlates to SIMS
DOE trends correlate to probing of test structures
P-well appears to have minimal effect
Found four mis-implanted wafers
- High Cl signal indicates bad implant, not missed RTA
- Confirmed with re-anneal + 4-point probe and SIMS
Junction depth trends with SIMS

BX-10 Xj vs. SIMS @ 1e18 cm-3

- BX-10 Xj (A)
- SIMS Xj (A)

S/D anneal
△ final anneal

Source: Sematech

CI measurement trends with SIMS over full range of energies
As LDD: Correlation to drive current (0.18 µm NMOS)

NMOS extension depth measured in SIMS test structures after RTA

Source: AMD
NMOS Design of Experiment (DOE) matrix

S/D DOE evaluates Cl measurement sensitivity to implant energy, dose, anneal time and temperature

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<tr>
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<th>center</th>
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<tbody>
<tr>
<td>Dose (/cm^2)</td>
<td>3.60E+15</td>
<td>3.00E+15</td>
<td>2.40E+15</td>
</tr>
<tr>
<td>Energy (keV)</td>
<td>47</td>
<td>42</td>
<td>37</td>
</tr>
<tr>
<td>Temperature (C)</td>
<td>1025</td>
<td>1000</td>
<td>975</td>
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<tr>
<td>Time (sec)</td>
<td>10</td>
<td>6</td>
<td>2</td>
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</table>
NMOS patterned wafer DOE result: correlation to energy

Source: Sematech
**B\textsuperscript{11} LDD implants vs. dose**

Depth trends with dose
Correlation to SRP, SIMS, 4PP
Noise limited resolution better than 2Å
N-well has minimal effect

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Std process thru PLDD → Implant: B, 800 eV, 4.5 - 6.5e14/cm\textsuperscript{2} → P+ RTA: 1000\textdegree C, 10s, \textsubscript{N\textsubscript{2}} → CI → S/D RTA: 1000\textdegree C, 10s, \textsubscript{N\textsubscript{2}} → CI
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Post-anneal signal correlates to LDD dose

After LDD anneal:
Resolution of $5 \times 10^{12}/\text{cm}^2$
($1\sigma$ noise = 5 $\mu$V)

After LDD and S/D anneal:
Resolution of $6 \times 10^{12}/\text{cm}^2$
($1\sigma$ noise = 5 $\mu$V)

Source: Sematech
SIMS, SRP confirm top-to-bottom Xj trend

Rs - Xj correlation

Source: Sematech
CI correlation to SRP measurements

Offset due to use of p/p algorithm
The three outlier SRPs trend opposite process ($x_j$ drops with increasing dose)

800 eV B$^{11}$ into n-well
dose range $4e14$ to $6.5e14$/cm$^2$

Source: Sematech
Pre-amorphization implant (PAI) depth measurement

Carrier Illumination Signal (uV)

Si: 7-15 keV
1E14-2E15

Ge: 15-30 keV
2E14-1E15

Source: AMD

Amorphization depth measured with TEM
Good reproducibility and stability

- Wafer mean junction depth variation ($1\sigma$) for 9 sites, 30 runs, including load/unload:
  - 24 June: 0.63%
  - 28 June: 0.83%

- Graph shows measurements taken on reference sample over the four months following installation
Matching of field systems

Measurements at 5 sites on same wafer, taken on field systems S1 and S3
Conclusions

CI measurement characterizes critical sub-180 nm S/D processes (S/D, Extension, PAI)

- Provides non-destructive high resolution measurement on product
- Provides fast turn-around, suitable for in-line use or uniformity measurement
- Gage capability sufficient for in-line SPC

CI method enables tighter control required for current and future Source/Drain processes.

Acknowledgement: International Sematech, AMD, IMEC