

Stress-Induced Effects Caused by 3D IC TSV Packaging on Advanced Semiconductor Processes

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ABSTRACT

Mechanical stress management is a challenge for leading edge semiconductor technology, both in terms of achieving the desired device performance through strain engineering, and in terms of managing chip-package interactions. Starting from the 45 nm CMOS technology node, the mechanical stress has comparable impact on layout-driven variability of intra-channel charge carrier mobility and threshold voltage as the lithography-caused effects. The process steps employed by 3D IC technology such as wafer/die thinning, through silicon via (TSV) etching and filling, wafer bumping, high-temperature solder reflow, and chip stacking, etc. act as additional stress sources that can affect the chip-stack performance. It is a very challenging task to get an entire picture of the modification of the stress distribution across device layers caused by this technology. Hence, it is important to have a capability to assess the stress generated during 3D IC stacking accurately. Clearly, any such methodology has to be based on multi-scale simulation. This paper describes a recently developed physics-based stress simulation flow that includes an interface to layout formats (GDS, OASIS, etc) and can be linked with finite-element analysis-based package-scale models. A set of physics-based compact models for a multi-scale simulation to assess the mechanical stress and the consequent effects on device performance across the device layers in silicon chips stacked and packaged with the 3D TSV technology is proposed (Fig. 1). Analogously to multi-scale simulation, a multi-scale materials characterization is critical as an input for the predictive simulation of stress distribution across the device layout. A calibration technique based on fitting to measured stress components and electrical characteristics of the test-chip devices is presented.

Keywords: 3D IC, TSV, stress, simulation.

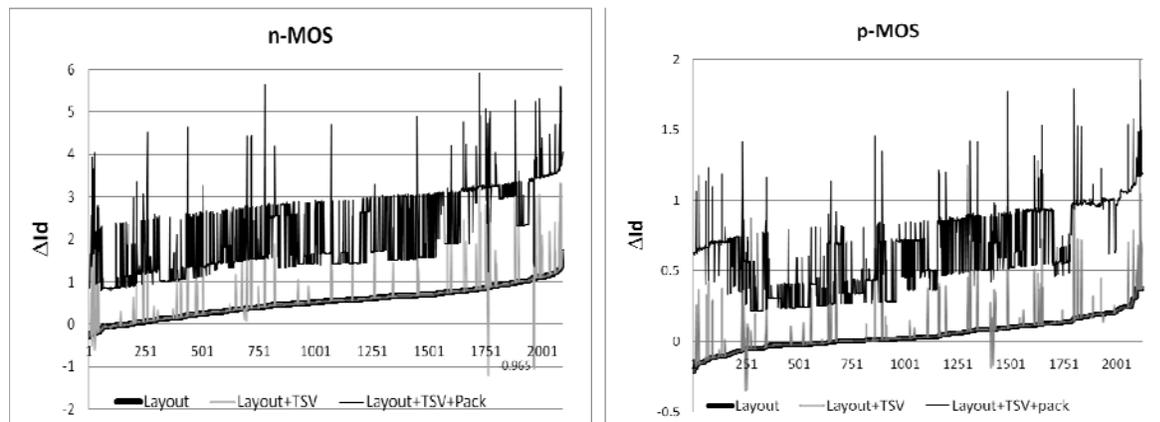


FIGURE 1. Sorted distributions of I_{dlin} for NMOS (a) and PMOS (b) when layout-induced stress sources were accounted (thick black lines); TSV-induced stress was added (light grey lines); TSV and package-induced stresses were added (thin black lines).