Strain Analysis in Scaled Si Transistors by Simulation-Hybrid UV Raman Microscopy

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ABSTRACT

Recent aggressive scaling of transistors imposes severe demand on material characterization. Material properties must be measured with high spatial resolution in complicated device structures composed of multiple materials. A typical example is mechanical strain in the channel region. It is preferable to measure the local strain quantitatively in a nondestructive manner after completion of transistor structure. To meet this demand, we are developing a hybrid technique of simulation and polarized UV Raman measurements. [1]

In this technique, the strain distribution in a transistor is estimated by a simulator, for which the Raman measurement plays two essential roles, calibration and verification. Strain simulation needs mechanical properties of constituent materials such as elastic constants and internal stress but these values are usually difficult to measure. Thus, these parameter values in strain simulation are calibrated by comparing the calculated Raman shift mapping with actual measurement results in a μm-scale transistor structure. The polarization dependence of Raman spectra enables detailed quantitative comparison.[2,3] Finally, the simulated strain distribution in actual scaled transistor is verified by the polarized Raman measurement. The fact that the light polarized normal to the gate side wall can penetrate through the side wall spacer enables this comparison.[4] Figure 1 shows that after the calibration the simulation reproduces the measured dependence of Raman shift on S/D width for pMOSFETs of 45-nm gate length.

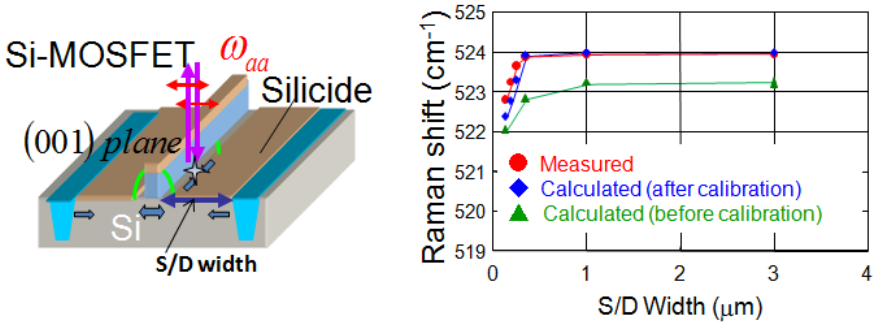

FIGURE 1. Simulation-hybrid Raman measurement of mechanical strain in p-MOSFET with 45-nm gate length. Dependence of Raman shift on S/D width is calculated and compared with actual measurements for vertical illumination/observation conditions. It is verified that the compressive strain due to stress liner decreases when the S/D width is reduced.

REFERENCES

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