

# Carbon Based Nanoelectronics

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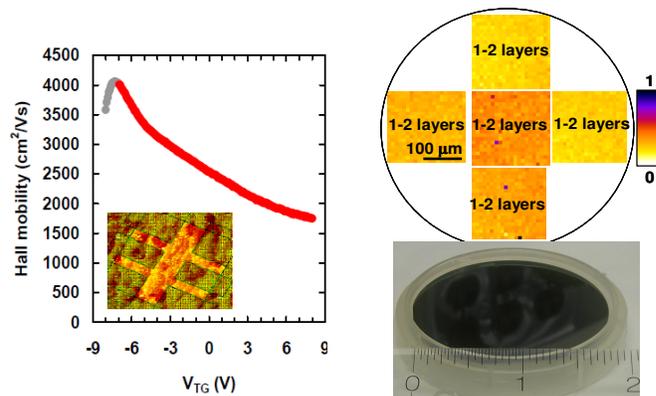
## ABSTRACT

Carbon nanoelectronics are strong candidates in replacing or supplementing Si technology. Theoretical and experimental studies have shown that carbon based transistors perform well at nanoscale device dimensions. Significant progress has been made for graphene radio-frequency (RF) applications where high on/off ratio is not necessarily required. IBM graphene FETs (GFET) yield the highest cut-off frequency ( $f_T$ ) values reported: >200 GHz on epitaxially grown SiC wafer and >150 GHz on CVD-grown-transferred onto Si wafer, which are well above ITRS Si MOSFET  $f_T$ - $L_g$  trend. Device simulations show that transconductance can be greatly improved by further reducing the contact resistance and structure optimization.  $f_T$  as high as 350 GHz is expected for 90-nm self-aligned gate GFET. A novel reconfigurable graphene p-n junction based logic device will be introduced. Its switching is accomplished by using co-planar split gates that modulate the properties that are unique to graphene including angular dependent carrier reflection which can dynamically change the device operation, leading to reconfigurable multi-functional logic. Epitaxy is to produce wafer-scale, high-quality graphene. A decomposition-based technique is implemented with in-situ monolayer control using a UHV growth chamber, equipped with low-energy electron diffraction microscopy (LEEM), which is capable of monolayer thickness precision and provides real-time electron reflection images from the graphene surface, allowing graphene formation via Si desorption from the SiC surface to be studied, optimized and controlled. 1-2 layers of graphene uniformly grown across Si-face SiC wafers with only monolayer variation exhibits high Hall mobility  $>4000 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$ . It is an important advance in large scale graphene epitaxy. Chemical vapor deposition (CVD) is another promising way to produce large-scale graphene which hold great commercialization potential at low cost. IBM demonstrated large dimension, single layer high quality graphene sheets CVD grown on Cu foil and later transferred to any desired substrate (Si wafer).

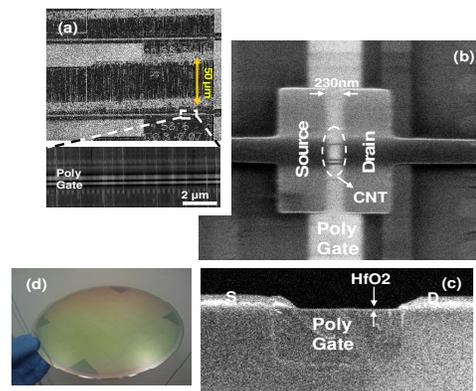
IBM also demonstrated a wafer-scale fabrication of high performance CNFETs using an 8" Si-CMOS line. A novel embedded poly-Si gate structure is employed to provide excellent electrostatics, CMOS process compatibilities and threshold tuning ability through gate doping. The nanotube transistors maintain their performance as their channel length is scaled from 3  $\mu\text{m}$  to 15 nm, with an absence of short channel effects. The 15-nm device has the shortest channel length and highest room-temperature conductance and transconductance of any nanotube transistor reported. Finally, we demonstrate the performance of a nanotube transistor with channel and contact lengths of 20 nm, an on-current of 10 mA, an on/off current ratio > 13000, and peak transconductance of 20 mS. These results provide an experimental forecast for carbon nanotube device performance at dimensions suitable for future transistor technology nodes through the next decade of the technology roadmap.

## REFERENCES

1.Dimitrakopoulos et al , Journal of Vacuum Science & Technology B, Vol.28, Issue 5, 7 Sep 2010. 2. 2010 IEDM Proceeding. 2.Han et al.: 2010 IEDM conference.



**Fig. 1.** Hall mobility and atomically smooth graphene of 1-2 layers with monolayer variation is uniformly grown on 2" SiC.



**Fig. 2** (a) Transferred aligned CNTs on the wafer with embedded poly gates. (b) Top, (c) cross-sectional view. (d) Fully-processed 8" wafer with CNFETs.