Current and Future Critical Dimension Metrology Perspective for Sub-10nm Process

Mar/23/2017
Mari Nozoe
Business Strategy Planning Division
Electronic Device Systems Business Group
## Technology Trend of Advanced Devices

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</thead>
<tbody>
<tr>
<td>Technology Node (nm)</td>
<td>Logic: N28</td>
<td>N22</td>
<td>N14</td>
<td>N10</td>
<td>N7</td>
<td>N5</td>
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<tr>
<td></td>
<td>HVM</td>
<td>DRAM/NAND: 25/20</td>
<td>20/16</td>
<td>18/14</td>
<td>16/14</td>
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<tr>
<td>Litho/ Patterning</td>
<td>ArF</td>
<td>SE</td>
<td>DP(SADP, LE^2)</td>
<td>MP(SAQP, LE^3)</td>
<td>EUV</td>
<td>SE</td>
<td>DP(SADP, LE^2)</td>
<td></td>
</tr>
<tr>
<td>Logic Device (MOS)</td>
<td>Planer</td>
<td>Si FinFET</td>
<td></td>
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<tr>
<td>Non-volatile Cash memory</td>
<td>3D(FinFET)</td>
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<tr>
<td></td>
<td>eMRAM</td>
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<tr>
<td>Main Memory</td>
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<tr>
<td>Storage-class Memory</td>
<td>DRAM</td>
<td></td>
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<td></td>
</tr>
<tr>
<td>Non-volatile memory</td>
<td>2D NAND</td>
<td>3D NAND</td>
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</tr>
</tbody>
</table>

- **2010**:
  - Logic: N28
  - HVM: DRAM/NAND: 25/20

- **2012**:
  - Logic: N22
  - Litho/Patterning: ArF

- **2014**:
  - Logic: N14
  - Litho/Patterning: SE

- **2016**:
  - Logic: N10
  - Litho/Patterning: DP(SADP, LE^2)

- **2018**:
  - Logic: N7
  - Litho/Patterning: MP(SAQP, LE^3)

- **2020**:
  - Logic: N5
  - Litho/Patterning: EUV

- **2022**:
  - Logic: N22

- **2024**:
  - Logic: N14

### Key Technologies
- **3D NAND**: 48L, 64L, 96L, 128L, >160L
- **MRAM**: N40, N28, N22, N14
- **XP-RAM**: 2L, 4L, >4L
- **2D NAND**
Evolution in Structure, Process and Material

FinFET

Multi-Patterning

DRAM

3D-NAND

Nano-wire, GAA

High-Mobility NW

MRAM

Si NW

GAA

Sacrificial layer

III-V NW

STI

Si

Stack

MgO
(tunnel layer)

SiN
(Encapsulation layer)

W

SiO2
Evolution in Structure, Process and Material

**FinFET**
- Pattern Fidelity Analysis
- Massive Measurement

**Multi-Patterning**
- LER, LWR
- PSD analysis

**DRAM**
- Overlay (in die, layer to layer)
- Precision < 0.1nm

**3D-NAND**
- HAR feature
  - Bottom, profile measurement

---

- **CD Metrology → EPE Metrology**
- **PSD: Power Spectrum Density**
# CD Metrology Overview

<table>
<thead>
<tr>
<th>Metrology method</th>
<th>Pros</th>
<th>Cons</th>
</tr>
</thead>
<tbody>
<tr>
<td>CD-SEM (image-based)</td>
<td>- Measure <strong>any complex arbitrary feature</strong></td>
<td>- Mid throughput for large area coverage</td>
</tr>
<tr>
<td>(In-line use)</td>
<td>- <strong>Direct</strong> measurement from image (no modeling)</td>
<td>- Difficult to measure pattern height</td>
</tr>
<tr>
<td></td>
<td>- <strong>Automated, stable, precise</strong></td>
<td></td>
</tr>
<tr>
<td>Optical Scatterometry</td>
<td>- High <strong>throughput</strong> (for global monitoring)</td>
<td>- Average measurement only (unavailable for complex pattern)</td>
</tr>
<tr>
<td>(OCD) (model-based)</td>
<td>- High <strong>sensitivity</strong>, <strong>CD/3D profile measurement</strong></td>
<td>- Long time for modeling (recipe setup) (reference needs)</td>
</tr>
<tr>
<td>(in-line use)</td>
<td>- <strong>Automated, stable, precise</strong></td>
<td></td>
</tr>
<tr>
<td>CD-AFM (image-based)</td>
<td>- Measure <strong>3D profile of arbitrary feature</strong></td>
<td>- Measurable pattern is limited</td>
</tr>
<tr>
<td>(image-based)</td>
<td></td>
<td>- <strong>Low throughput</strong></td>
</tr>
<tr>
<td>X-ray Scatterometry (CD-SAXS) (model-based) (off-line)</td>
<td>- <strong>CD/2D X-section profile measurement</strong></td>
<td>- Need large test pad</td>
</tr>
<tr>
<td></td>
<td></td>
<td>- Average measurement only (unavailable for complex pattern)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>- <strong>Low throughput</strong></td>
</tr>
<tr>
<td>Cross section TEM/STEM</td>
<td>- Atomic <strong>resolution</strong>, <strong>CD/3D profile measurement</strong></td>
<td>- <strong>Destructive</strong></td>
</tr>
<tr>
<td>(image-based) (off-line)</td>
<td></td>
<td>- <strong>Low throughput</strong></td>
</tr>
</tbody>
</table>
Edge Placement Error

\[ \sigma^2_{EPE} = \sigma^2_{CD} + \sigma^2_{OVL} + \sigma^2_{LCDU} \]

CD, Space, Pitch

OVL

LCDU, Pattern Fidelity

Global (average)

Local

1st litho
1st side wall
2nd side wall

L1 L2 L3 L4

d1 d2 d3
d4 d5 d6
d7
e1 e2 e3 e4 e5 e6 e7 e8

MNC 2016, Y. Momonoi, H. Fukuda
Pattern Fidelity Analysis

Measurement of Every Pattern in FOV

Extract contour from SEM image ➔ Design matching ➔ Edge Place Analysis

Measurement Value

Size (X, Y) ➔ Push out/Pull back ➔ Max CD/Min CD ➔ Protrusion/Necking ➔ Tip-to-tip/Side-to-side

2016 March, Hitachi Review Vol 65
**Pattern Fidelity Analysis**

**Logic/ SRAM Metal-1**
(Target Design)

**Patterns after Final Etching**
(Pattern Contour)

### Evaluation Point
(Align image to design data)

- **Design data**
- **Fidelity Quantification Result**
  (Volume of Line-end Pull-back)

### Risk for Missing Connection

**Line-end Pull-back:**

### Risk for Leak-current

**Line-end Push-out:**

**Pattern Fidelity Analysis**
EPE Analysis of Metal 1 Block

Especially important for multi-patterning (spacers and block)

P32 spacers on TiN
Block litho on SoC
SoC etch
TiN etch
Low-k etch

L1 L2 L3 L4

2016.Nov, Greg McIntyre
Patterning and Lithography update
Pitch walking measurement require to identify each line and space.
Overlay Metrology
Overlay Requirement

In-die device feature, control <1nm, layer-to-layer

Photo resist patterning
- Optical overlay measurement
- SEM based Overlay measurement

Etching
- Optical overlay measurement
- SEM based Overlay measurement

Prove Test + Root Cause Analysis

Overlay Requirement

Multiple Patterning
- Logic "node name"
- Flash hp
- DRAM hp
- Overlay Uncertainty

2015 ITRS Roadmap

Year

2015 2017 2019 2021 2023

Logic node/DRAM, Flash hp [nm]

Overlay Uncertainty [nm]

0 0.5 1 1.5 2 2.5 3

0 5 10 15 20 25 30

2015 2017 2019 2021 2023

EUV+MP

SPIE 2017, Kazuhisa Hasumi
SEM based overlay measurement between Via patterns and buried M1 patterns using high voltage SEM
High-precision, layer-to-layer overlay

1) Actual device pattern, layer-to-layer overlay is available
2) Under layer (um order depth) becomes visible
3) SEM_OVL results at ADI show good correlation to OPT_OVL

With high voltage SEM (HV_SEM),

**Optical Overlay Result**

<table>
<thead>
<tr>
<th>Yield Star at ADI</th>
<th>SEM_OVL at ADI</th>
</tr>
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</tbody>
</table>

SPIE 2017, Kazuhisa Masumi
SEM based overlay measurement between Via patterns and buried M1 patterns using high voltage SEM
LER / LWR Metrology
LER/ LWR and PSD analysis

PSD analysis: effective tool to reveal patterning process problems

- Various source in roughness, each having different spatial period range, need different index
  - side-wall film thickness (white)
  - resist stochastic (1/f)
  - wiggling in etching (long period)

Precision in CD measurement

\[ \sigma_{CD}^2 = \frac{\sigma^2_{\text{meas}}}{N} + \frac{\sigma^2_{\text{real}}}{N} \]

LER measurement

observed \( LER^2 \) = \( LER^2_{\text{real}} + \sigma^2_{\text{measurement}} \)

\[ N \sim 10^3 \sim 4 \]

\[ \text{SADP LWR} \]

\[ \text{SADP LER} \]
HAR Pattern Measurement

FinFET  Multi-Patterning  DRAM  3D-NAND
**Bottom CD Measurement of HAR pattern**

- **Low voltage, with energy filtering**
  - Si hard-mask
  - Si-sub
  - SEM images
  - \( \Delta V = V_R - V_{EF} \)
  - \( \Delta V \) in [V]: -20, 0, 6, 12

- **High voltage, detect BSE signal**
  - High Voltage 15-30kV
  - BSE
  - SE
  - In the SE image, the shape of the surface is clearly visible, but the bottom is not visible.
  - BSE is increased by a high-acceleration electron beam, and the contour of the bottom becomes clearer. (The slope is also visible)

SPIE 2017, Daisuke Bizen
High-precision CD measurement using energy-filtering SEM techniques
Another approach: FIB + SEM/STEM

K Takamasu, Y Iwaki; Satoru Takahashi; Hiroki Kawada; M Ikota; G F Lorusso; N Horiguchi “3D-profile measurement of advanced semiconductor features by reference metrology” SPIE 2016
Bottom CD Measurement of HAR pattern

New approach: Oblique FIB + Top-down CD-SEM

- Tilted FIB on 3D-NAND hole array
- Schematic cross section
- Cut planes at various depth levels
- Raw results
- AFM for height calibration

CD-SEM and FIB enable full 3D reconstruction

SPIE 2017, Gian Lorusso
Enabling CD SEM Metrology for 5nm Technology Node and Beyond
Metrology for Next Generation Device

Nano-wire, GAA

High-Mobility NW

MRAM

Si NW

GAA

Sacrificial layer

III-V NW

STI

Si

Stack

MgO (tunnel layer)

SiN (Encapsulation layer)

SiO2

CoFeB

CoFeB

CoPt

Ru

W

TaN

Ru

Ta
Nanowire metrology

CD measurement of Si and III–V lateral nanowires is feasible

Consistent CD trend between NWs and Si/SiGe fins.

BSE images enabled robust edge detection.

SPIE 2017, Gian Lorusso
Enabling CD SEM Metrology for 5nm Technology Node and Beyond
Emerging Memory metrology

Studying STT-MRAM CD measurement

High / low resistance difference is used as a memory bit “0/1”.

Typical configuration

Access time

Energy consuming

Access-time gap

Change in memory device hierarchy

SPIE 2017, Takeyoshi Ohashi
Variability study with CD-SEM metrology for STTMRAM

STT-MRAM memory cell

*MTJ : Magnetic Tunnel Junction
Emerging Memory metrology

Metrology for size-independent resistance variability qualification

SPIE 2017, Takeyoshi Ohashi
Variability study with CD-SEM metrology for STTMRAM

MgO

Electrically effective area

Physical area

Measured area

Damage width

Δ CD/2

Etching bias

16-19 nm

SiN thickness

4-9 nm

Encapsulation

SiN

Constant CD offset: D (fitting parameter)

Effective area: \( A_e \)

Measured area: \( A_m \)

Measured perimeter: \( C \)

Subtracted area: \( D(C - \pi D) \)

\[ A_e = A_m - D(C - \pi D) \]

Conductance

Under-estimated

Best fit

Over-estimated

Estimated effective area

Effective area
Metrology for HVM
Requirement for HVM metrology tool

1nm resolution, <0.1nm precision, >10K point /Hr

Border of CD metrology and defect inspection becomes close

Resolution, Precision

Throughput

Critical <1nm(r) Low

High

Rough 3-5nm(r)

CD-SEM

EPE Mass Measurement

HS, WS Global CDU

FEM Check

EBI

Super tool
Requirement for HVM metrology tool

\[ TMU^2 = \sigma_{\text{short-term}}^2 + \sigma_{\text{long-term}}^2 + \sigma_{\text{matching}}^2 + \sigma_{\text{other}}^2 \]

Stability, matching is required

- **Short-term ~ 0.04 nm**

- **Long-term ~ 0.06 nm**

- **Matching < 0.1 nm**

K. Ueda, et al., SPIE 8681-82 (2013) (Data of previous model)
Gap & Potentials of Hybrid Tool
# Gap from the requirement

<table>
<thead>
<tr>
<th>Requirement</th>
<th>CD-SEM</th>
<th>OCD</th>
<th>CD-AFM</th>
<th>CD-SAXS</th>
<th>SEM/STEM</th>
</tr>
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<tbody>
<tr>
<td>Sensitivity (sub-1nm)</td>
<td></td>
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<td></td>
<td>Probe effect at lateral direction</td>
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</table>

**Where to measure**

<table>
<thead>
<tr>
<th>Measure any pattern</th>
<th>In-die, Complex pattern</th>
<th>grating</th>
<th>In-die, Complex pattern</th>
<th>grating</th>
<th>In-die, Complex pattern</th>
</tr>
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</table>

**What to measure**

<table>
<thead>
<tr>
<th>EPE</th>
<th>CD</th>
<th>LER/LWR</th>
<th>OVL</th>
<th>Profile</th>
<th>HAR bottom</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td>High Voltage</td>
<td>Top view</td>
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<td></td>
<td></td>
<td></td>
<td>DBO</td>
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</tbody>
</table>

**In-line useage**

<table>
<thead>
<tr>
<th>Throughput</th>
<th>Recipe setup</th>
<th>Non-destructive</th>
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</thead>
<tbody>
<tr>
<td></td>
<td>modeling</td>
<td></td>
</tr>
<tr>
<td></td>
<td>modeling</td>
<td>Preparation</td>
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</table>
Potential of Hybrid Tool

- Smart sampling for precise measurement
- Smart recipe for OCD measurement
- Fusion map of height and EPE

- Precise 3D measurement for any complex pattern
Further ideas of Hybrid Tool

- Wafer level 3D measurement (precise, availability for complex pattern)
- Other combination?
Evolution in structure, process and material brings new requirement to CD-metrology, such as EPE metrology (including pattern fidelity check, overlay, LER/ LWR analysis), HAR pattern measurement (including bottom/underlayer measurement, 3D-profile).

In-line CD-SEM had changed its HW/ SW to suit every use application.

Though metrology technologies improve, there are many challenges to reach the requirements.

Collaboration needed
Acknowledgment

We would like to thank Gian Lorusso, Greg McIntyre, Daisuke Bizen, Takeyoshi Ohashi and all the people in imec and Hitachi team to provide the data and discussion.
<table>
<thead>
<tr>
<th>Abbreviation</th>
<th>Definition</th>
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<tr>
<td>ADI</td>
<td>After development inspection</td>
</tr>
<tr>
<td>AFM</td>
<td>Atomic force microscopy</td>
</tr>
<tr>
<td>BSE</td>
<td>Back scattered electron</td>
</tr>
<tr>
<td>CD</td>
<td>Critical dimension</td>
</tr>
<tr>
<td>CDU</td>
<td>Critical dimension uniformity</td>
</tr>
<tr>
<td>DBO</td>
<td>Diffraction based overlay</td>
</tr>
<tr>
<td>EB</td>
<td>Electron beam</td>
</tr>
<tr>
<td>EBI</td>
<td>Electron beam inspection</td>
</tr>
<tr>
<td>EF</td>
<td>Energy filter</td>
</tr>
<tr>
<td>EPE</td>
<td>Edge placement error</td>
</tr>
<tr>
<td>EUV</td>
<td>Extreme ultra violet</td>
</tr>
<tr>
<td>FEM</td>
<td>Focus exposure matrix</td>
</tr>
<tr>
<td>FET</td>
<td>Field effect transistor</td>
</tr>
<tr>
<td>FIB</td>
<td>Focused ion beam</td>
</tr>
<tr>
<td>GAA</td>
<td>Gate all around</td>
</tr>
<tr>
<td>HAR</td>
<td>High aspect ratio</td>
</tr>
<tr>
<td>HS</td>
<td>Hot spot</td>
</tr>
<tr>
<td>HVM</td>
<td>High volume manufacturing</td>
</tr>
<tr>
<td>LCDU</td>
<td>Local CDU</td>
</tr>
<tr>
<td>LELE</td>
<td>Litho etch litho etch</td>
</tr>
<tr>
<td>LER</td>
<td>Line edge roughness</td>
</tr>
<tr>
<td>LWR</td>
<td>Line width roughness</td>
</tr>
<tr>
<td>MB</td>
<td>Multi beam</td>
</tr>
<tr>
<td>MP</td>
<td>Multi patterning</td>
</tr>
<tr>
<td>MRAM</td>
<td>Magneto resistive random access memory</td>
</tr>
<tr>
<td>OCD</td>
<td>Optical CD measurement</td>
</tr>
<tr>
<td>OVL</td>
<td>Overlay</td>
</tr>
<tr>
<td>PFC</td>
<td>Pattern fidelity check</td>
</tr>
<tr>
<td>PSD</td>
<td>Power spectrum density</td>
</tr>
<tr>
<td>SAQP</td>
<td>Self aligned quadruple patterning</td>
</tr>
<tr>
<td>SAXS</td>
<td>Small angle X-ray spectroscopy</td>
</tr>
<tr>
<td>SE</td>
<td>Secondary electron</td>
</tr>
<tr>
<td>SEM</td>
<td>Scanning electron microscope</td>
</tr>
<tr>
<td>STEM</td>
<td>Scanning transmission electron microscope</td>
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Thank you

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