The Status and Future of Metrology: Challenges from the ITRS Metrology Roadmap

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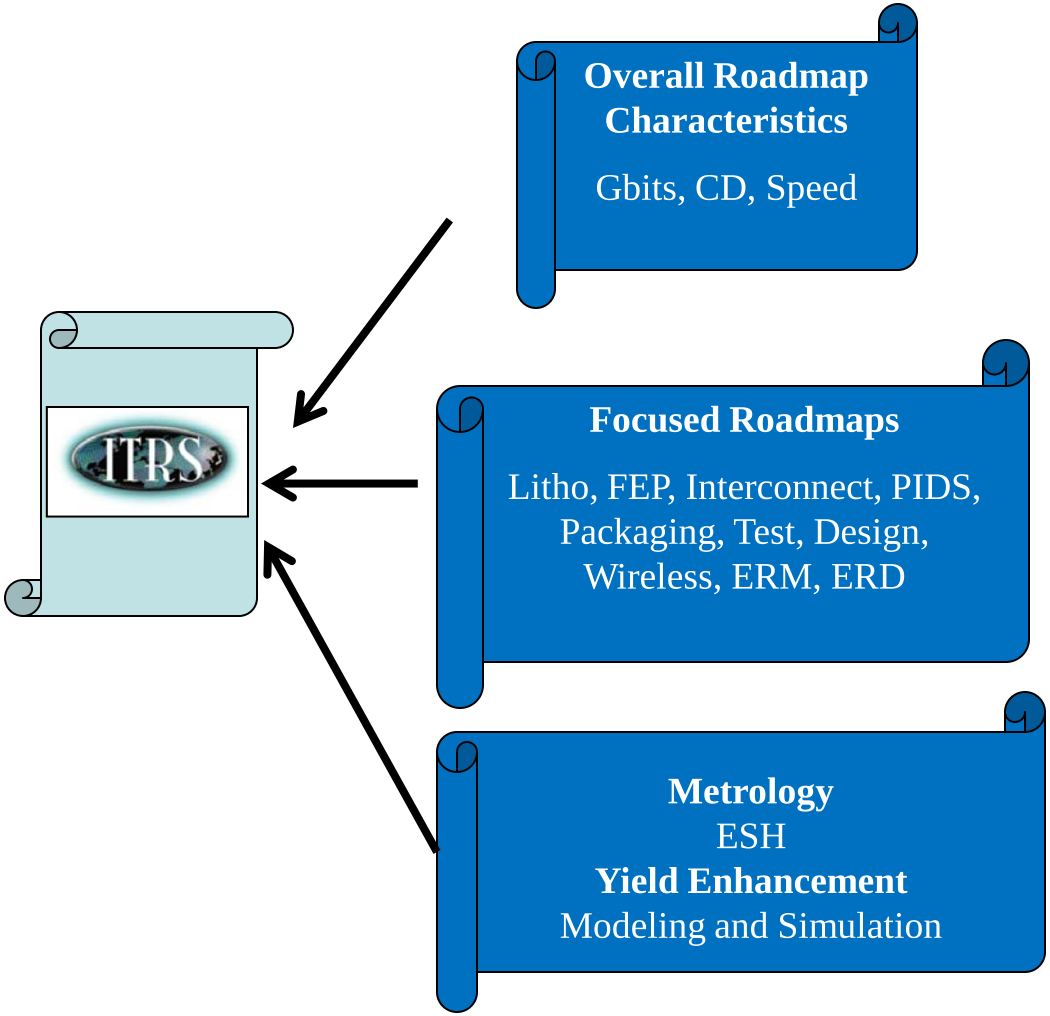
Center for Nanoscale Metrology

(NC)3

INDEX
INSTITUTE FOR NANOELECTRONICS
DISCOVERY AND EXPLORATION

ITRS Process
www.itrs.net



Overall Roadmap Characteristics

Gbits, CD, Speed

Focused Roadmaps

Litho, FEP, Interconnect, PIDS, Packaging, Test, Design, Wireless, ERM, ERD

Metrology
ESH
Yield Enhancement
Modeling and Simulation

2011 – Text & Requirements Update

2012 – Requirements Update

3 Meetings/year

Spring Europe

Summer US – Semicon West

Winter – Japan/Taiwan/ Korea

Extreme CMOS

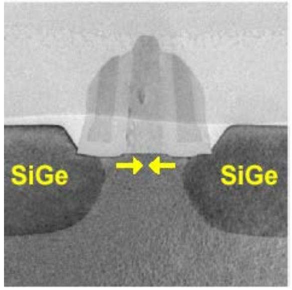
NanoElectronics – NanoTechnology – NanoScale Science

15 year Horizon
Non-classical CMOS

The Future

Strain
Metrology

Yesterday
90 nm ½ Pitch

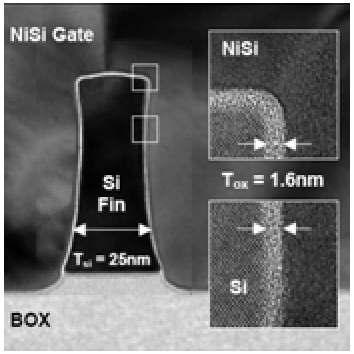


Strain
Enhanced Mobility

High κ/interface
& Metal Gate
Metrology

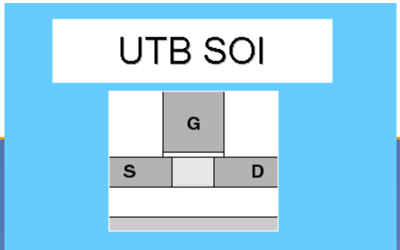
Today
<32 nm ½ pitch

New Materials



CMOS
pMOS FINFET

Metrology
For New
Structures



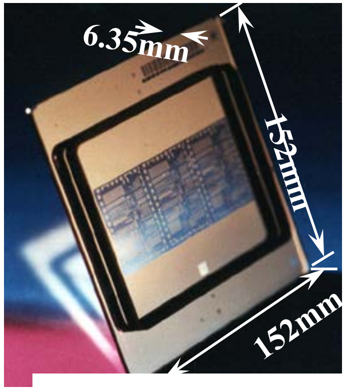
2010 Metrology Roadmap

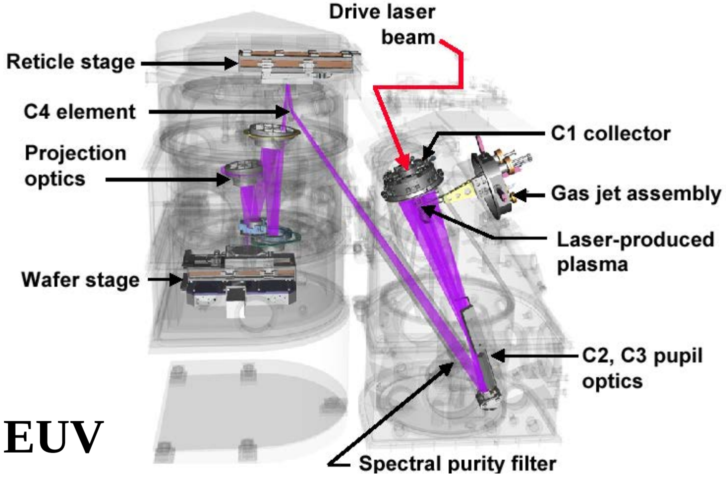
		2010	2013	2016	2019
	Flash 1/2 pitch (nm)	***32***	***22***	***16***	***11***
	DRAM ½ Pitch (nm)	**45**	**32**	**22**	**16**
	MPU Printed Gate Length (nm)	**41**	**28**	**20**	**14.0**
	MPU Physical Gate Length (nm)	**27**	**20**	**15.0**	**12.0**
	Wafer Overlay Control (nm) - 20% DRAM	**9.0**	**6.0**	**5.0**	**3.0**
	Wafer Overlay Control Double Patterning (nm)	**6**	**4**	**2**	**1**
	Lithography Metrology				
Gate	Physical CD Control (nm) Allowed Litho Variance = 3/4 Total Variance	**2.8**	**2.1**	**1.6**	**1.2**
	Wafer CD metrology tool **uncertainty** (3σ, nm) at P/T = 0.2	**0.55**	**0.42**	**0.31**	**0.25**
	Etched Gate Line Width Roughness (nm) <8% of CD	**2.1**	**1.6**	**1.2**	**1.0**
Dense Lines	Printed CD Control (nm) Allowed Litho Variance = 3/4 Total Variance	**3.3**	**2.3**	**1.7**	**1.1**
	Wafer CD metrology tool **uncertainty** (3s, nm) at P/T = 0.2	**0.7**	**0.5**	**0.4**	**0.3**
	Double Patterning Overlay Metrology				
	Double Exposure and Etch - Process Range (nm)	**6.4**	**5.1**	**4.0**	**3.2**
	Double Exposure and Etch - **Uncertainty** (nm)	**1.3**	**1.0**	**0.8**	**0.6**
	Spacer PEE process				
	First pass CD control (after etch) - Process Variation (nm)	**3.0**	**2.4**	**1.9**	**1.6**
	First pass CD control (after etch) - Uncertainty (nm)	**0.6**	**0.5**	**0.4**	**0.3**
	Front End Processes Metrology				
	High Performance Logic EOT equivalent oxide thickness (EOT), nm	**0.65**	**0.5**	**0.5**	**0.5**
	Logic Dielectric EOT Precision 3σ, nm	**0.0026**	**0.002**	**0.002**	**0.002**
	Interconnect Metrology				
	Barrier layer thick (nm)	**3.3**	**2.4**	**1.7**	**1.3**
	Void Size for 1% Voiding in Cu Lines	**4.5**	**3.2**	**2.2**	**1.6**
	Detection of Killer Pores at (nm) size	**4.5**	**3.2**	**2.2**	**1.6**

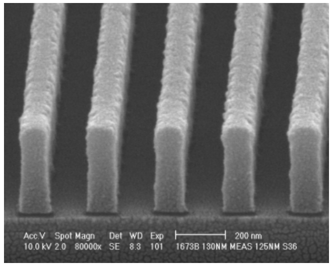
AGENDA

- **Lithography Metrology**
- FEP Metrology
- Interconnect Metrology
- Beyond CMOS
- Conclusions

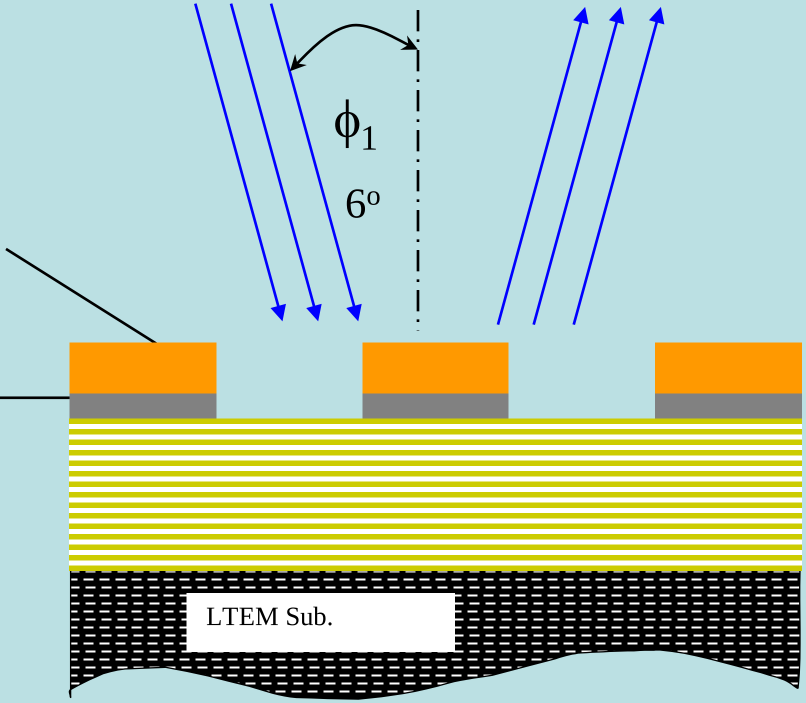
Patterning via EUV Lithography







Patterning via EUV Lithography



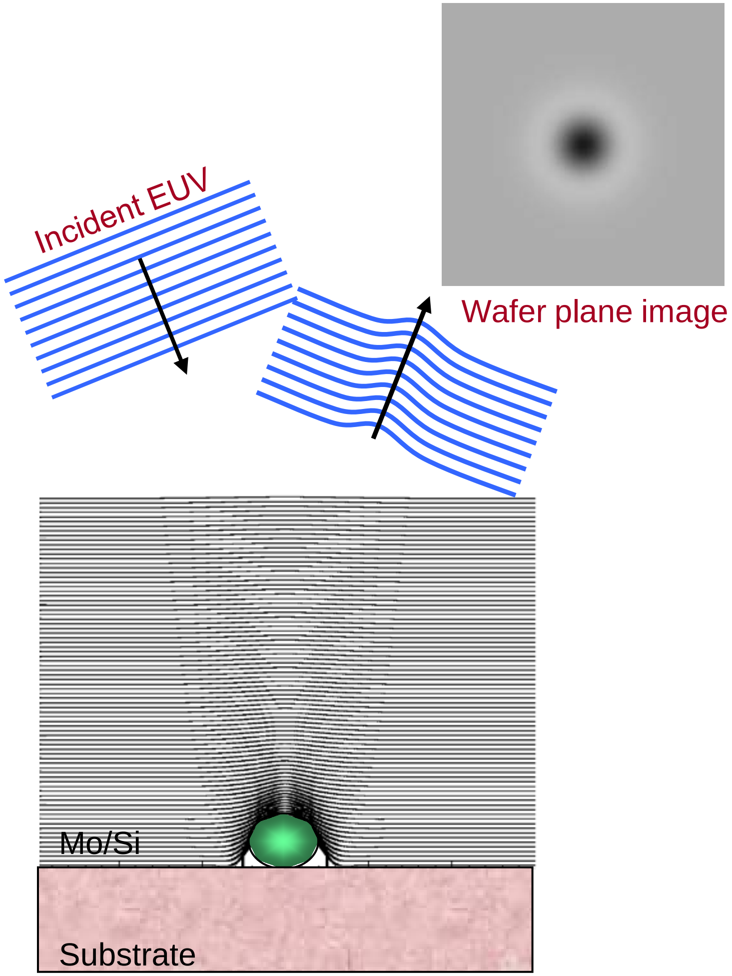
Patterned Absorbers
~ 100 nm thick
(e.g. Al, Cr, TaN, W)

Buffer Layer
~ 50 nm thick
(e.g. SiO_2)

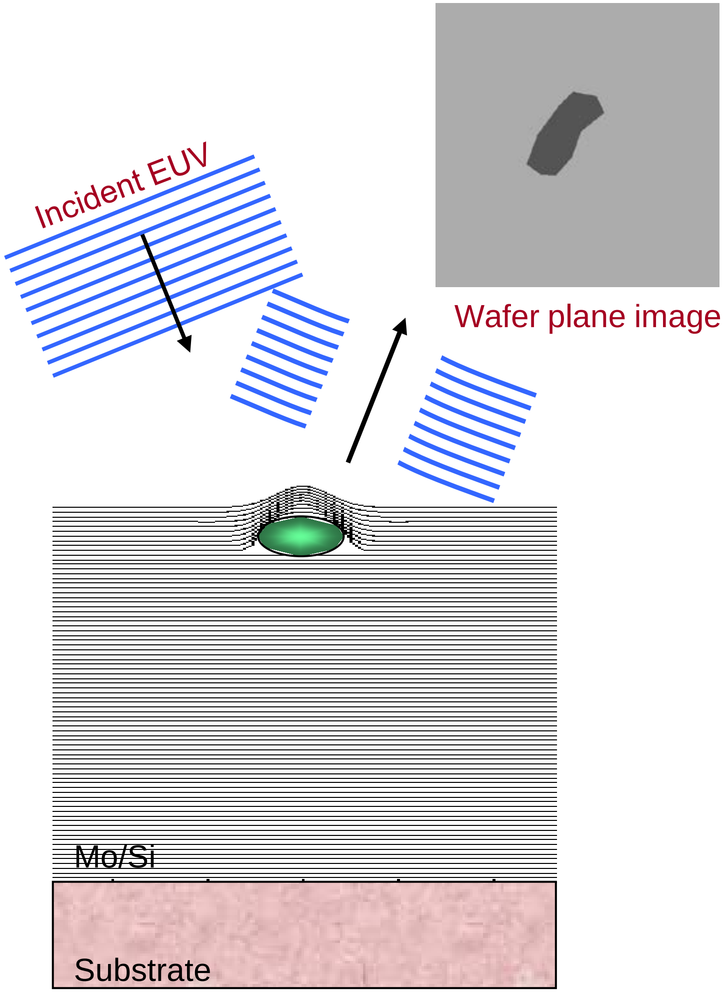
Reflective Multilayers
~ 300 nm thick
(Mo - Si = 13.5nm)
40 - 50 Pairs

Phase and Amplitude Defects

“Phase defects”



“Amplitude defects”

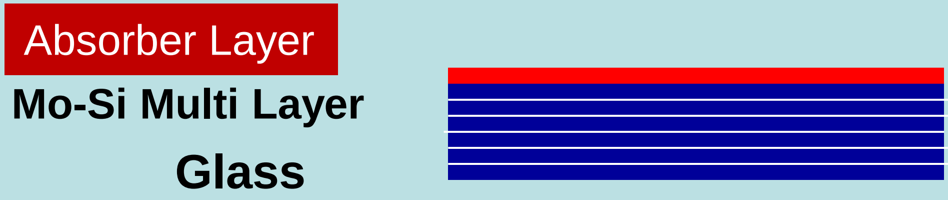


Phil Seidel 2003

EUV Lithography Metrology

Mask Substrate Defect Inspection

Mask Blank Inspection

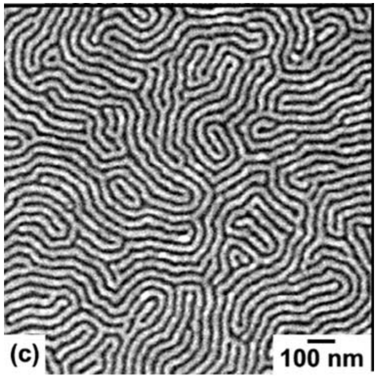


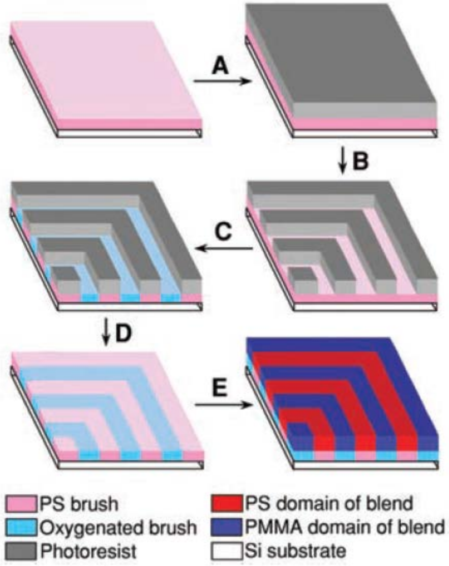
AIMS

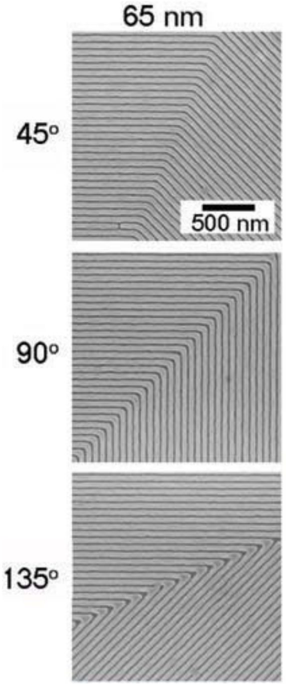
Project what mask will print onto a detector

Patterned Mask Inspection

Self Assembly Patterning





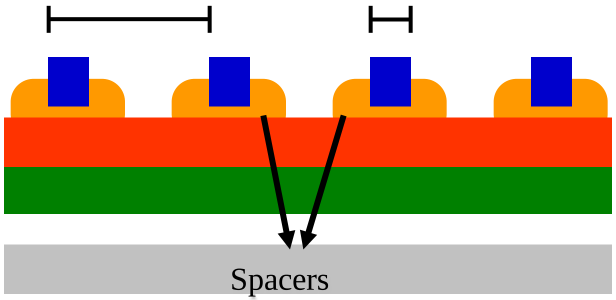


Block co-polymers

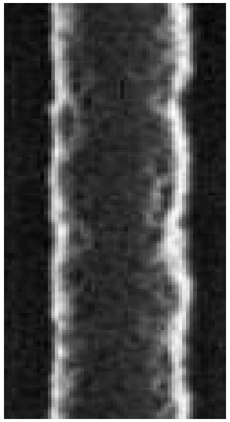
Black and Bezencenet, IEEE Trans NanoTech 3, (2004) p 412
Stoykovich, et al, Science 308 (2005), 1442

Lithography Metrology

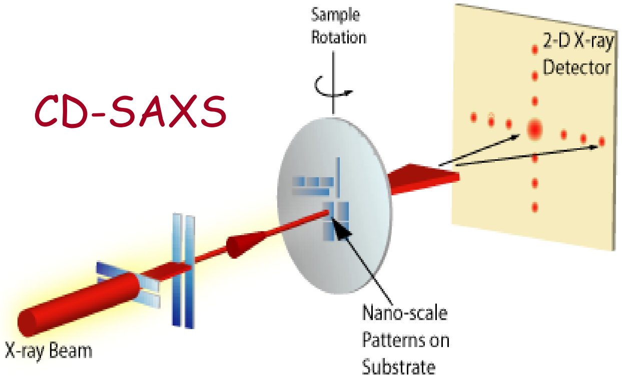
Dual Patterning



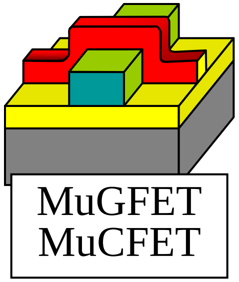
Line Edge Roughness

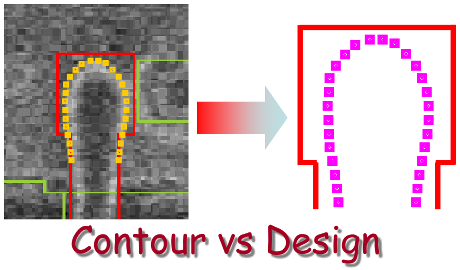


CD Metrology Extendibility

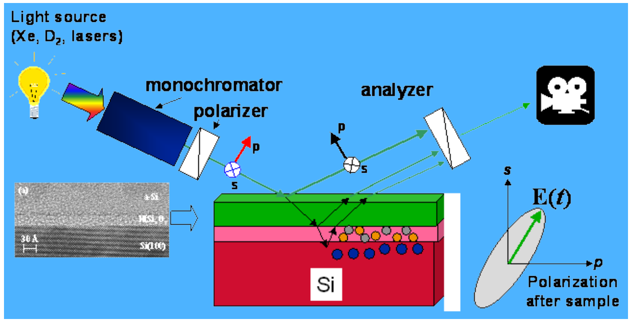


Litho Metrology for 3D Devices





Mueller Matrix Ellipsometry



Lithography Metrology Requirements

		2010	***2013***	***2016***	***2019***	***2024***
	Flash 1/2 pitch (nm)	***32***	***22***	***16***	***11***	***6.3***
	DRAM ½ Pitch (nm)	**45**	**32**	**22**	**16**	**8.9**
	MPU Printed Gate Length (nm)	**41**	**28**	**20**	**14.0**	**7.9**
	MPU Physical Gate Length (nm)	**27**	**20**	**15.0**	**12.0**	**7.4**
	Wafer Overlay Control (nm) - 20% DRAM	**9.0**	**6.0**	**5.0**	**3.0**	**?**
	Wafer Overlay Control Double Patterning (nm)	**6**	**4**	**2**	**1**	**?**
	Lithography Metrology					
Gate	Physical CD Control (nm) Allowed Litho Variance = 3/4 Total Variance	**2.8**	**2.1**	**1.6**	**1.2**	**0.8**
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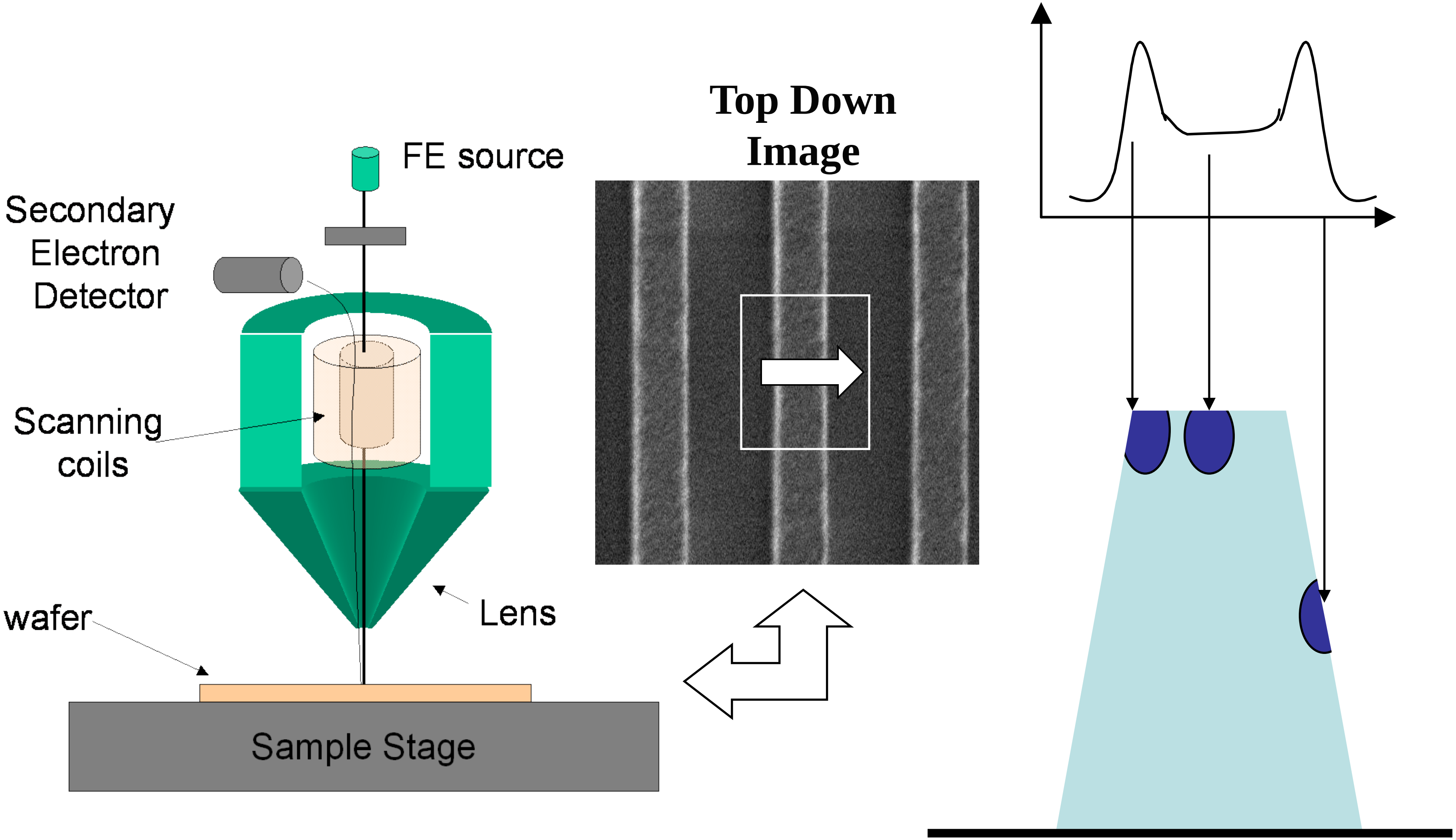
Dense Lines	Printed CD Control (nm) Allowed Litho Variance = 3/4 Total Variance	**3.3**	**2.3**	**1.7**	**1.1**	**0.7**
	Wafer CD metrology tool **uncertainty** (3s, nm) at P/T = 0.2	**0.7**	**0.5**	**0.4**	**0.3**	**0.1**

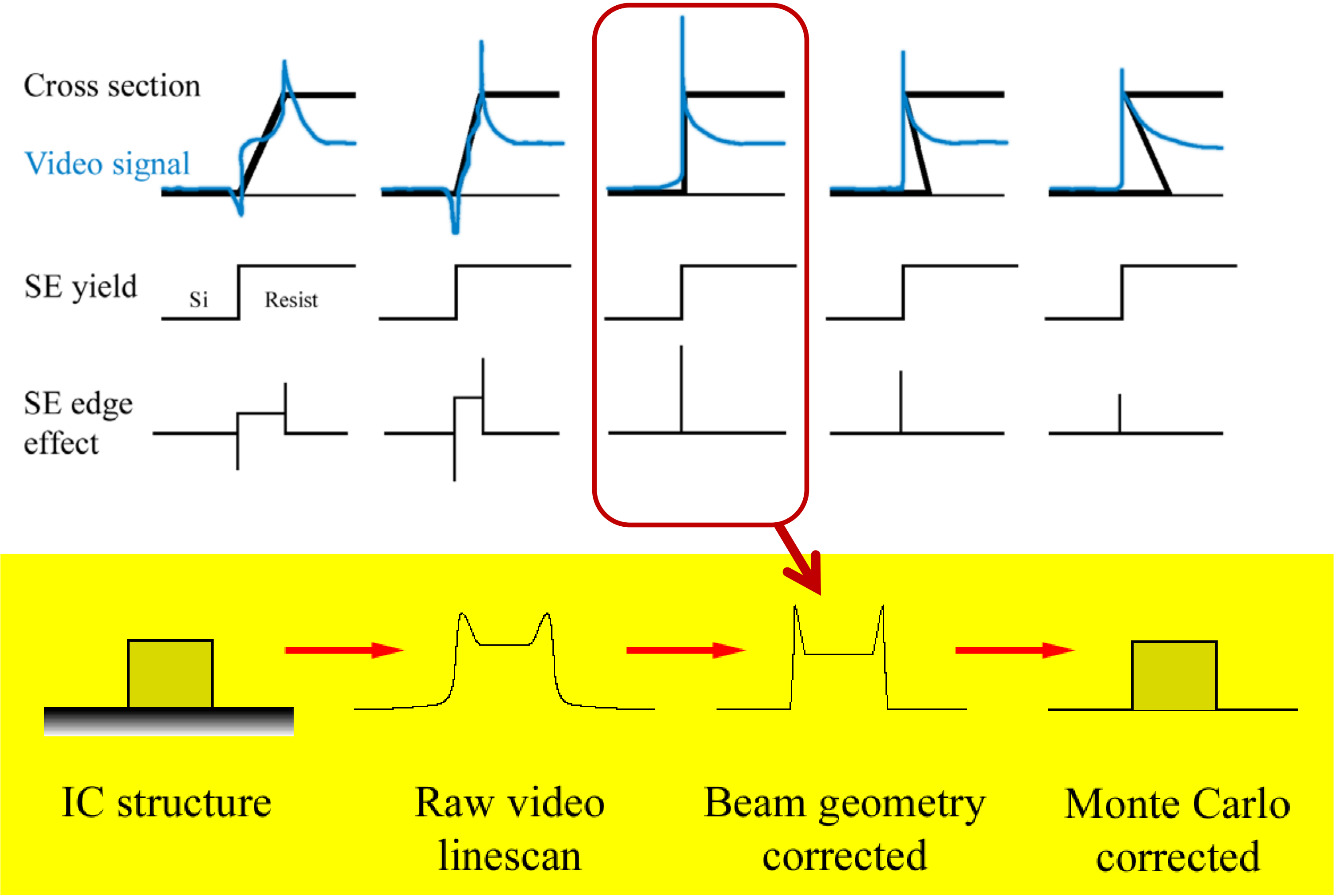
Patterning Metrology

Typically - Line Edge has Higher Intensity



NIST Research Finds 3D info

Before 2000



IC structure

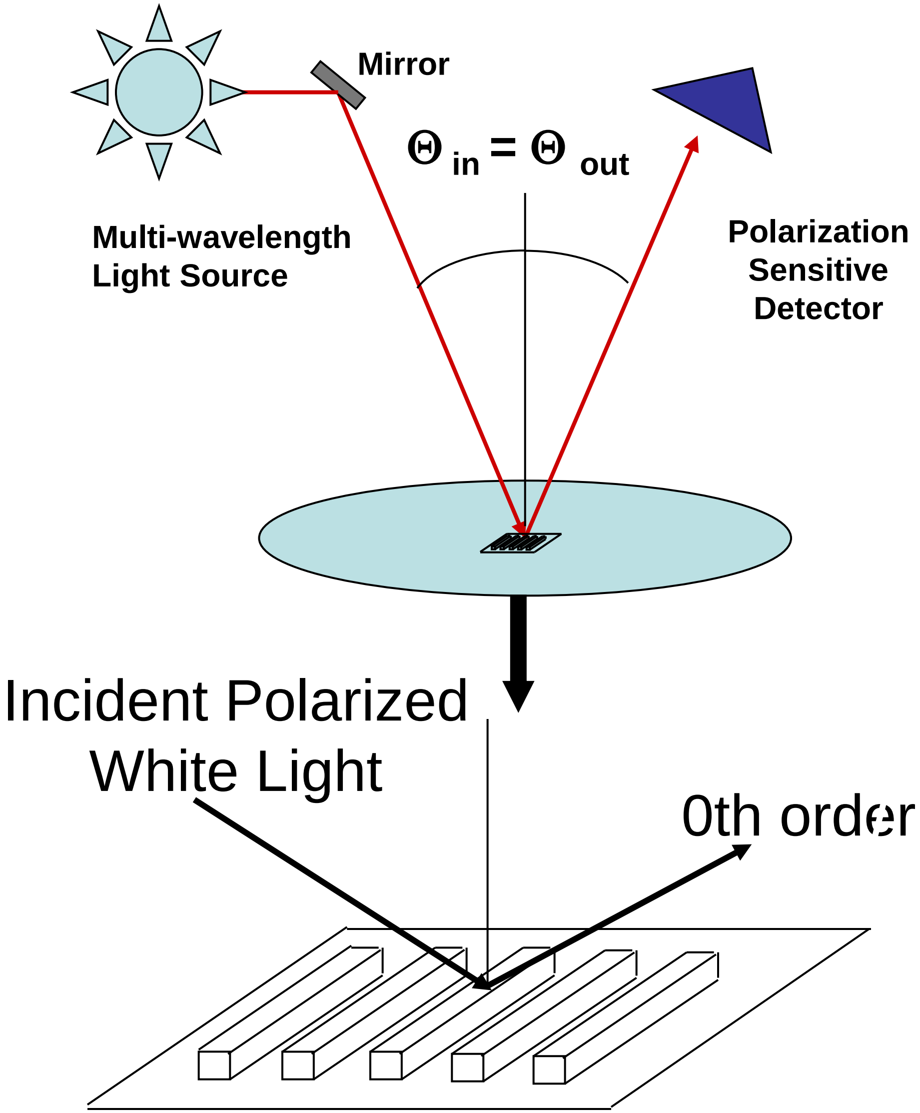
Raw video linescan

Beam geometry corrected

Monte Carlo corrected

Andras Vladar, Mike Postek, & John Villarrubia

Scatterometry Was Introduced



Mirror

Multi-wavelength
Light Source

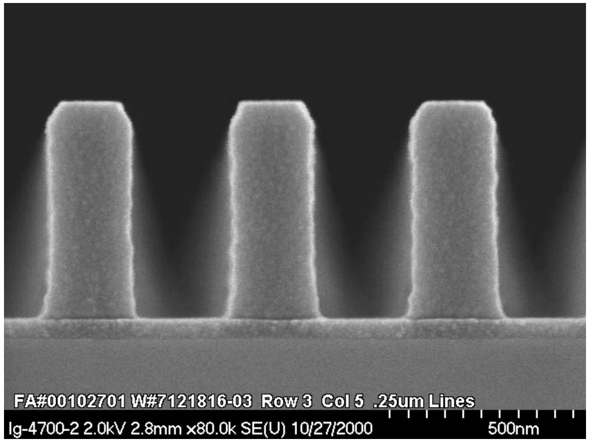
$\Theta_{in} = \Theta_{out}$

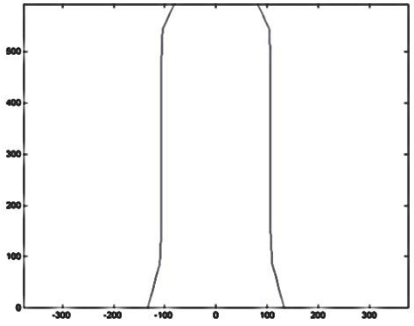
Polarization
Sensitive
Detector

Incident Polarized
White Light

0th order

Real Time Calculation of line width & shape & Libraries





See – Scatterometry by Chris Raymond in Handbook of Silicon Semiconductor Metrology

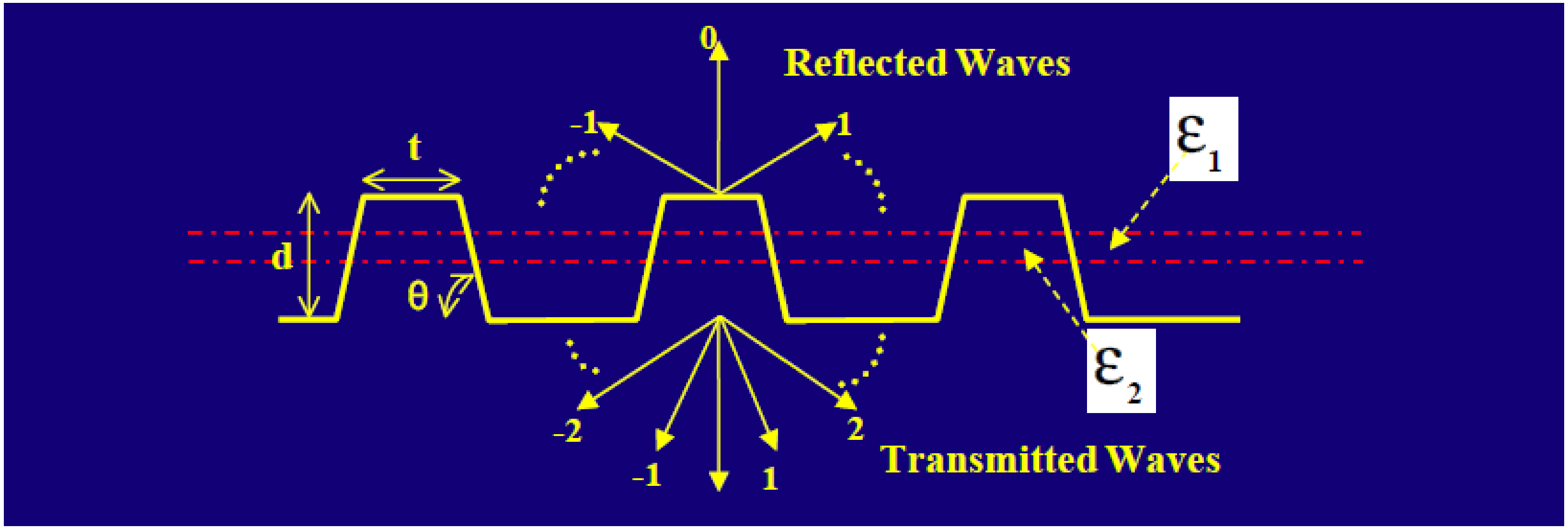
Rigorous Couple Wave Analysis

Grating - periodic in x direction

$$\varepsilon(x) = \sum_h \varepsilon_h \exp\left(j \frac{2\pi}{\Lambda} h x \right)$$

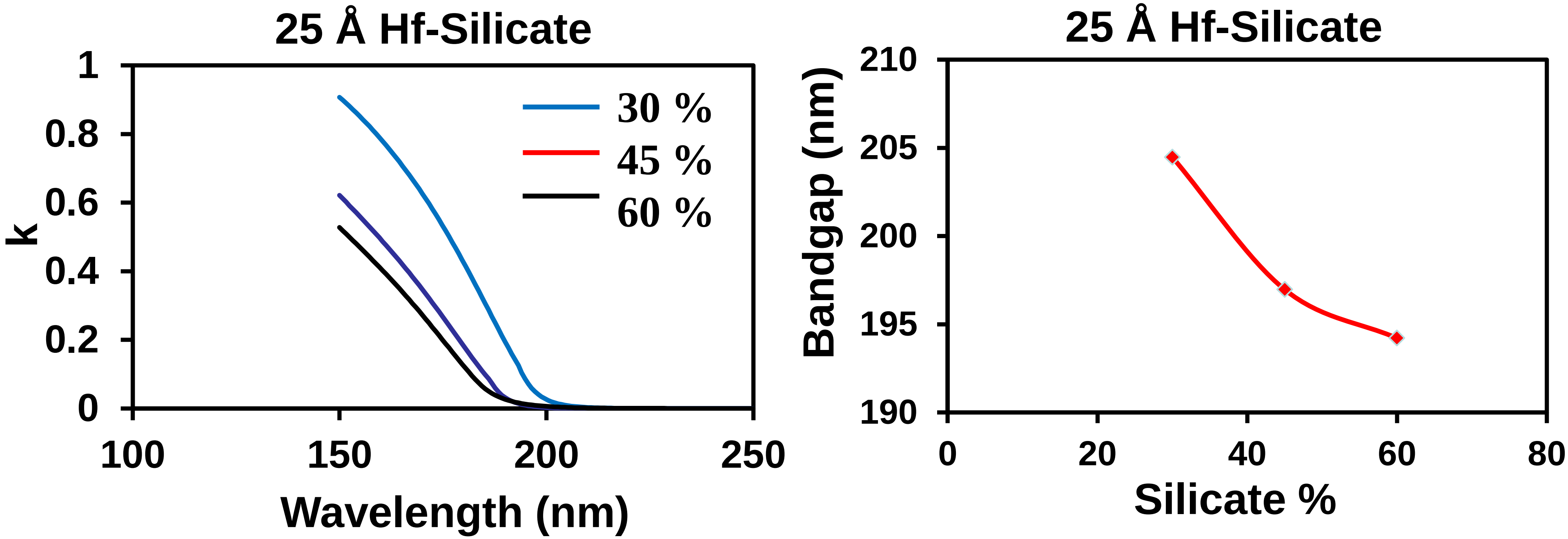
Solve coupled wave equations by ordinary matrix techniques with matched boundary conditions in the interface of air and substrate.

$$\frac{\partial S_{yi}}{\partial z} = k U_{xi} \qquad \frac{\partial U_{xi}}{\partial z} = \left(\frac{k_{xi}^2}{k} \right) S_{yi} - k \sum_p \varepsilon_{(i-p)} S_{yp}$$

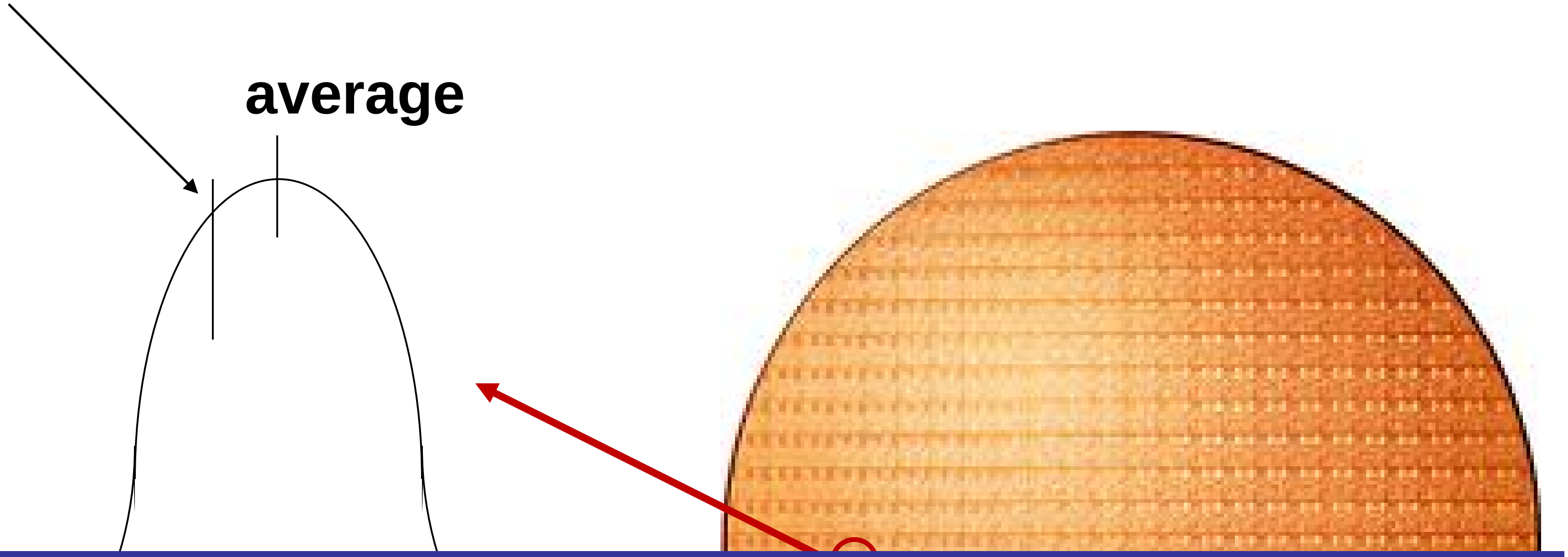


Scatterometry -- What is n and k ?

High K Optical Model Requirement
Variability with Composition and Process



What are you measuring?



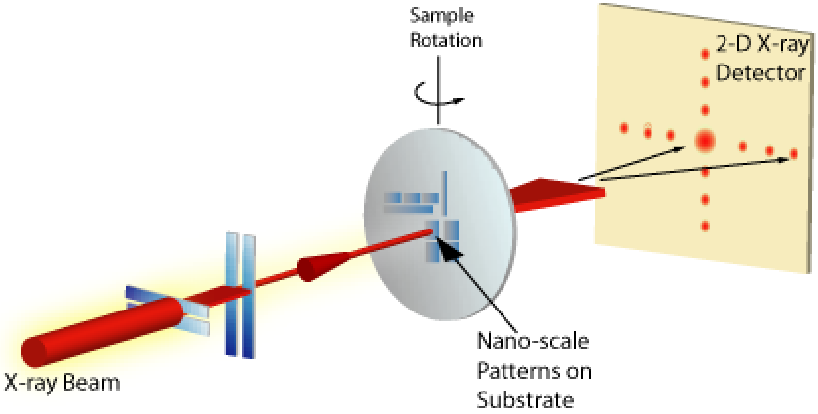
single value from distribution

average

Measurement Convergence -
CD-SEM measurement of multiple lines in same image and Scatterometry determined Average Value

Potential New CD Methods

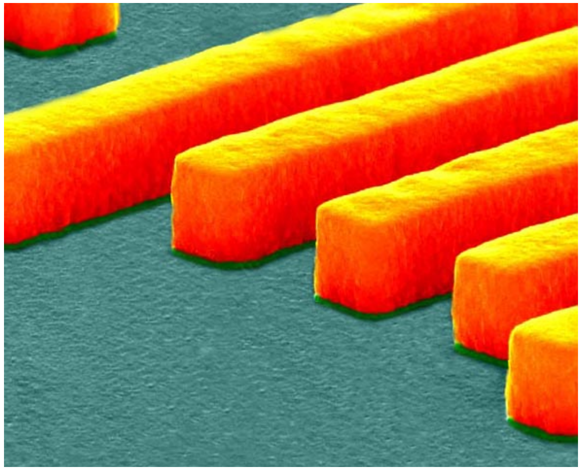
CD-SAXS



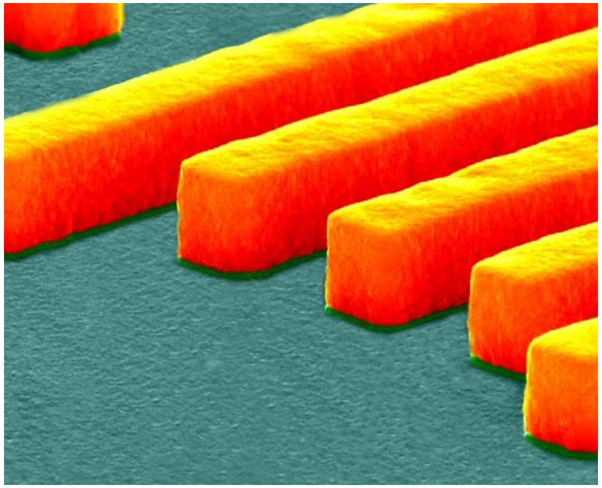
Winli Wu NIST

He Ion Microscope
New Imaging Physics

More Signal from Existing Methods

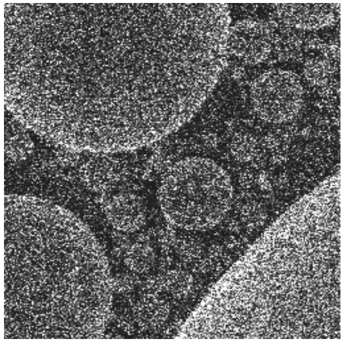


- **Mueller Matrix Ellipsometry**

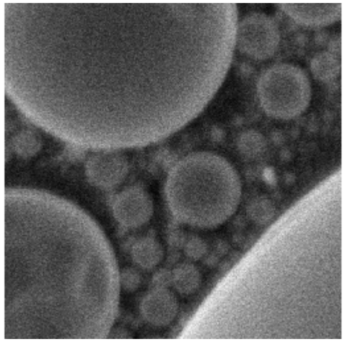


- **3D Dimensional SEM Metrology**

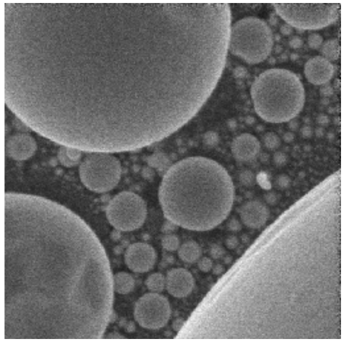
3D Metrology - CD-SEM



Fast single frame

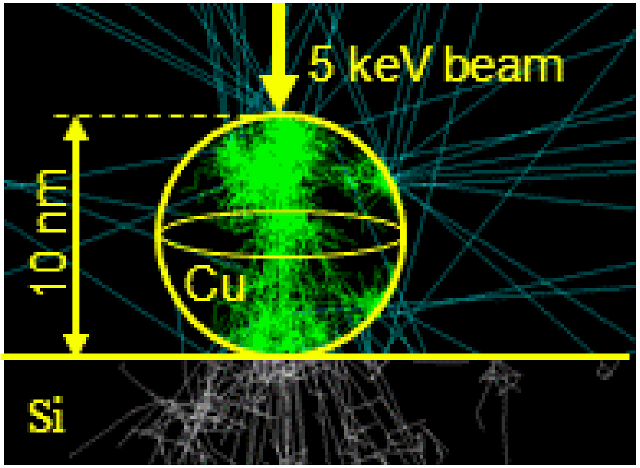


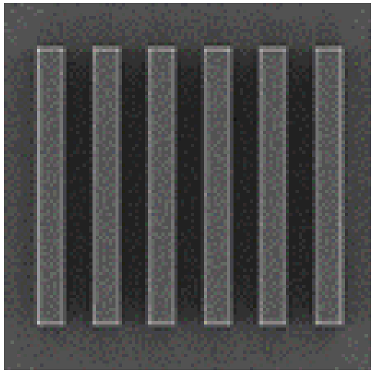
Traditional frame averaging

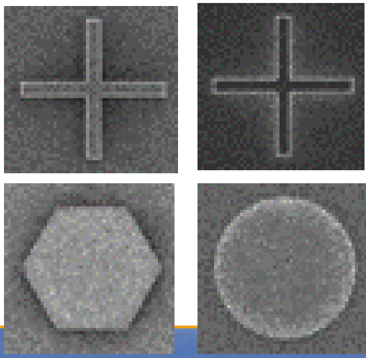


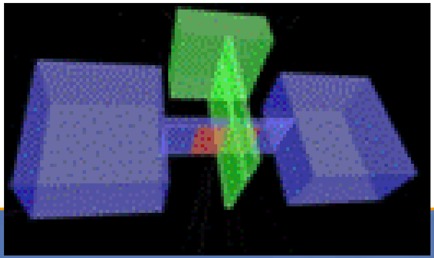
Drift-corrected frame averaging

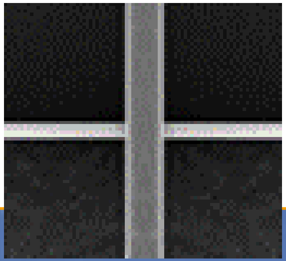
Better CD SEM Via Small Improvements









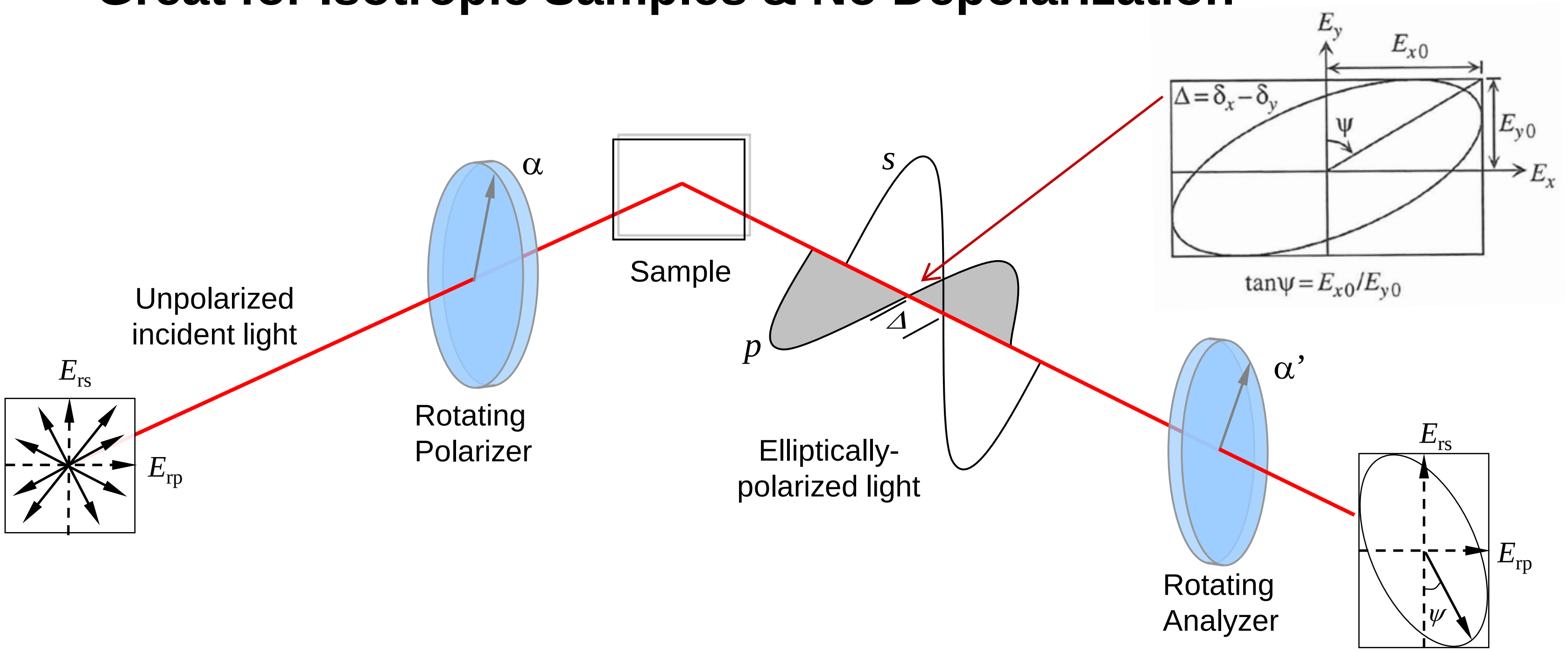


3D model determines all structure dimensions

Andras Vladar, NIST

Rotating-polarizer ellipsometry ($P_R SA$)

One example from many types of ellipsometers
Great for Isotropic Samples & No Depolarization



$$S = \begin{bmatrix} s_0 \\ s_1 \\ s_2 \\ s_3 \end{bmatrix} = \begin{bmatrix} I_x + I_y \\ I_x - I_y \\ I_{\pi/4} - I_{-\pi/4} \\ I_{LCP} - I_{RCP} \end{bmatrix}$$

Stokes Vector

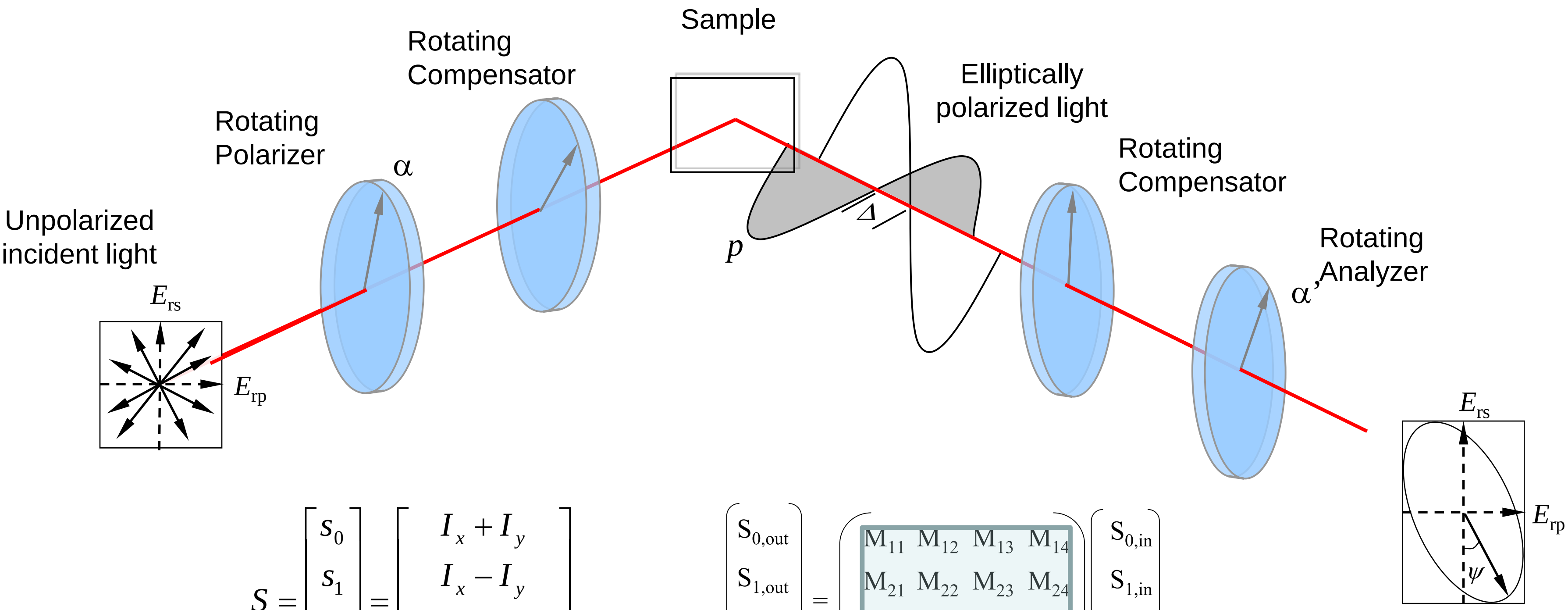
$$\begin{pmatrix} S_{0,out} \\ S_{1,out} \\ S_{2,out} \\ S_{3,out} \end{pmatrix} = \begin{pmatrix} \boxed{\begin{matrix} M_{11} & M_{12} & M_{13} \\ M_{21} & M_{22} & M_{23} \\ M_{31} & M_{32} & M_{33} \end{matrix}} & \begin{matrix} M_{14} \\ M_{24} \\ M_{34} \end{matrix} \\ \begin{matrix} M_{41} & M_{42} & M_{43} \end{matrix} & M_{44} \end{pmatrix} \begin{pmatrix} S_{0,in} \\ S_{1,in} \\ S_{2,in} \\ S_{3,in} \end{pmatrix}$$

Mueller Matrix

$$\tan \Psi e^{i\Delta} = \frac{r^P}{r^S}$$

Dual Rotating Compensator Ellipsometer (RC2)

Laboratory Ellipsometer
Great for All Types of Samples



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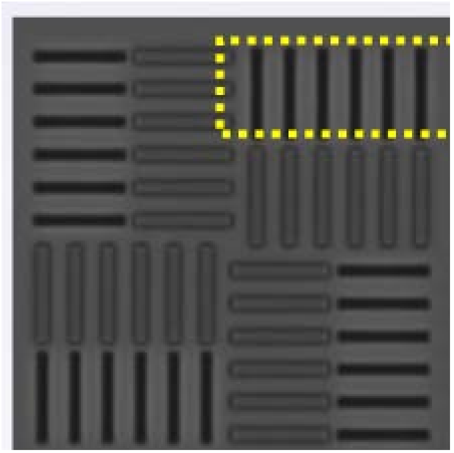
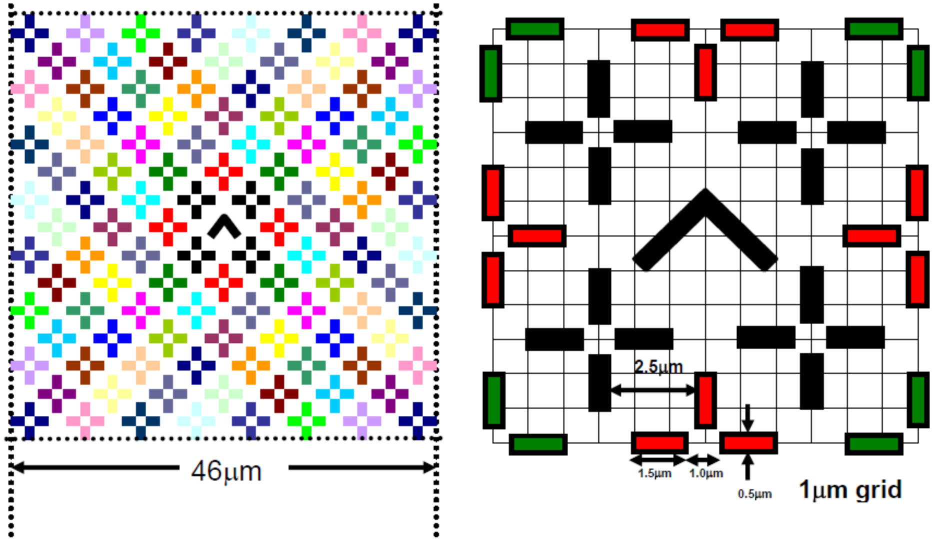
Mueller Matrix

Diffraction Effects and Scatterometry



AIM Target



(a) (b)

*Blossom target in
(a) full view and (b) center detail*

K. Suzuki & B.W. Smith,
Microlithography: Science and Technology,
Part III Chapter 14

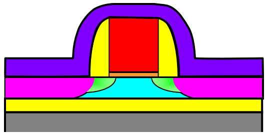
C.P. Ausschnitt et al, Proc SPIE 6152, 615210, (2006)

AGENDA

- Lithography Metrology
- **FEP Metrology**
- Interconnect Metrology
- Beyond CMOS
- Conclusions

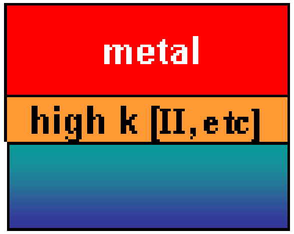
Metrology for New Structures

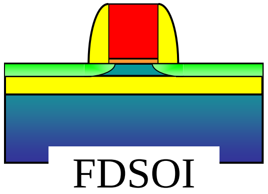
EOT & Defects for Alternate Channel Materials



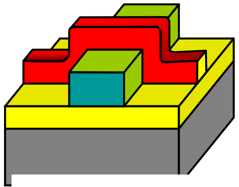
+ III/V and Ge High μ Alternative Channel Materials

Metrology for Generation II and III Metal Gate/High k stacks



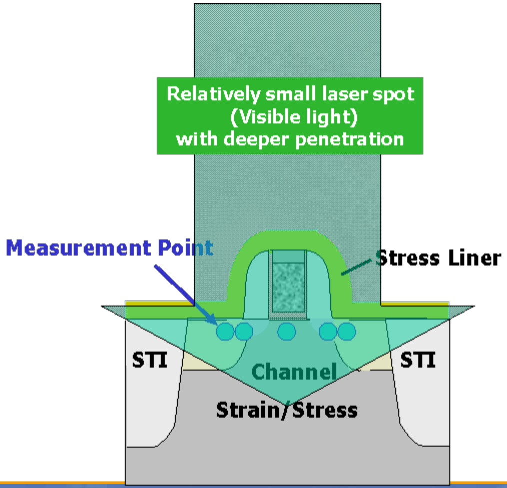


CD/Sidewall/Height/Stress Metrology for 3D Devices



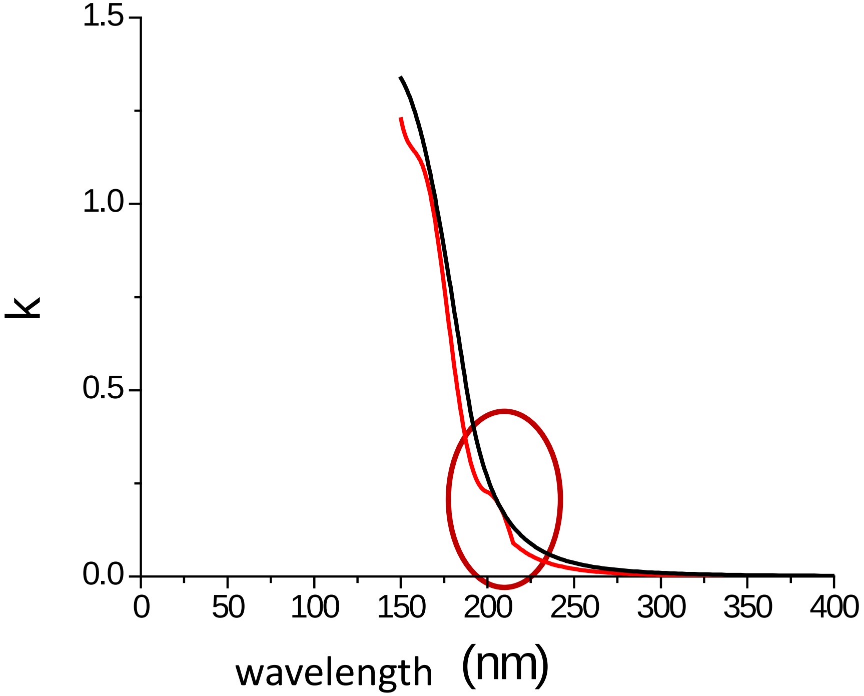
MuGFET
MuCFET

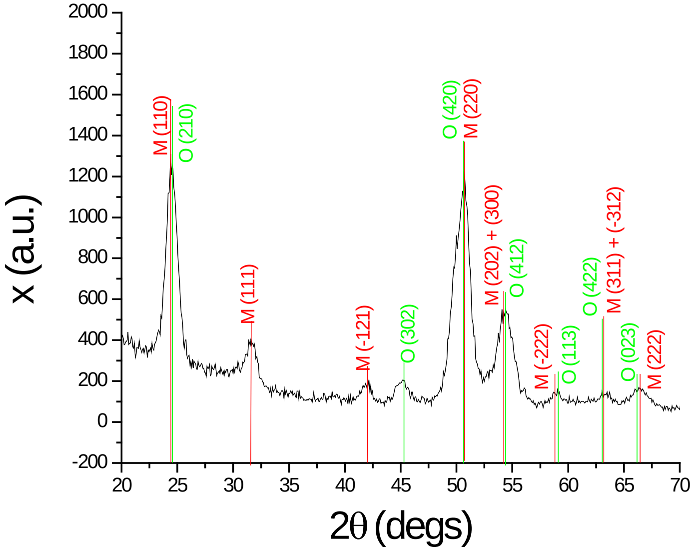
Nano-topography & Local Stress measurements



New Memory Materials Phase Change Memory

Optical Properties of next Gen High k





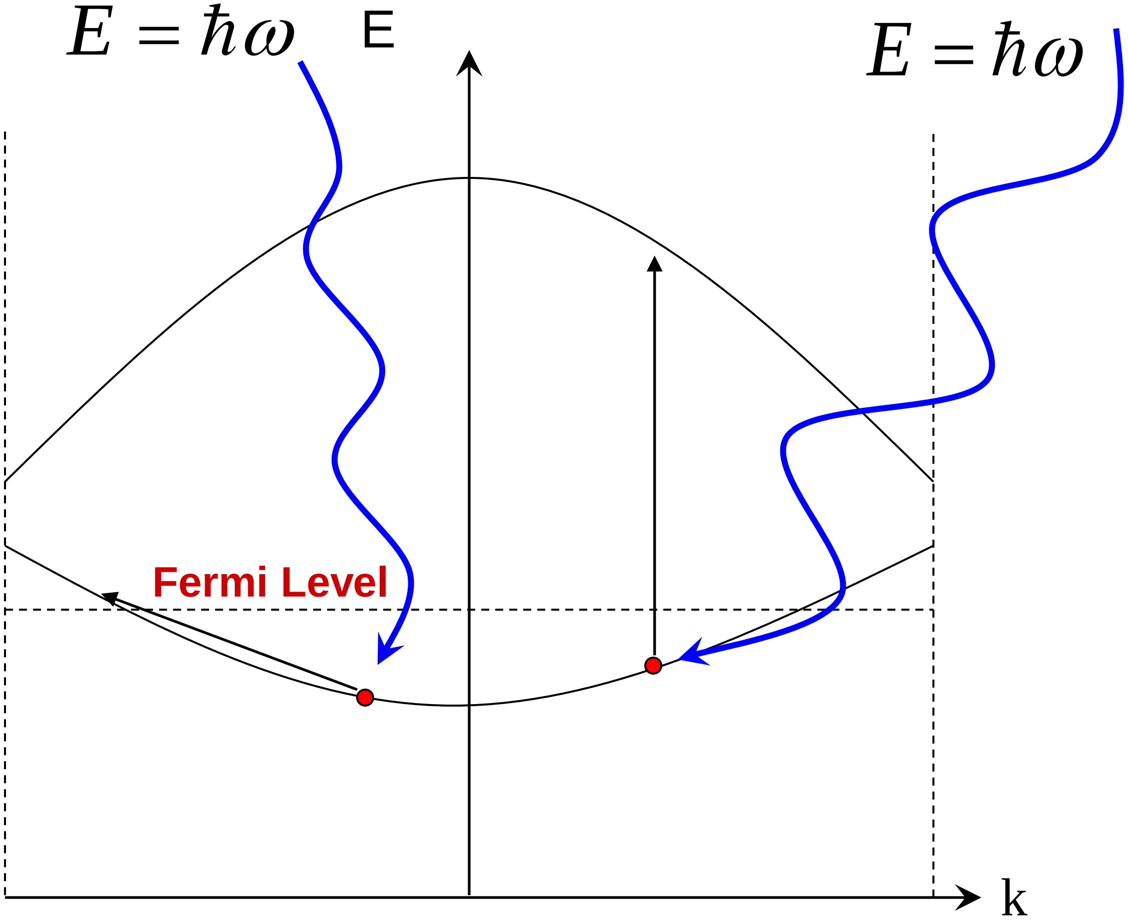
Measuring Interfacial Layer is more challenging

TEL – CNSE Collaboration Steve Consiglio/ Rob Clark, Gert Leusink TEL / Josh LaRose – CNSE

Optical Model for NanoScale Metal Film

Drude Oscillator - Free Electron

Lorentz Oscillator - Bound Electron



$$\varepsilon_1 = \varepsilon_1^f + \varepsilon_1^b$$

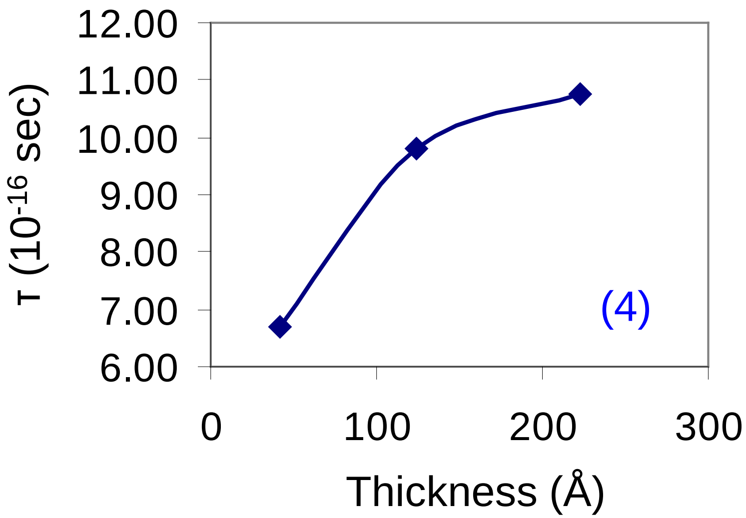
$$\varepsilon_2 = \varepsilon_2^f + \varepsilon_2^b$$

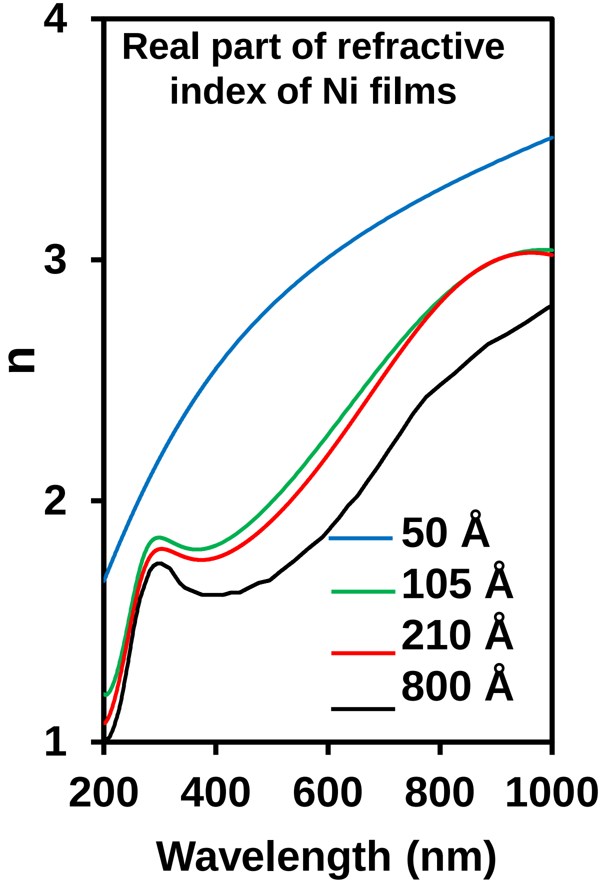
$$\tilde{\varepsilon} = \varepsilon_1 + i\varepsilon_2 = (\tilde{N})^2 = (n+ik)^2 = (n^2 - k^2) + 2ink$$

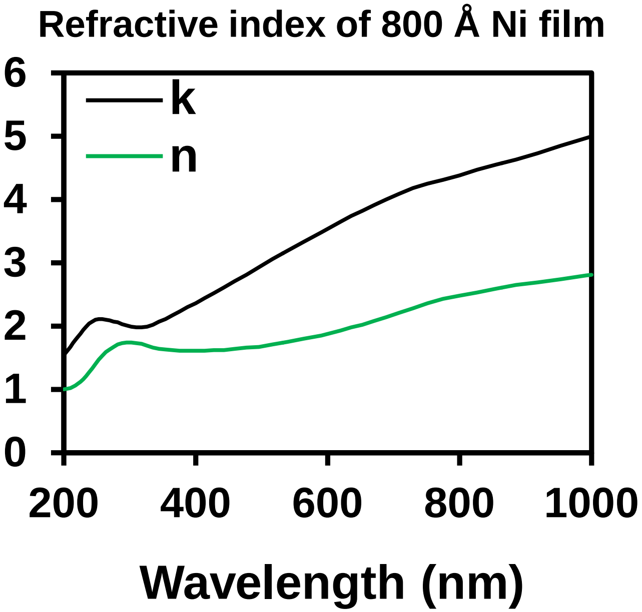
Thickness Dependent Metal n and k

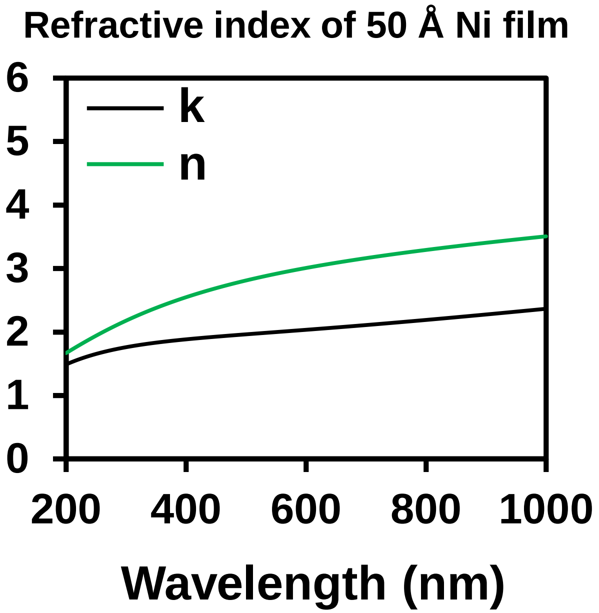
$$\frac{1}{\tau_f} = \frac{1}{\tau_{bulk}} + \frac{v_F}{\lambda}$$

$$\lambda = \left[\frac{2(1-\Re)}{3\Re}\right] R_g$$




Real part of refractive index of Ni films


Refractive index of 800 Å Ni film


Refractive index of 50 Å Ni film

Gap in Dopant Metrology

- Emphasis on Dopant Metrology
  - USJ Conference

- SOI impacts methods such as **photomodulated optical reflectance**

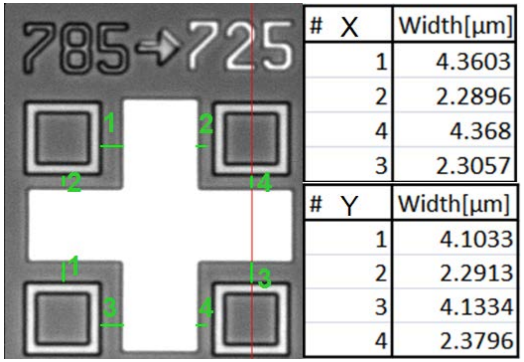
- **Start with the Theory – see** JOURNAL OF APPLIED PHYSICS **108**, 104908 (2010)

AGENDA

- Lithography Metrology
- FEP Metrology
- **Interconnect Metrology**
- Beyond CMOS
- Conclusions

Metrology for Future 3D Interconnect

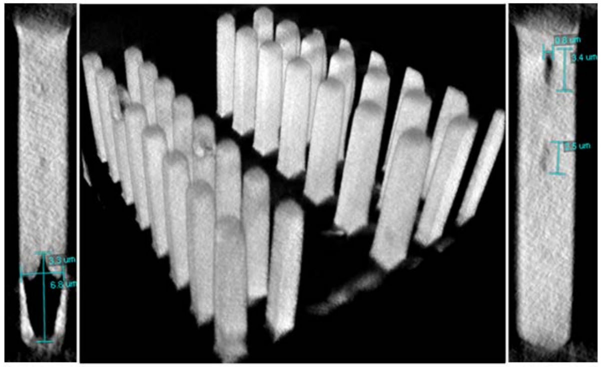
Overlay – IR Microscopy



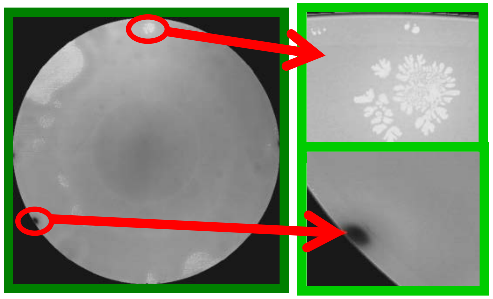
# X	Width[µm]
1	4.3603
2	2.2896
4	4.368
3	2.3057

# Y	Width[µm]
1	4.1033
2	2.2913
3	4.1334
4	2.3796

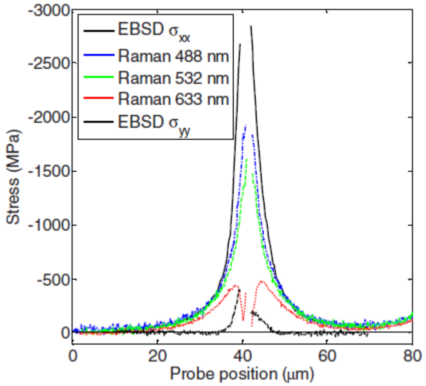
X-Ray Microscopy



Bonding Defects – SAM Scanning Acoustic Microscopy



Stress Metrology Raman Microscopy



Lai Way Kong & Alain Diebold – CNSE Ehrenfried Zschech, Fraunhofer, Andy Rudack SEMATECH

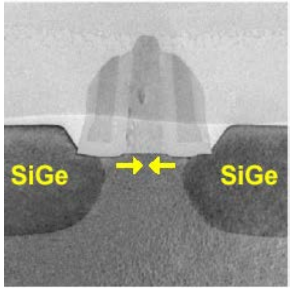
AGENDA

- Lithography Metrology
- FEP Metrology
- Interconnect Metrology
- **Beyond CMOS**
- Conclusions

Extreme and Beyond CMOS

Strain
Metrology

Yesterday
90 nm ½ Pitch



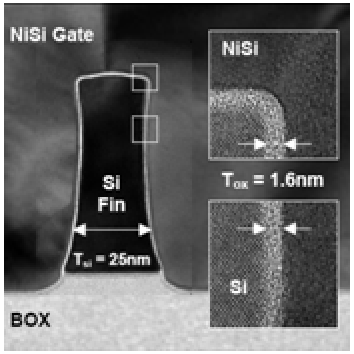
**Strain
Enhanced Mobility**

High κ/interface
& Metal Gate
Metrology

Today
<32 nm ½ pitch

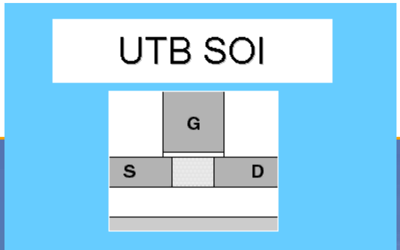
New Materials

15 year Horizon
Non-classical CMOS

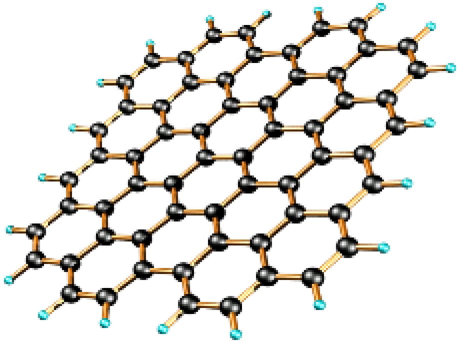


**CMOS
pMOS FINFET**

Metrology
For New
Structures



Beyond CMOS

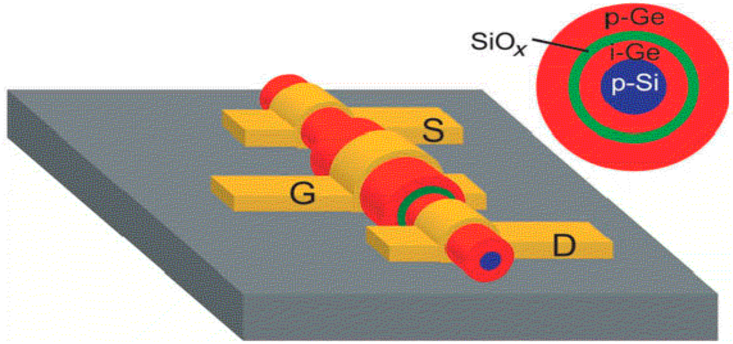


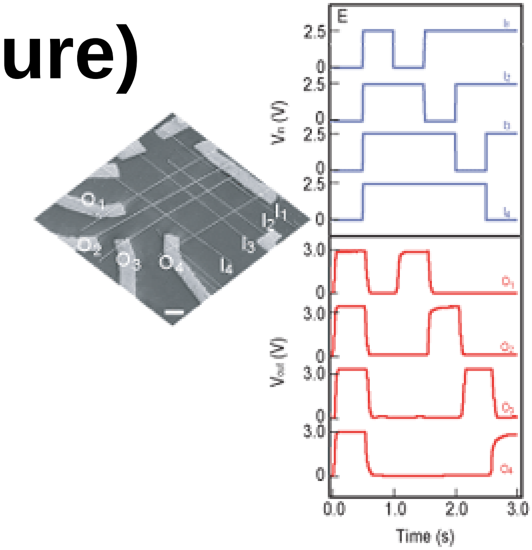
Is Graphene *THE* material?

Metrology
For New
Switches

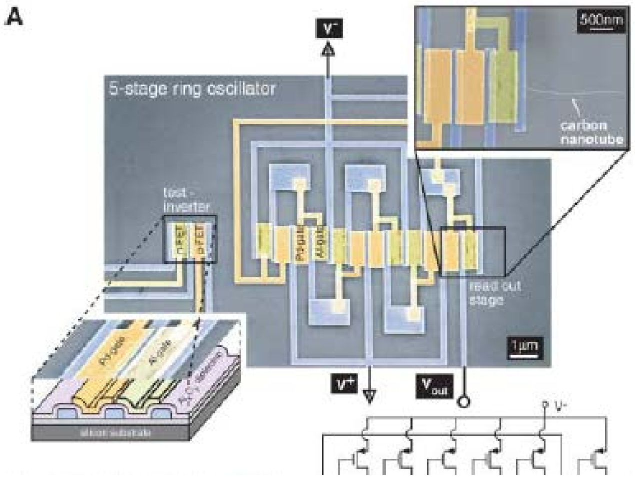
Transition to Beyond CMOS

Nanowire Electronics (Lieber -Nature)





NanoTube Electronics (Avouris – Chen, Science)



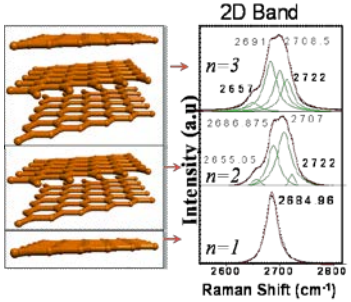
18 um long
Carbon nanotube

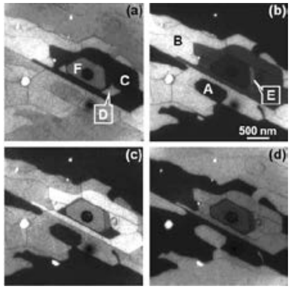
Ring Oscillator
5 CMOS inverters
= 10 FETs

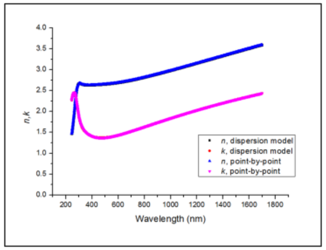
INDEX – Metrology for Graphene

High carrier mobility and structural robustness have driven a considerable effort in Graphene research

How many Layers? Raman, LEEM, Ellipsometry



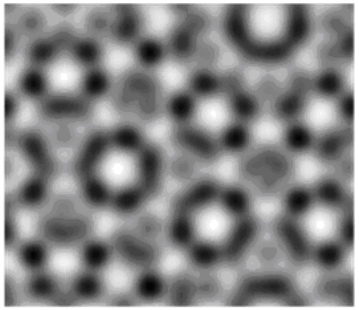




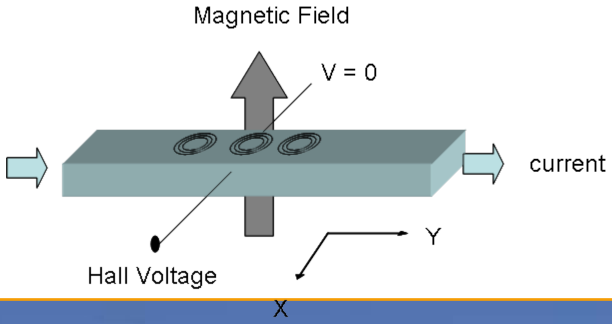
Measurement of Bi-layer

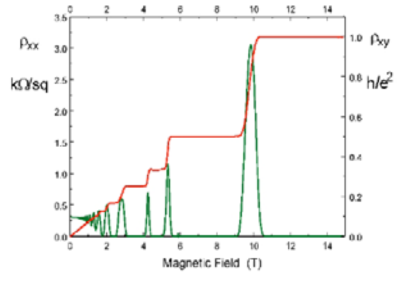
Mis-orientation

Aberration corrected TEM

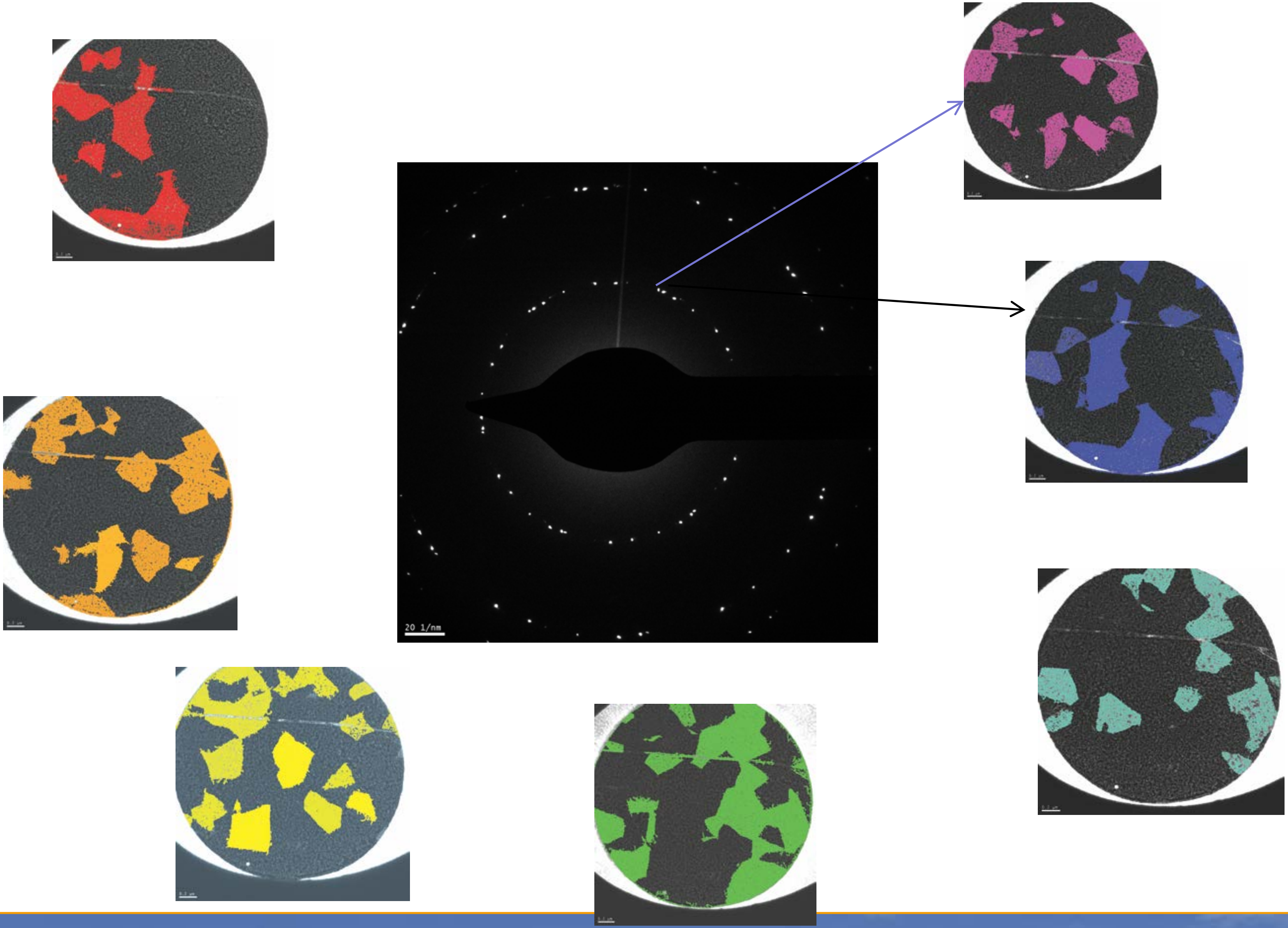


Quantum Hall Effect observes the Berry Phase





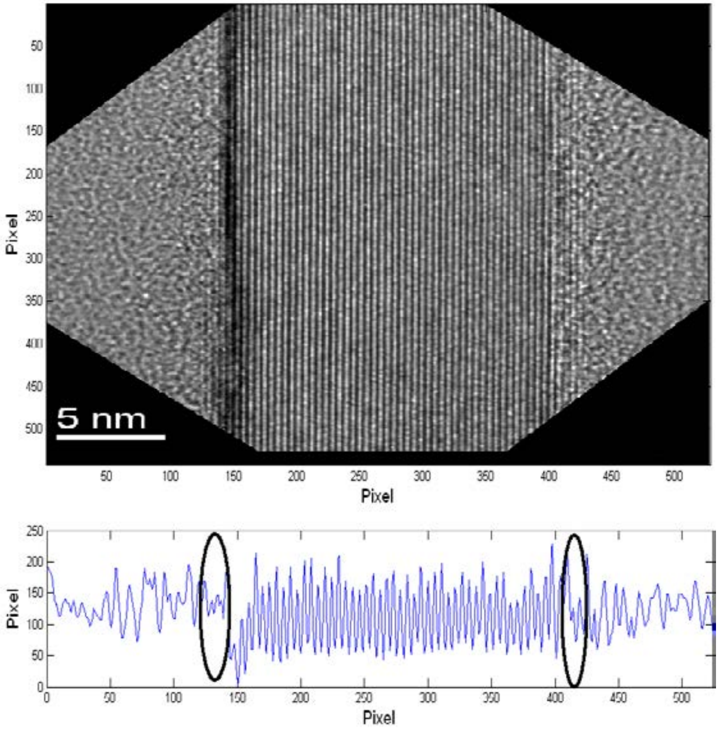
DF TEM of CVD Graphene



Method described in Muller groups 2011 Nature pub

Counting Atoms- the Ultimate Standard

Counting Atomic Columns in a FiN



NIST Traceable Standard
Ron Dixon – NIST
George Orji - NIST
Ben Bunday - SEMATECH

Beyond CMOS Materials Graphene

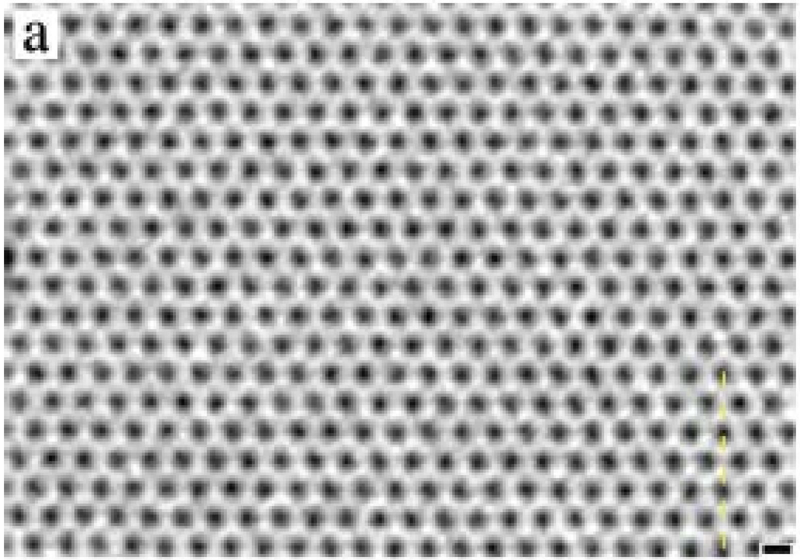
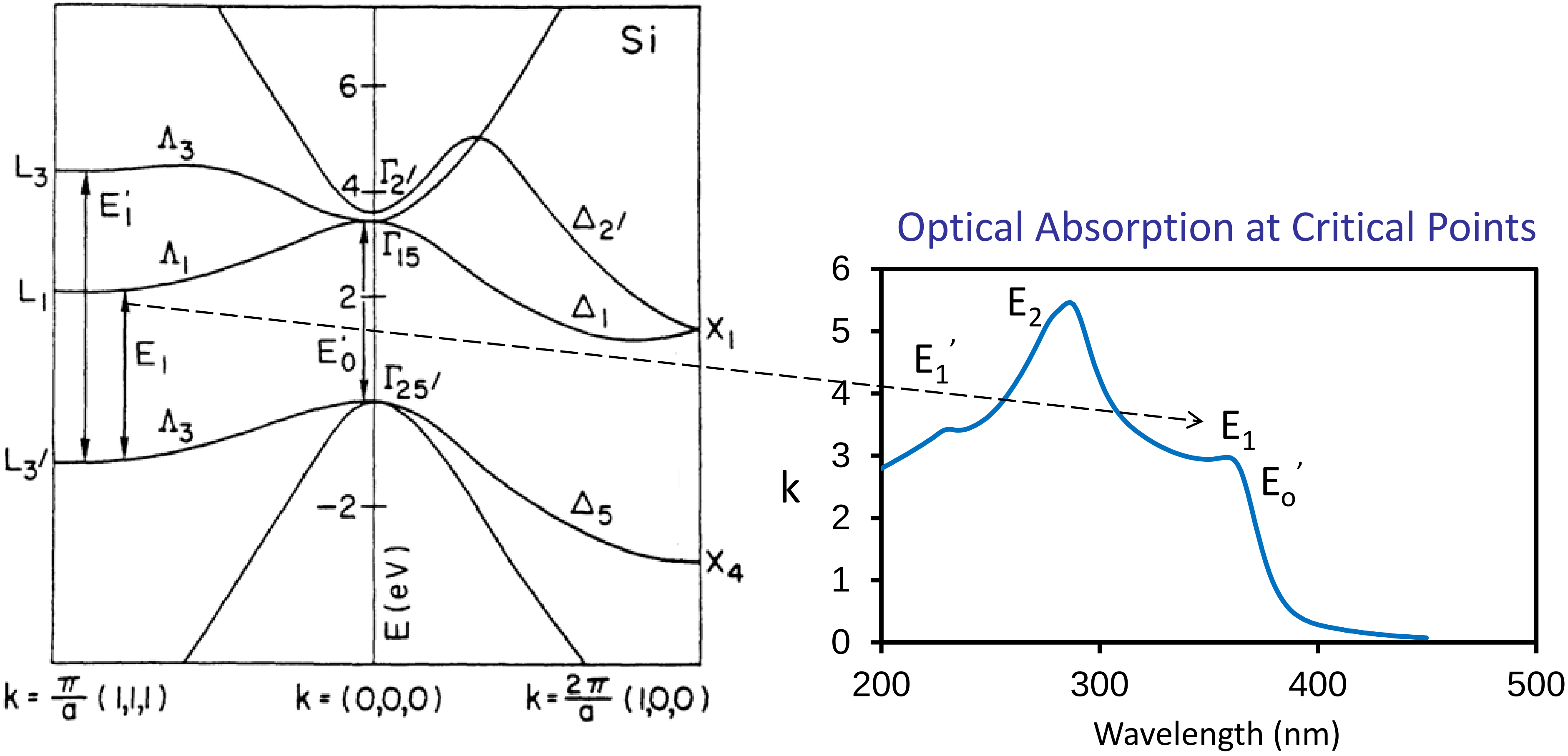


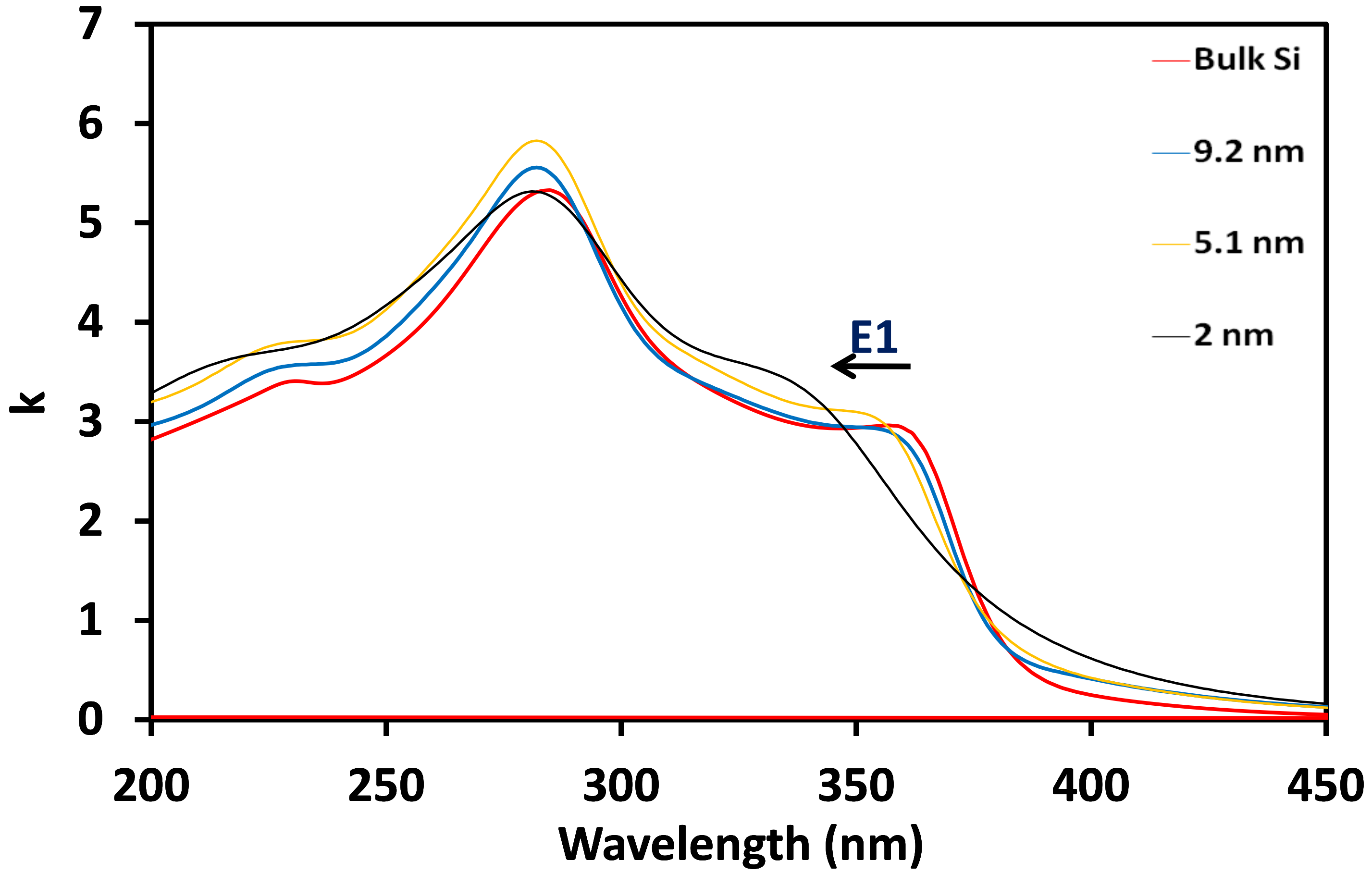
Figure Courtesy
C. Kisielowski - Nano Lett.8, (2008), 3582–3586

Optical Absorption at Critical Points



Ultra-Thin Silicon

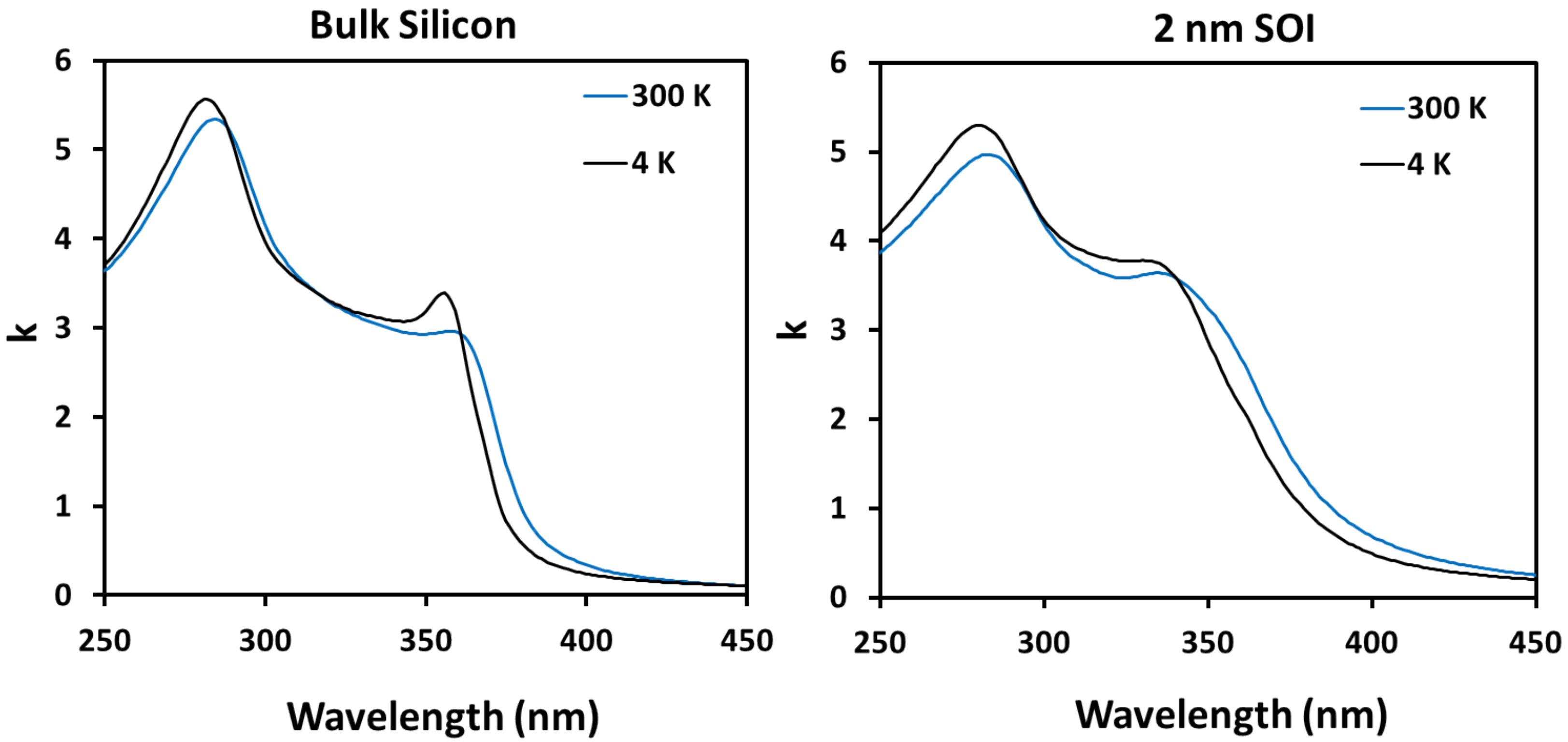
Blue shift for E1 transition – First Explanation was Quantum Confinement.



Nano-Dimensional Optical Properties

Ultra-Thin Silicon

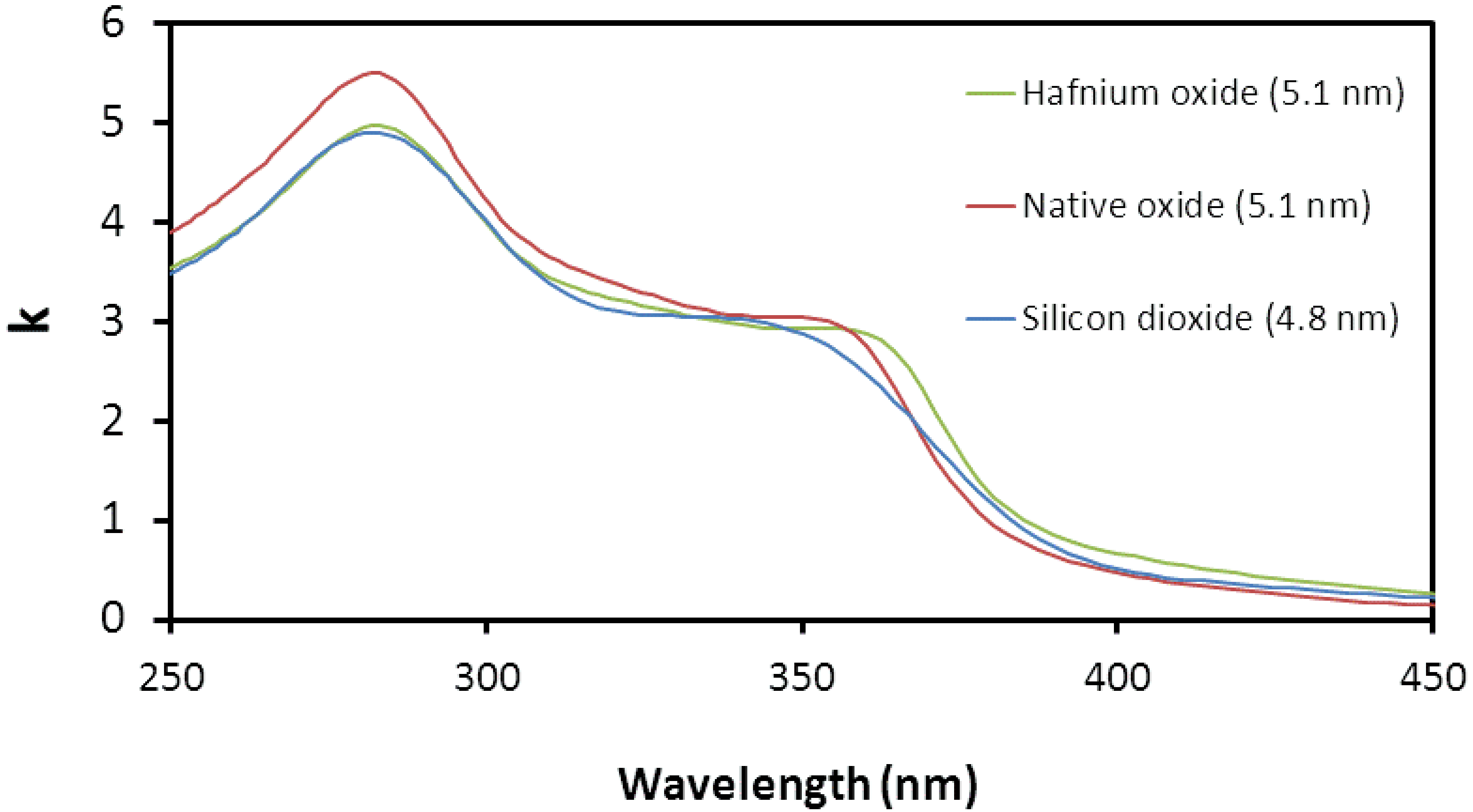
Blue shift for E1 transition. – Phonon confinement Plays a Role



Low Temperature Data shows that electron-phonon scattering strongly influences optical properties

Electron and phonon confinement change optical properties

5 nm SOI with different top dielectric layers



5 nm SOI with different top dielectric layers

Acoustic and optical phonon modes have a strong effect on
E1 Critical Point energy and broadening of E1
i.e. the refractive index

Our Modeling of acoustic phonon modes show that they change with film thickness and presence of a dielectric layer above the SOI

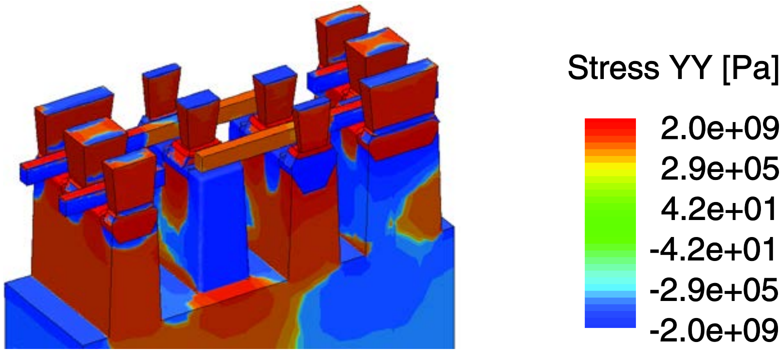
This implies that optical properties of Nanoscale Semiconductors depend on Materials and Structure

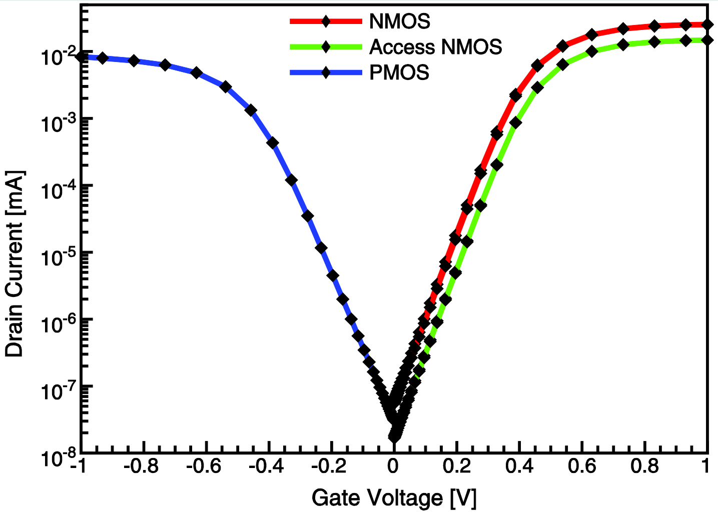
Modeling, Simulation, and Metrology

Metrology needs to measure the distribution of a property that is changing at Nano-Scale Dimensions across a large area such as stress across an SRAM Cell

We need more than CD to control Electrical Properties

Final Stress in SRAM Cell





"Sentaurus TCAD simulations from Synopsys – TCAD News Dec 2010"

Conclusions

- Changes in Metrology Requirements often outpace R&D of new methods
- Old methods often find new life : Measurements Require Nanoscale Materials Properties
- New Materials & Beyond CMOS drive most R&D

Acknowledgements

- ITRS Metrology TWG
- My research group - Vimal Kamineni, Florence Nelson, Josh LaRose, Lay Wai Kong, Ilyssa Wells, Eric Bersch and Tianhao Zhang
- Theme VI team
  - Ray Ashouri, Karl Berggren, Robert Geer, Julia Greer, Tony Heinz, Robert Hull, Philip Kim, Charlie Marcus
- NRI – NERC – INDEX Funding

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