

micro and nanoelectronics  
microsystem  
ambient intelligence  
image chain  
biology and health



2007

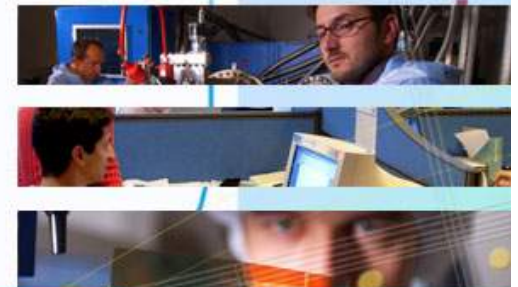
# CEA-LETI as a European model of cooperation in nanoelectronics

M. Brillouët

cea

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# Outline

## → A changing R&D landscape in nanoelectronics

- The European models, incl. CEA-LETI
- Characterization in nanoelectronics
- Conclusion



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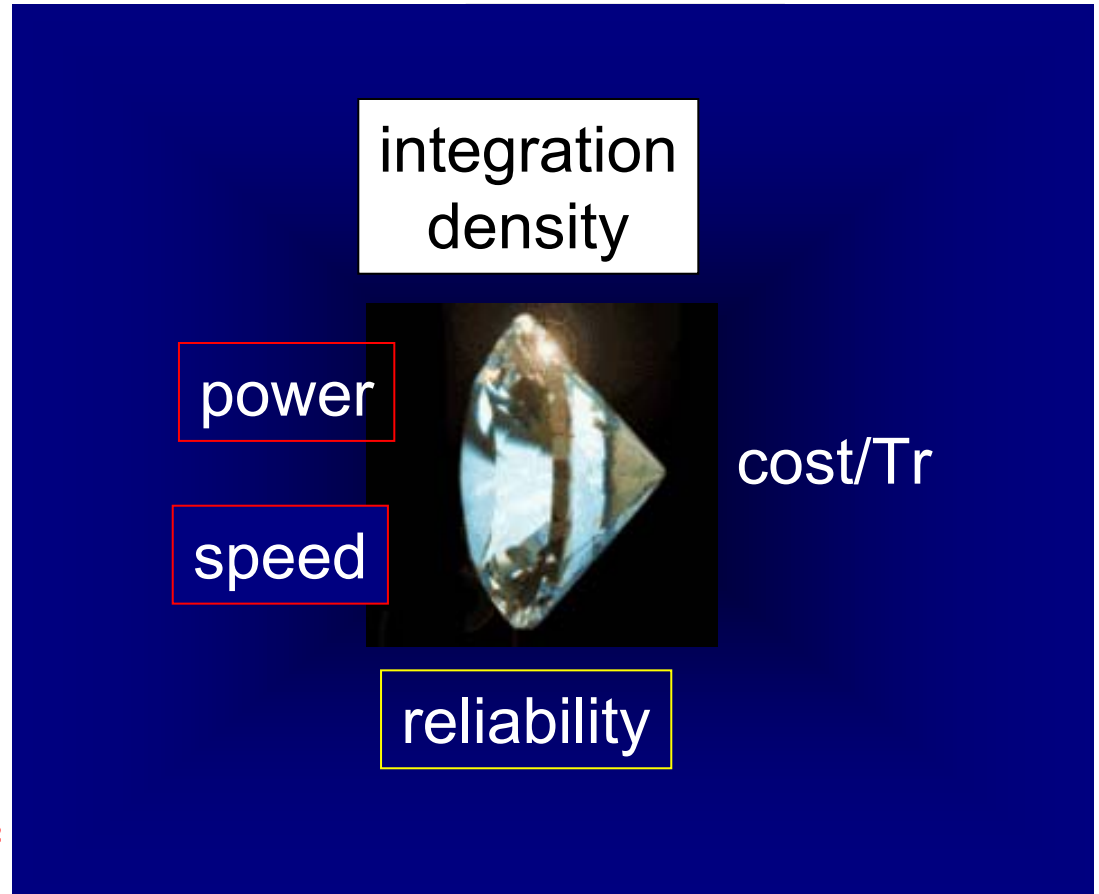
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R. Dennard © IEEE

dimensions $t_{ox}$ , L, W	$1/\alpha$
doping	$\alpha$
voltage	$1/\alpha$
integration density	$\alpha^2$
delay	$1/\alpha$
power dissipation/Tr	$1/\alpha^2$

# The happy scaling



*Smaller = better: for how long?*





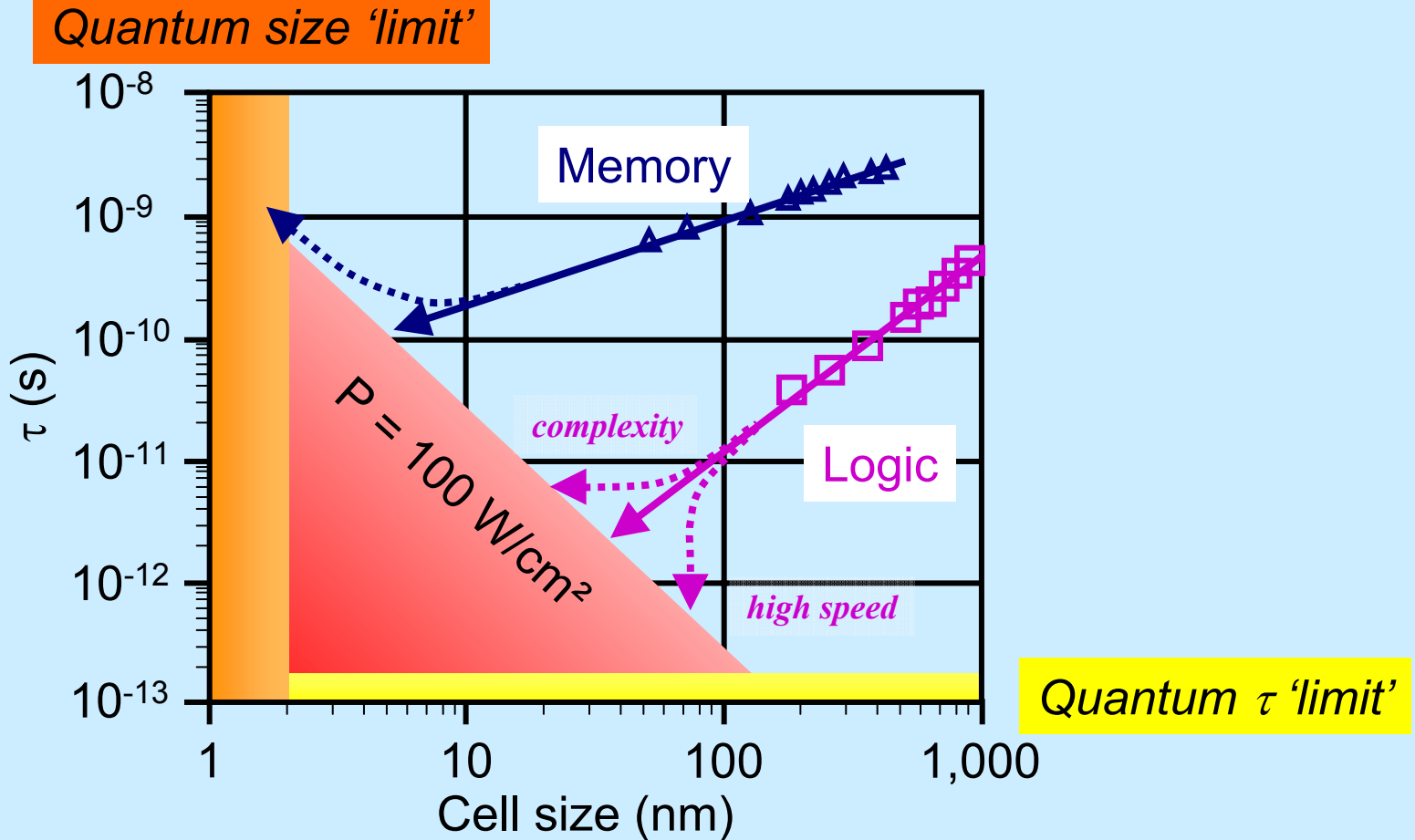
# No hard physical limits, but...



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after Zhyrnov

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# R&D spending: a gathering storm



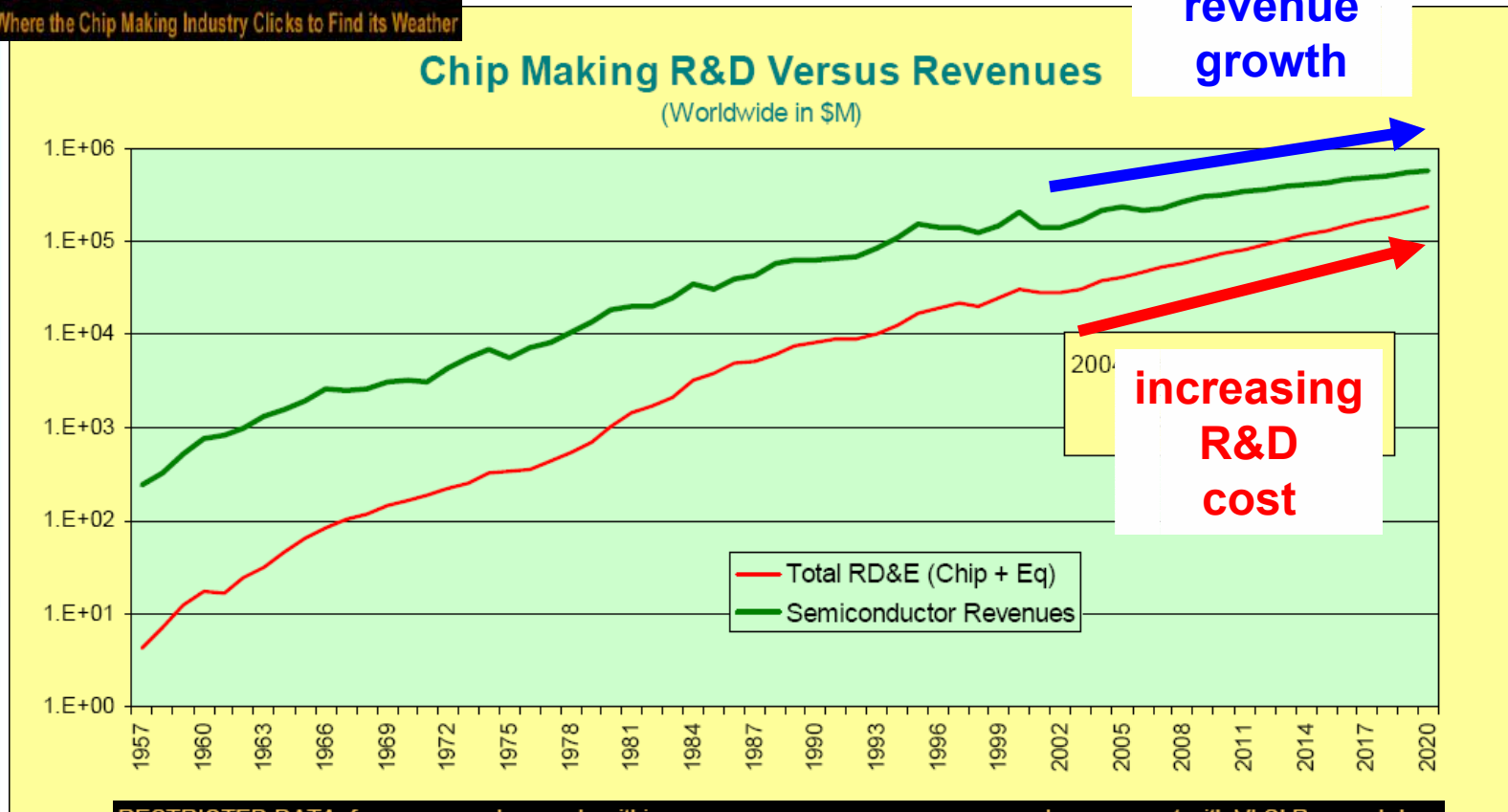
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**VLSI RESEARCH INC**  
Where the Chip Making Industry Clicks to Find its Weather

**Chip Making R&D Versus Revenues**  
(Worldwide in \$M)



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# The January 2007 PR 'tsunami'



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**NXP**  
founded by Philips



## EETIMES

### NXP to exit Crolles2 Alliance

(01/16/2007 2:55 AM EST)

SAN JOSE, Calif. — NXP Semiconductors on Tuesday (Jan. 16) said that it shall not extend its current cooperation in the Crolles2 Alliance beyond the initial term expiring at the end of 2007. NXP (Eindhoven, the Netherlands), formerly Philips Semiconductors, has decided to pursue a different path for its future development of process technology. It will work with long-time foundry partner Taiwan Semiconductor Manufacturing Co. Ltd. (TSMC). [...]

"We've chosen to strengthen our cooperation **with TSMC, in the area of advanced CMOS development,**" stated Frans van Houten, NXP president and CEO, in a statement. "This move will enable NXP to **concentrate more on creating innovative, differentiating process options,** such as embedded non-volatile technology in 45nm for our state of the art system-on-chip products, while building on the process platform from TSMC."

The strengthened global R&D cooperation will be built upon the existing NXP Research organization **at the IMEC facilities in Leuven, Belgium,** and **TSMC corporate R&D in Hsinchu, Taiwan.** TSMC (Hsinchu) is also a core member of IMEC.



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# The January 2007 PR 'tsunami'



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**NXP**  
founded by Philips

Launched by Motorola  
**freescale**  
semiconductor



## EETIMES

### Freescle joins IBM's 'fab club'

(01/23/2007 12:01 AM EST)

SAN JOSE, Calif. — In a major change of direction, Freescale Semiconductor Inc. on Tuesday (Jan. 23) announced plans that it will join IBM Corp.'s "fab club" for joint semiconductor research and development.

The move appears to be perhaps another nail in the coffin for the troubled Crolles2 Alliance, which is on shaky ground right now. It also raises questions about Freescale's deals with its current silicon foundry partners, such as Taiwan Semiconductor Manufacturing Co. Ltd. (TSMC) and United Microelectronics Corp. (UMC).

Under its new R&D strategy, **Freescale (Austin, Texas) will become a partner in IBM's technology alliance starting at the 45-nm node.** Freescale will also participate in the R&D alliance **at the 32- and 22-nm nodes and beyond.**

The agreement includes the development of CMOS and silicon-on-insulator (SOI) technologies. [...]

The IBM alliance provides "levels of investment significantly higher than what we could have accomplished at Crolles2." [...]

Sadana did not elaborate on Freescale's manufacturing strategy, which is characterized as a so-called **"fab-lite" model.**

He insisted that Freescale will **continue to work with TSMC and UMC despite joining the IBM "fab club."**

At present, Freescale outsources about 20-to-25 percent of its chip production to the foundries, namely TSMC and UMC.

The rest is produced in-house within its various fabs.

But at the 45-nm node and beyond, however, it is widely believed that Freescale will have most of its chips made at the foundries within the IBM "fab club."



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# The January 2007 PR 'tsunami'



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## EETIMES

### Texas Instruments exits process development race

(01/24/2007 5:27 AM EST)

LONDON — Texas Instruments Inc., one of the largest and most successful integrated device manufacturers, has **decided to drop the costly business of digital logic process development and rely on foundry partners** for its processes.

According to reports TI (Dallas, Texas) development has decided to stop internal development at the 45-nanometer node and use foundry supplied processes at 32-nm, 22-nm and thereafter.[...]

TI (Dallas, Texas) made the announcement that it would exit digital CMOS process development [...and] the company would close its Kilby wafer fab in Dallas. [...]

"One way we'll do this is by changing the way we develop advanced digital process technology.

Instead of separately creating our own core technology, we will work collaboratively with our foundry partners to specify and drive the next generations of digital process technology[...]" said Rich Templeton [...].

TI has long used foundries, such as Taiwan Semiconductor Manufacturing Co. Ltd., United Microelectronics Corp. and Semiconductor Manufacturing International Corp.[...].

**It seems unlikely that TI would ever construct a leading-edge wafer fab again** and is set to let its own manufacturing of advanced digital CMOS wither on the vine.



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# The January 2007 PR 'tsunami'



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## EETIMES

### ST decides to import CMOS, change Crolles function

(01/25/2007 9:15 AM EST)

LONDON — Carlo Bozotti, chief executive officer of STMicroelectronics NV, told analysts Wednesday (Jan. 24) that ST would align with "industry leaders" to obtain a 32-nm CMOS process for use in its wafer fabs and as a platform for specialized extensions.

Bozotti did not say who would provide ST with its 32-nm CMOS platform but said: "It is obvious we have alternatives." [...]

Speaking during a conference call for analysts Bozotti said that the Crolles2 Alliance would complete the development of 45-nm CMOS process technology during 2007 but there would then be a "discontinuation" in the role of the Crolles development center and pilot fab.

Bozotti said that because of the increased cost of developing 32-nm CMOS manufacturing process technology it had been **decided to import advanced CMOS** and that ST would then **use the Crolles research facility to develop derivative** proprietary technologies that would be important to its wireless business unit. Bozotti listed image sensor, radio frequency and analog extensions to basic CMOS as the technologies that would be developed at Crolles. [...]

"It is a clear change in strategy...but Crolles will remain the key center for advance technology development while on the CMOS bulk we will align with industry leaders and make sure this technology is available in our facilities," Bozotti said.



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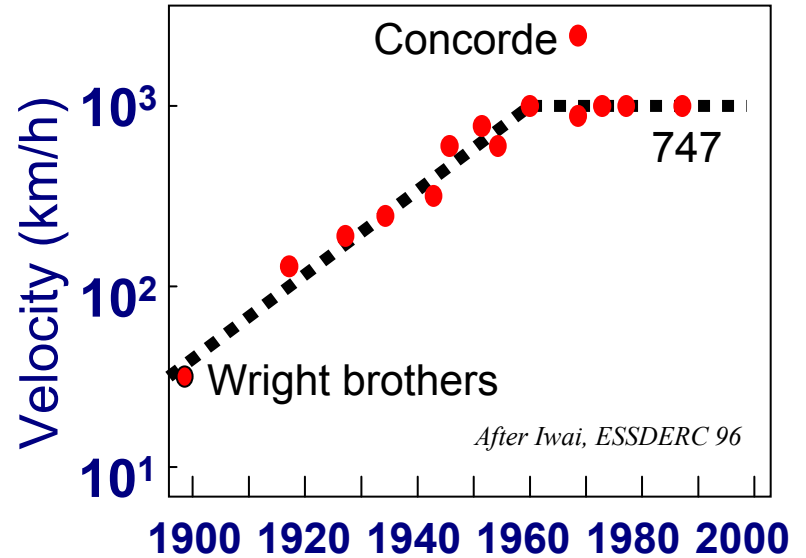
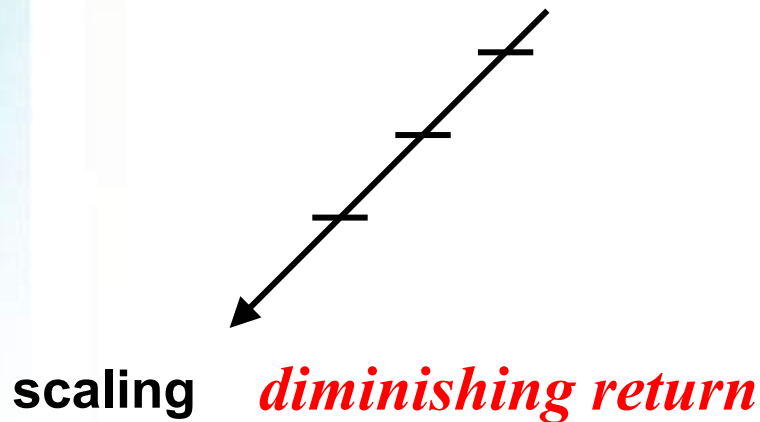


# Moving away from pure scaling...

Si CMOS-based logic

- + new materials
- + new device architectures

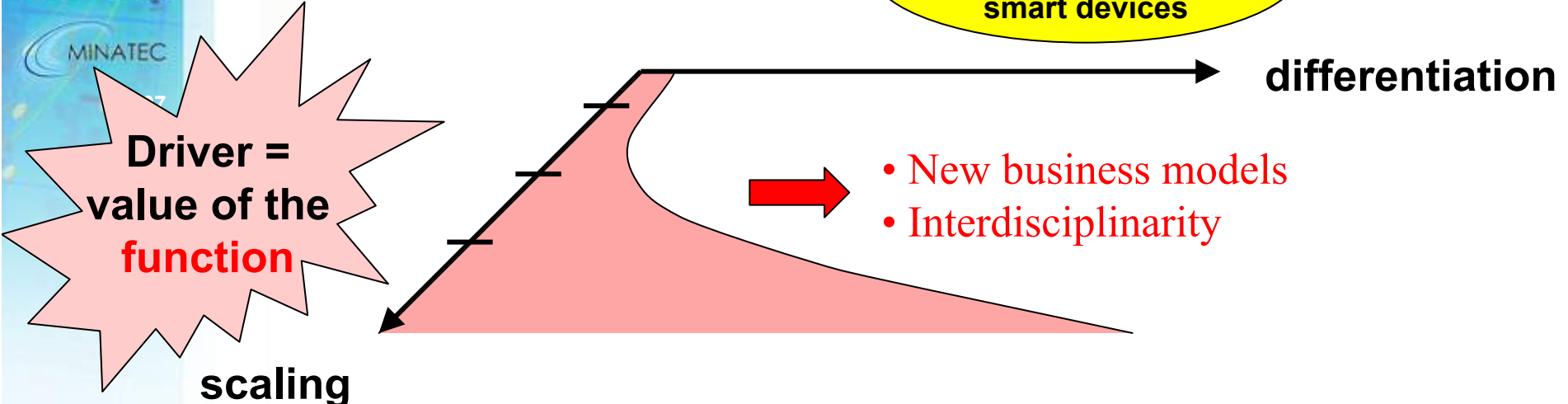
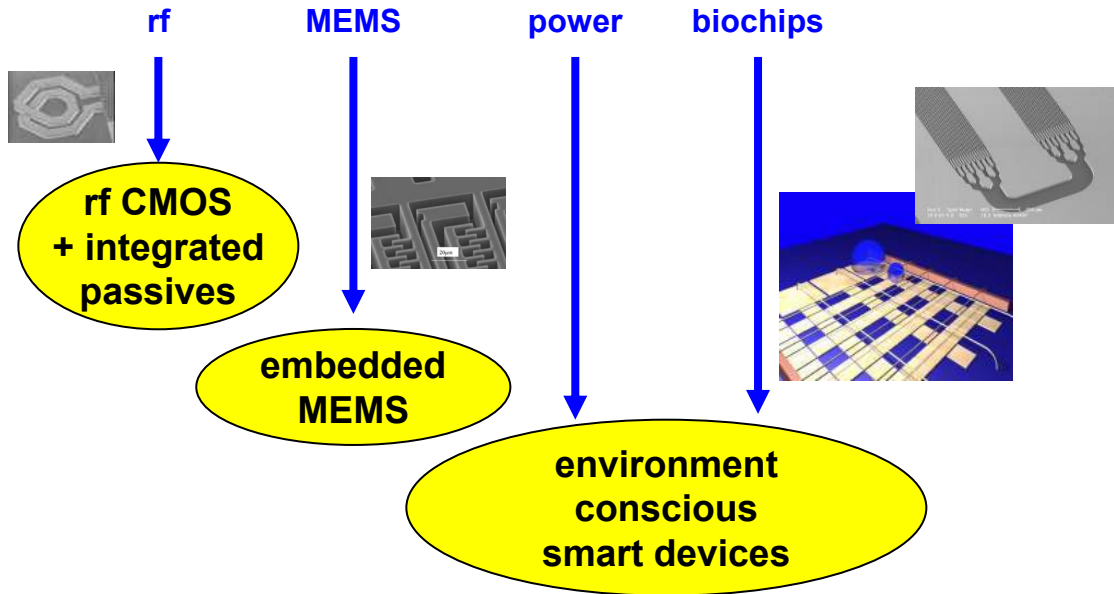
**Driver =  
cost +  
performance  
/gate**



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...through differentiating technologies...



*“the emergence of many new ideas and technologies, several of which are suitable for only certain function(s) and do not have broad application, may be signaling a coming dispersion of microelectronics technologies to address an increasingly diverse set of market-driven applications” [ITRS03, ERD]*





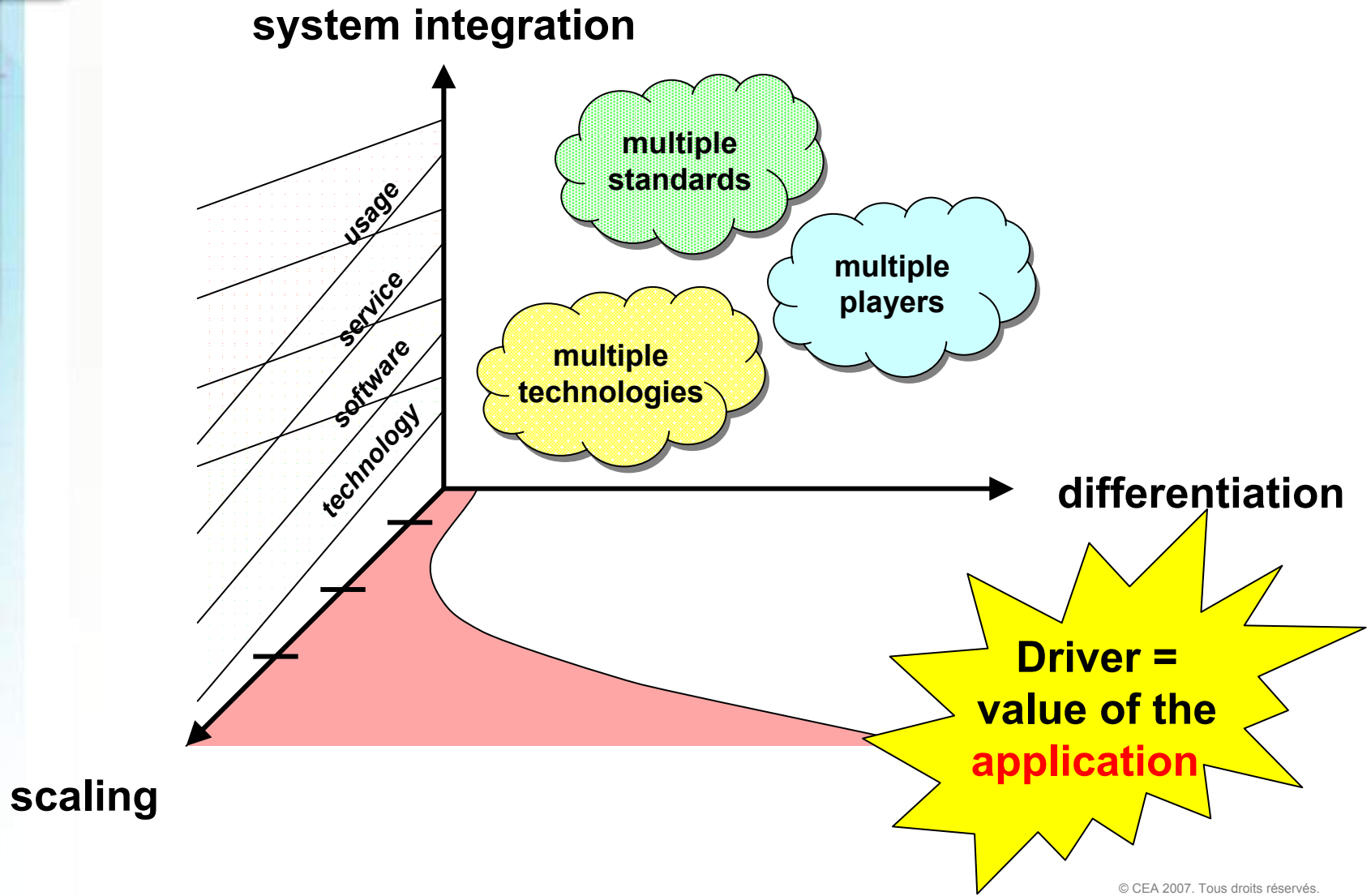
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...towards mastering the system complexity



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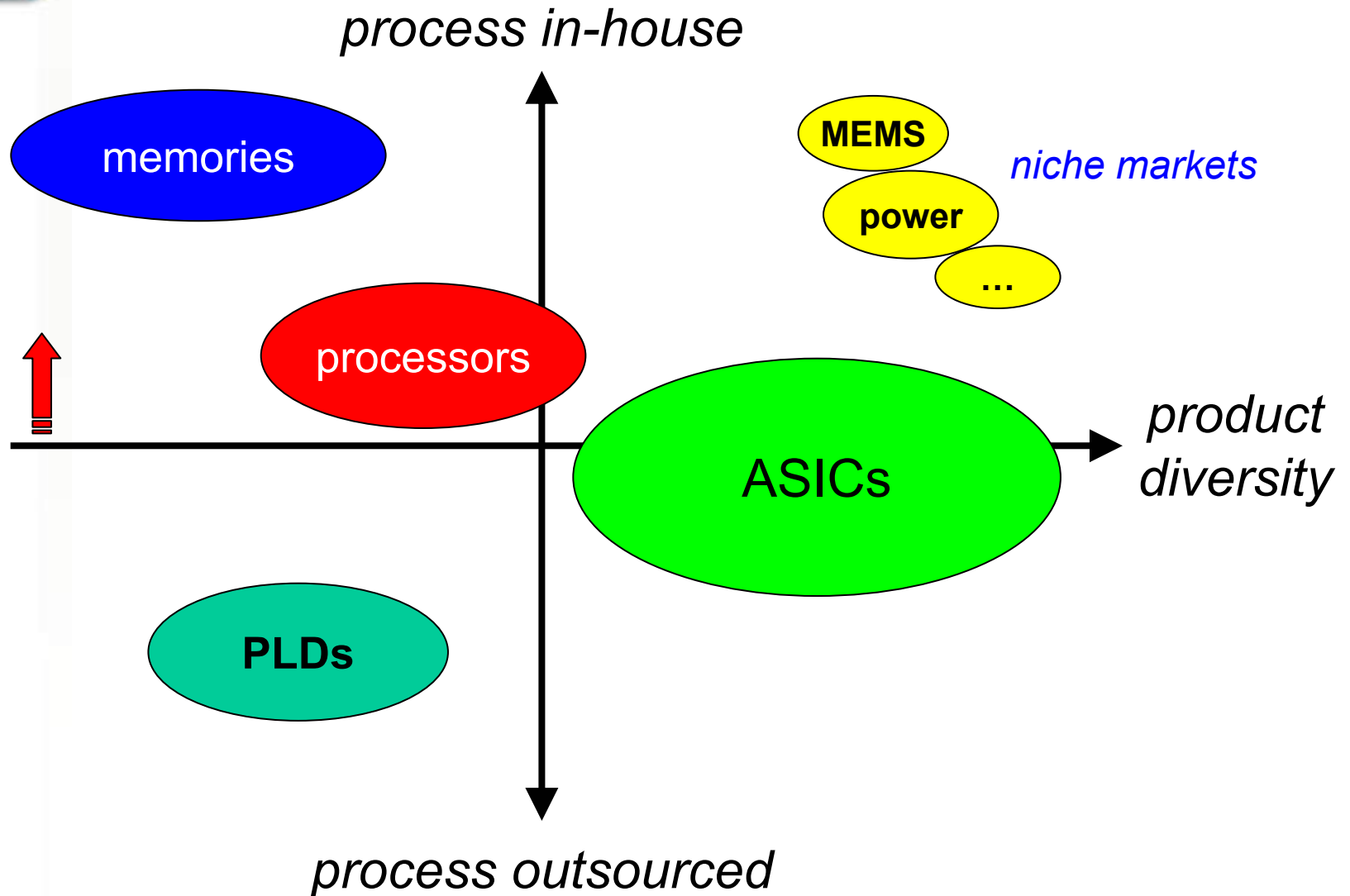
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# The IC technology landscape



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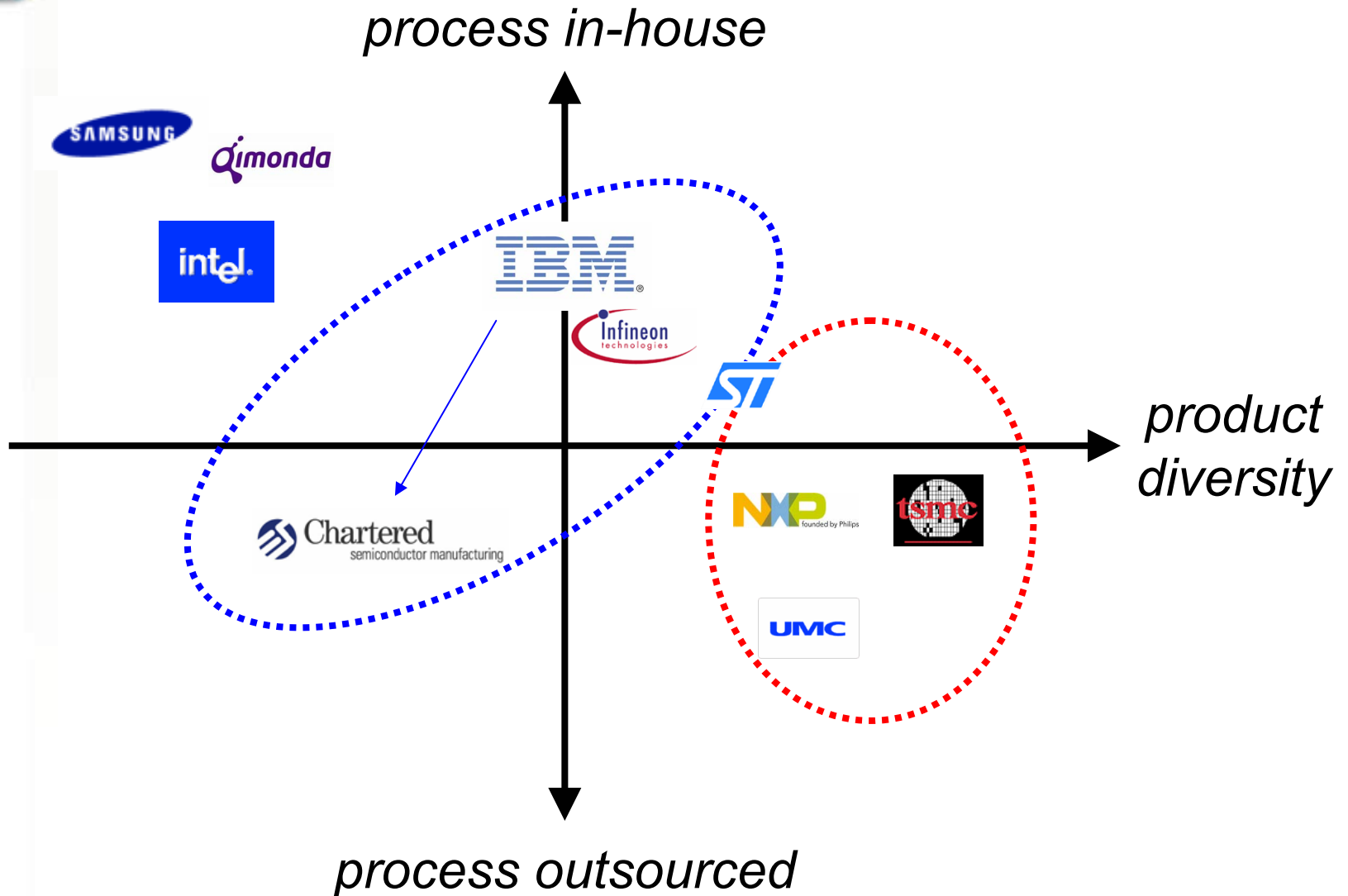


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# Where are the European companies?



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# Outline

- A changing R&D landscape in nanoelectronics
  - ➔ The European models, incl. CEA-LETI
- Characterization in nanoelectronics
- Conclusion



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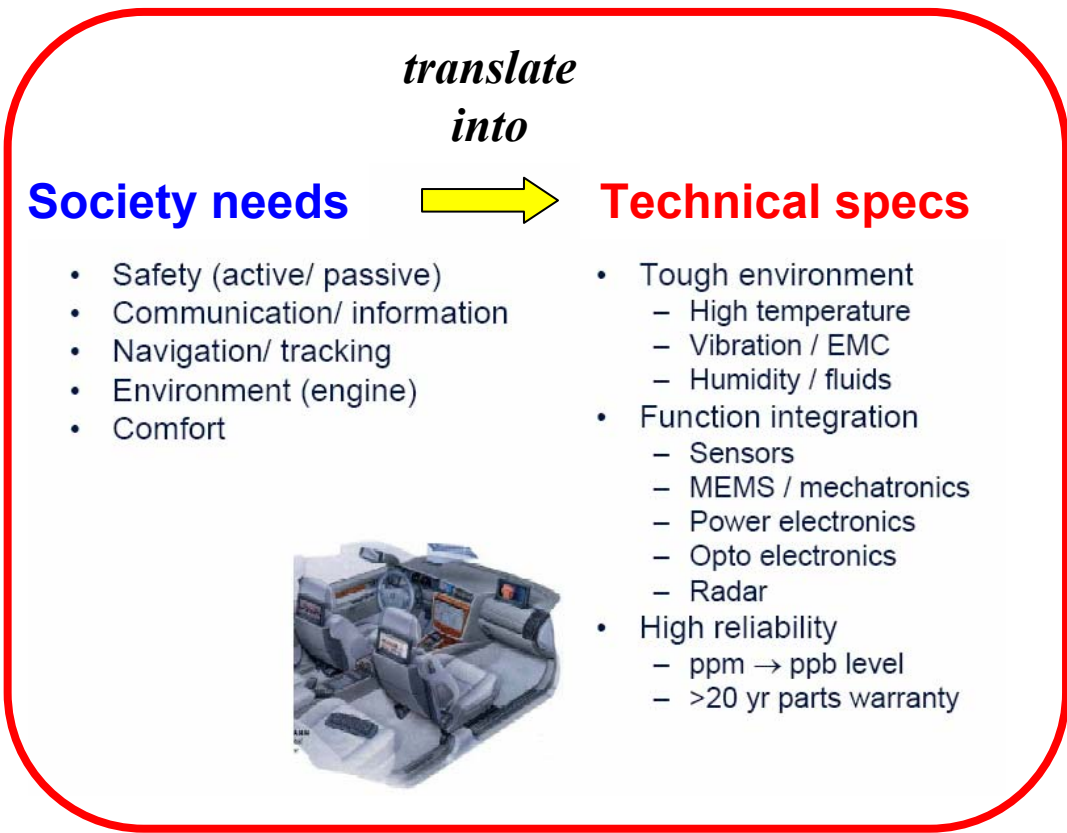




# An European way of thinking: application driven enabling technologies



- Health
- Mobility / Transport
- Security / Safety
- Communication
- Education / Entertainment
- Energy / Environment



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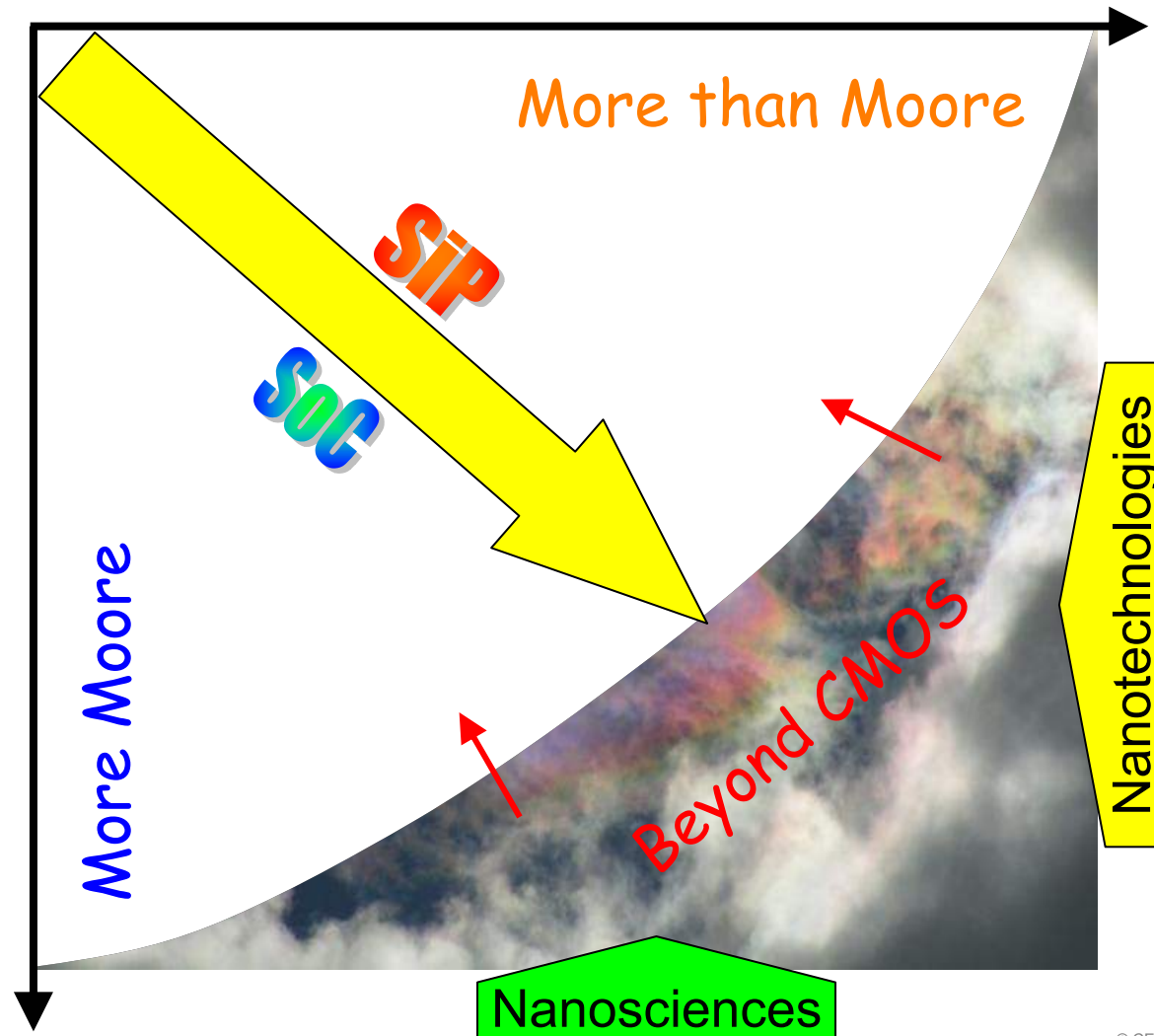


from  Strategic Research Agenda

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# A full coverage of the nanoelectronics themes



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# 300mm R&D ecosystems



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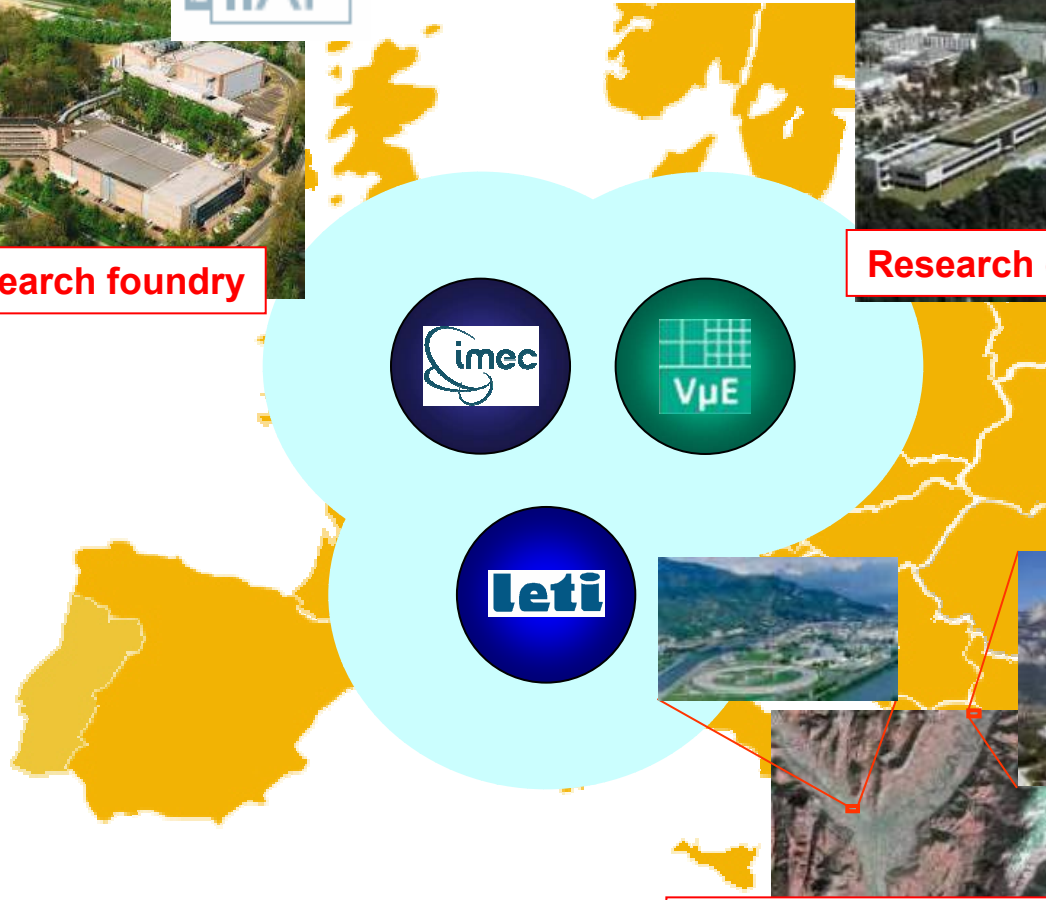
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Research foundry



Research docking in manufacturing



Collaborative proximity with Manufacturing & Academia



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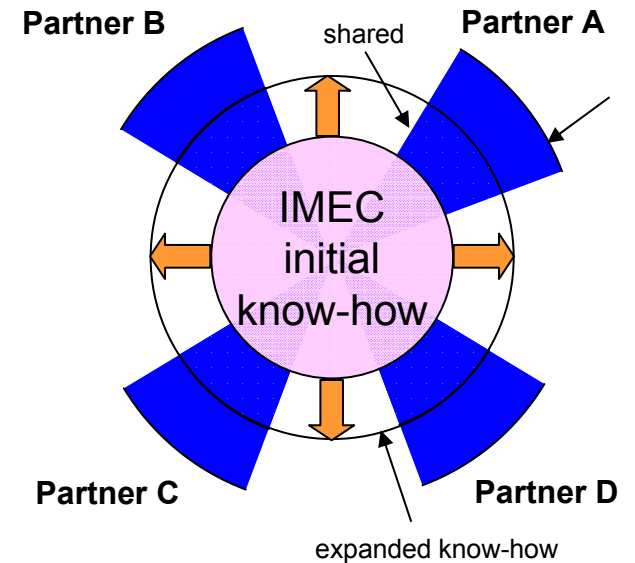


# imec : an open international model



<b>Lithography</b> (incl. DRAM eval.)  <b>Hyper NA Immersion</b>  <b>EUVL</b>	<b>Front End</b> (incl. DRAM eval.)  <b>PLANAR</b> <b>EMERALD</b>  <b>GATE STACK</b>		<b>Back End</b> (incl. DRAM eval.)  <b>Cu/Low k</b>  <b>3D-SiC</b>	<b>Flash Memory</b>  <b>Floating Gate</b>  <b>Charge trapping</b>  <b>Flash Scaling</b>
<b>Explore</b> Exploratory Materials and Device Research for CMOS based Technologies <b>Ge/III-V, expl. high-k</b> <b>Post-CMOS nano</b>		<b>Cleaning &amp; Contamination (UCP program)</b>	<b>Supporting Expertise Centers</b> <b>Materials Characterization &amp; Metrology</b> <b>Reliability &amp; Modeling</b>	

**Core Program**



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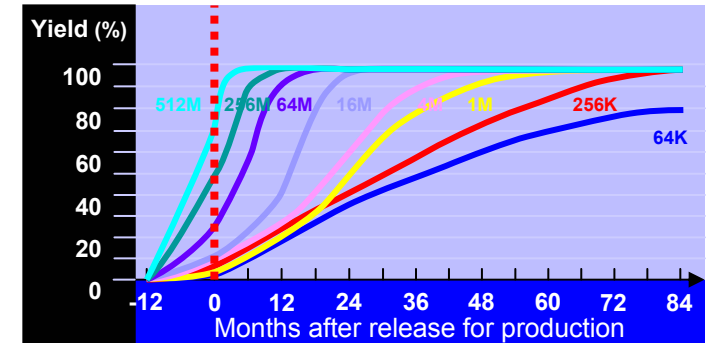
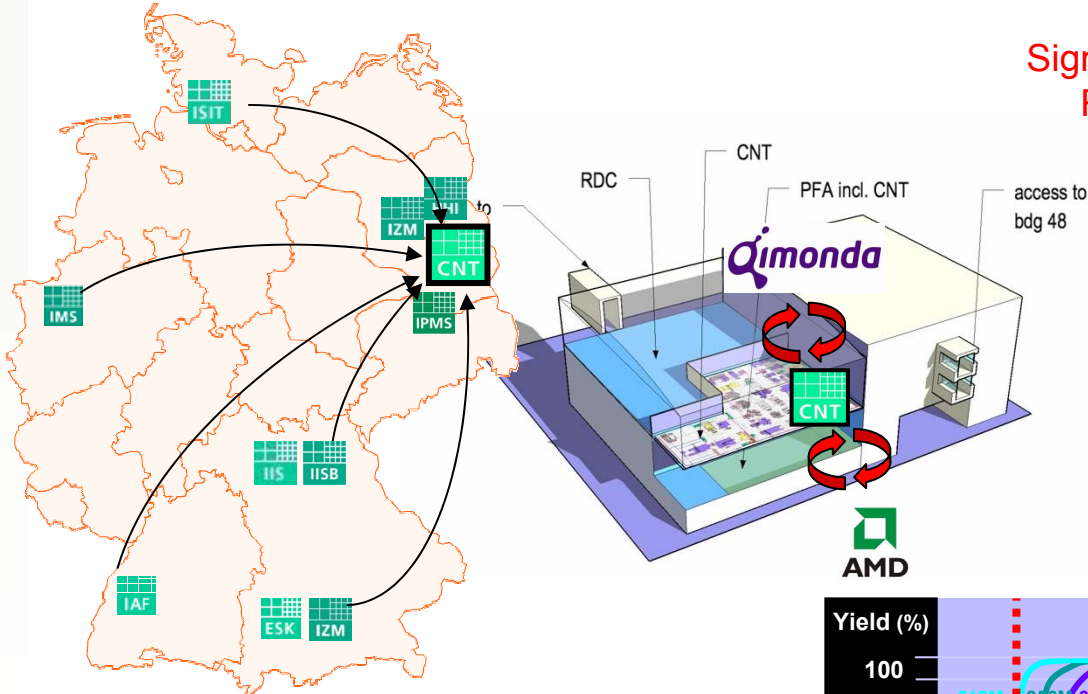

  
**Fraunhofer**
  
 Verbund
   
 Mikroelektronik

# : the CNT model

Research docking...

...in manufacturing

Significant volume of wafers  
 Realistic environment  
 Cost efficiency



Source: VLSI Research

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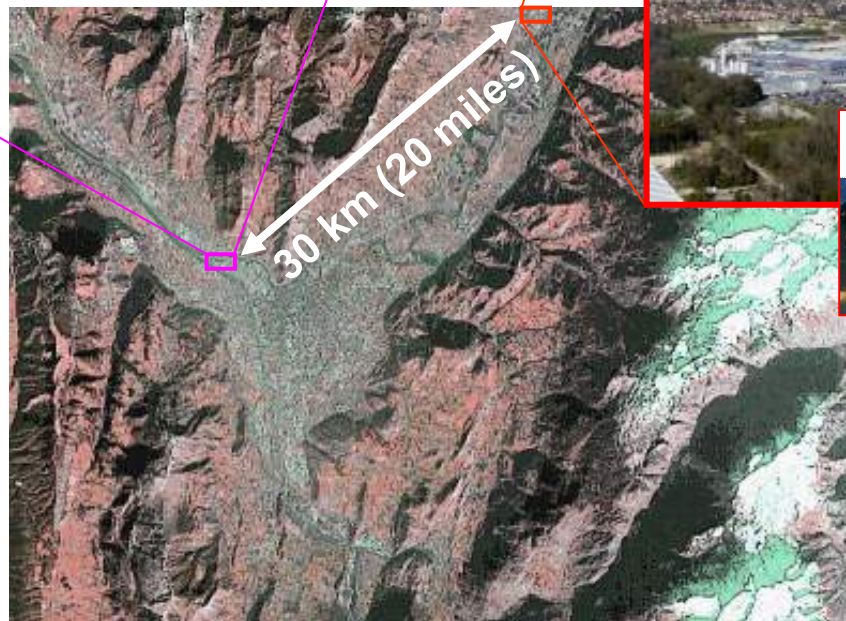
: close collaboration with industry and academia



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A complete set of research platforms

From advanced concepts to pilot lines

Short loops with industrial sites

Cooperative with academia and industry



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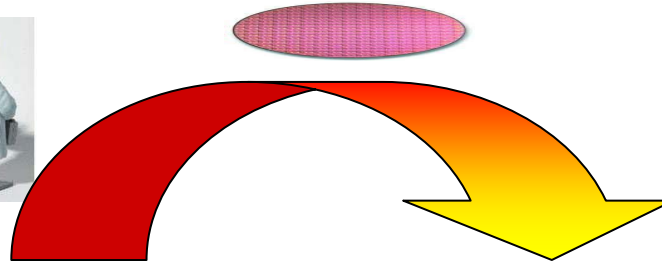
# A close collaboration with industry



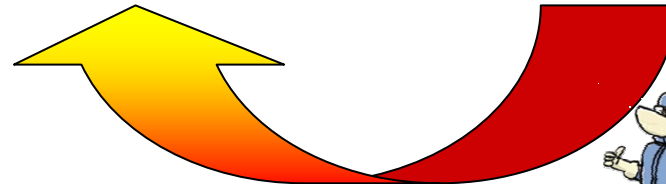
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- people X-assignment
- wafer exchange
- value-added investments



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# Need for a sensitive contamination control



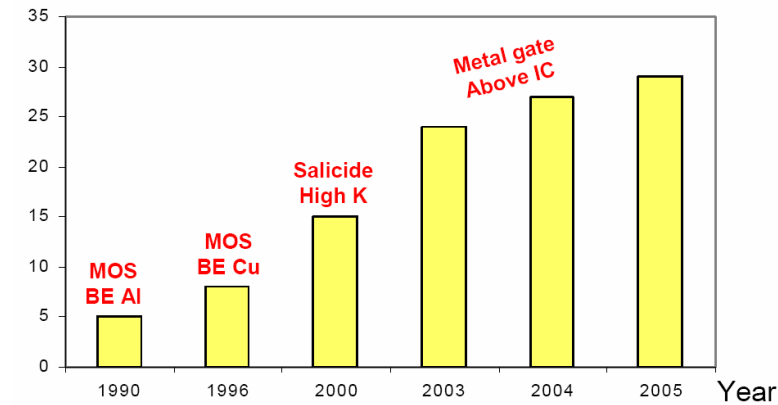
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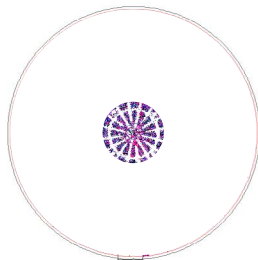


Number of metals

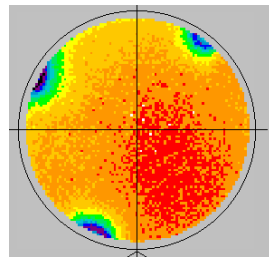


metals

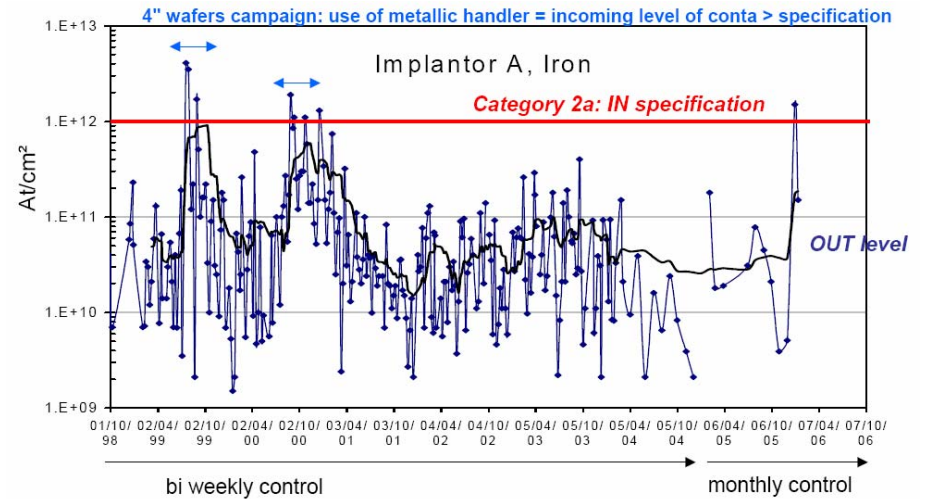
50+ tools  
monthly control



Chuck footprint



Cu from a contaminated quartz boat



from A. Danel - CEA/LETI

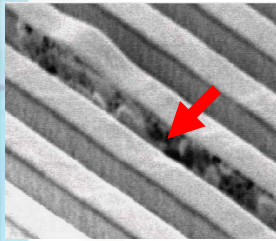
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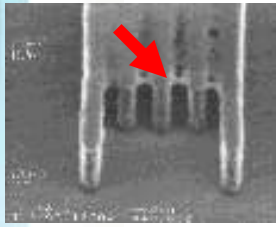


# Need for a sensitive contamination control

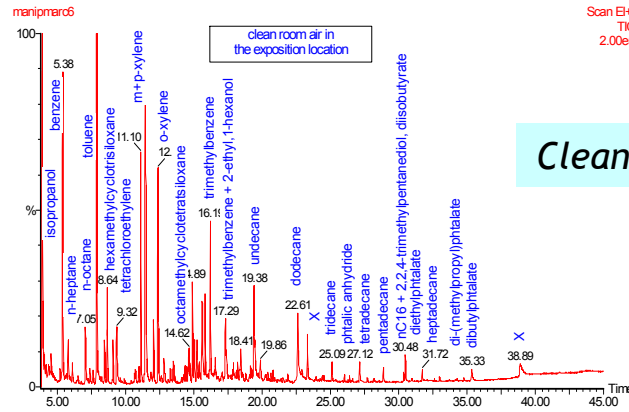
from M. Veillerot – CEA/LETI



Al corrosion

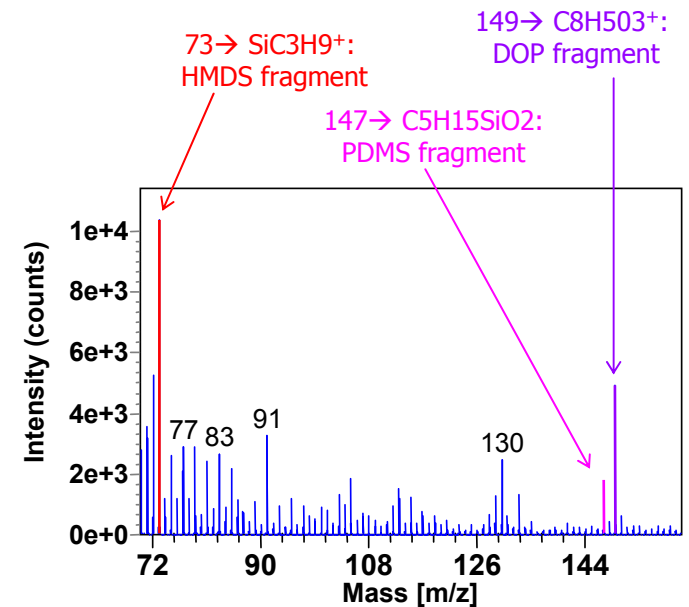


## TD-GC/MS

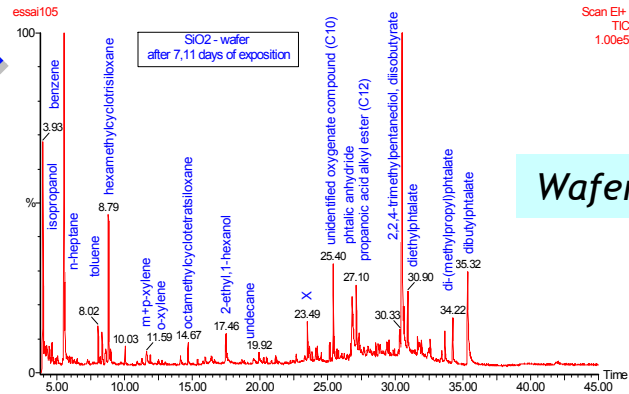


Clean room

## ToF-SIMS



T-top



Wafer

**Organic Contamination**

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# : an campus reinforcing the link with academia



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**Education**  
1500 students

- Attract young people
- New competences

**Research**  
1 200 p.  
on applied research  
500 p.  
on fundamental research

- Pluridisciplinarity
- Speed up innovation



**Pole:**  
Concentration of tools and competencies

**Valorization for Industry**  
1000 partners

- Hosted teams
- Access to facilities
- Start-ups

**MINATEC:**  
Focus:  
Micro and nano-technologies



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# Hosting research teams in a Pilot Line



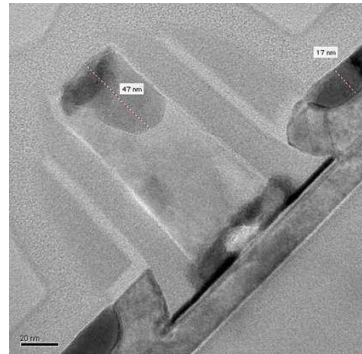
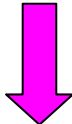
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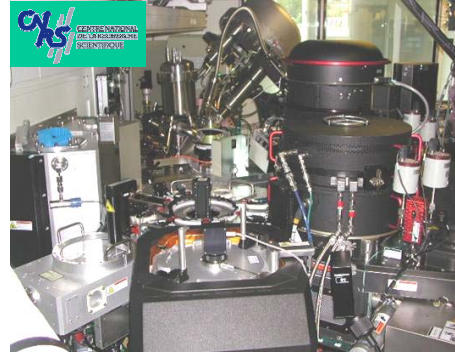


Hosted research team

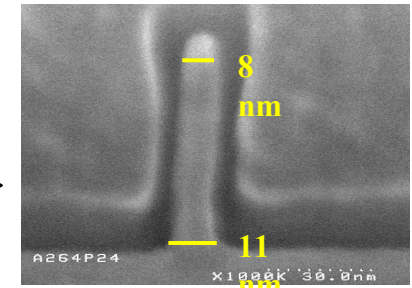
Applied on real problems



FD-SOI + high k/metal gate

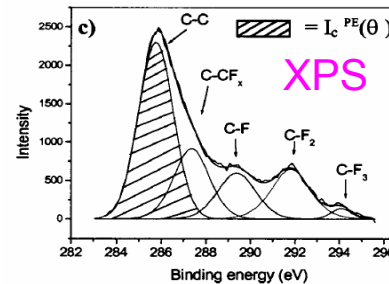


Ultimate  
patterning

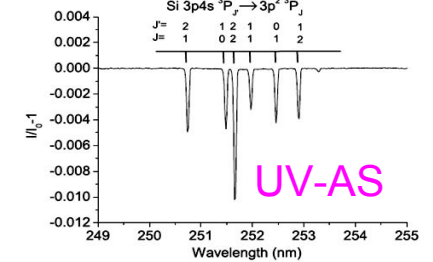


Industrial equipment

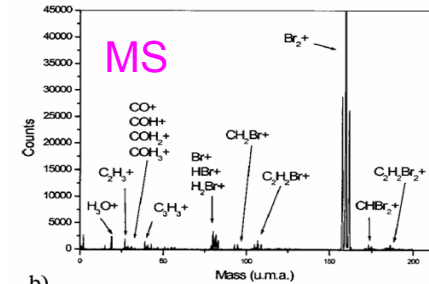
Understanding  
etch mechanisms



E.Pargon et al.  
*J.Vac.Sci.Technol. B22 (4) 1858 (2004)*



M.Kogelschatz et al.  
*J.Phys. D37 (14) 1954 (2004)*



E.Pargon et al.  
*J.Vac.Sci.Technol. B23 (1) 103 (2005)*



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# Outline

- A changing R&D landscape in nanoelectronics
- The European models, incl. CEA-LETI
- **Characterization in nanoelectronics**
- Conclusion



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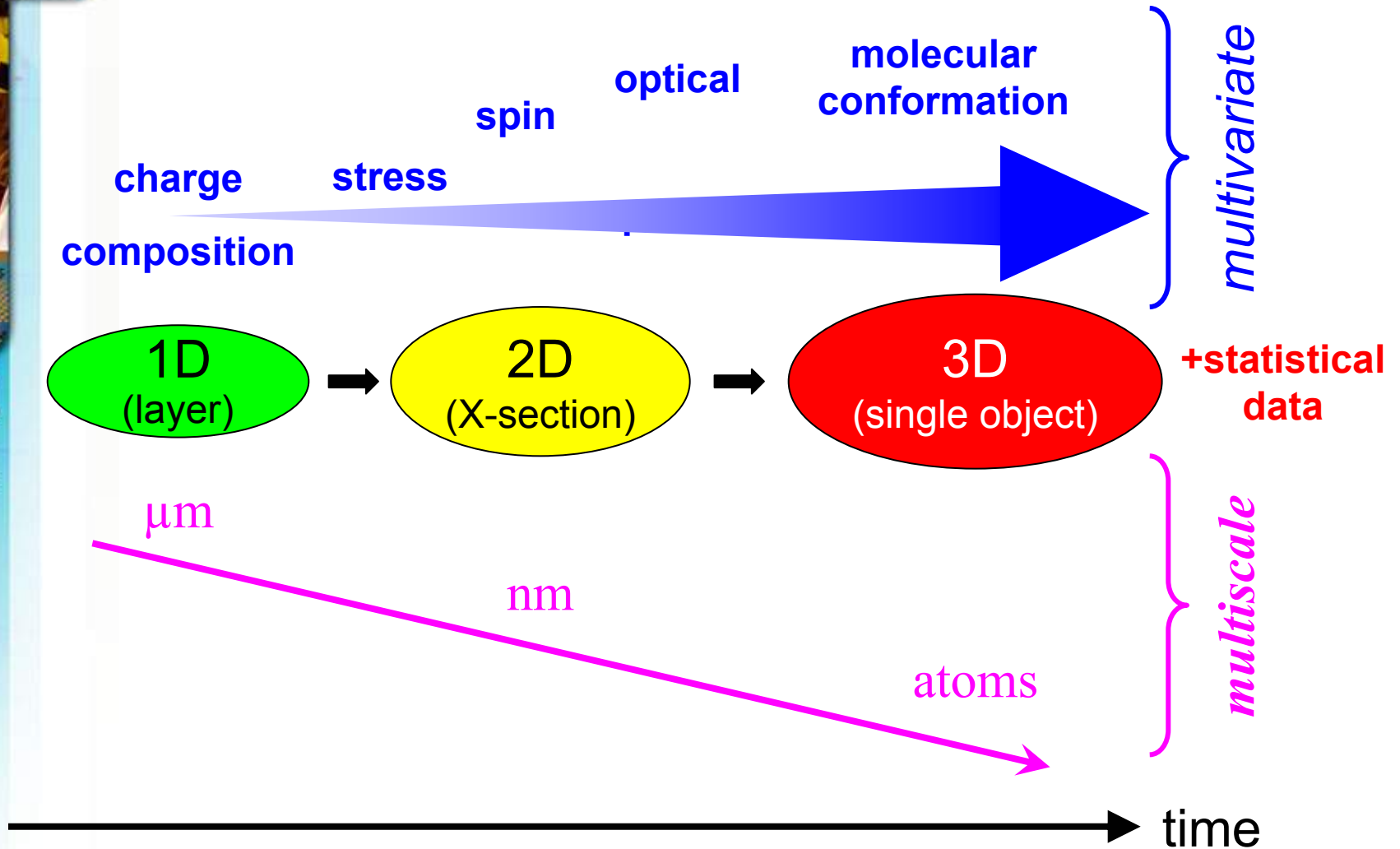
# Trends in nanocharacterization



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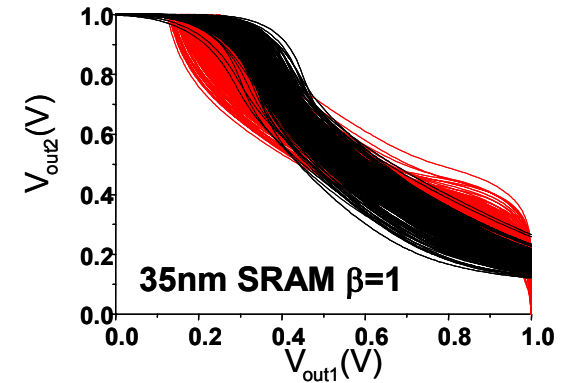
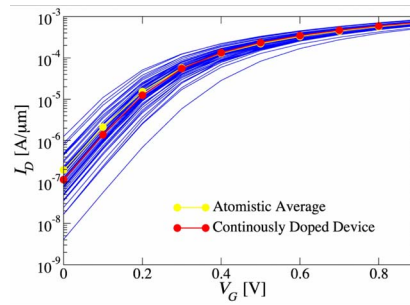
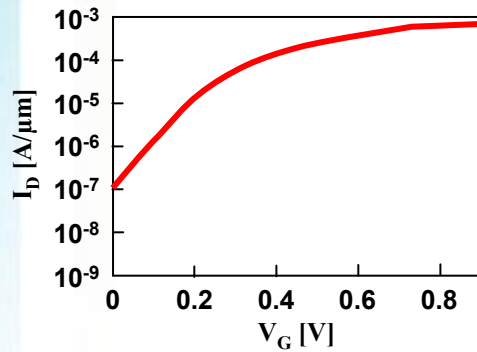
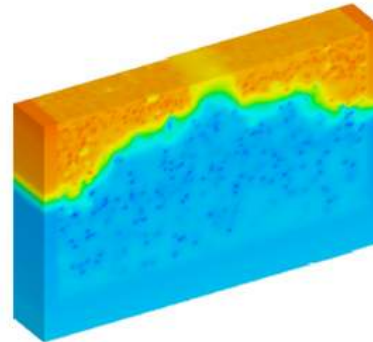
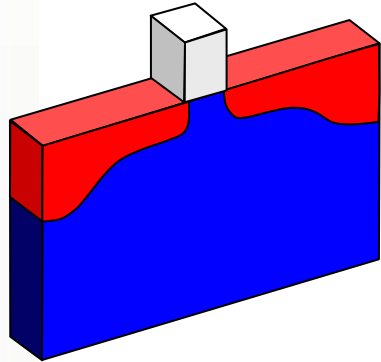
# 3D dopant fluctuation: a major problem



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from Asenov ESSCIRC '04

ideal MOST → actual MOST → unstable SRAM



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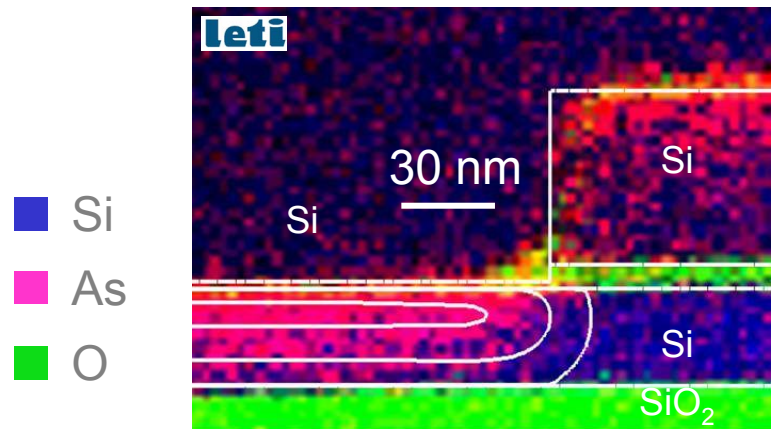


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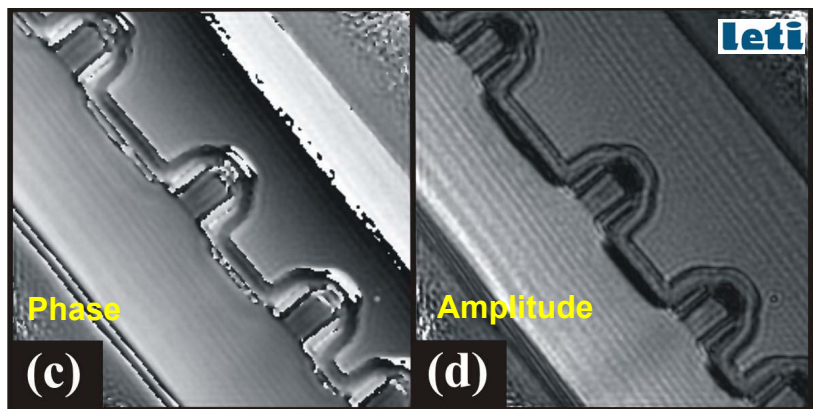


# 3D dopant profile: how to measure it?



Courtesy: JP. Barnes – CEA/LETI

TEM + EDX  
 < 1nm  
 > 10<sup>19</sup> cm<sup>-3</sup>

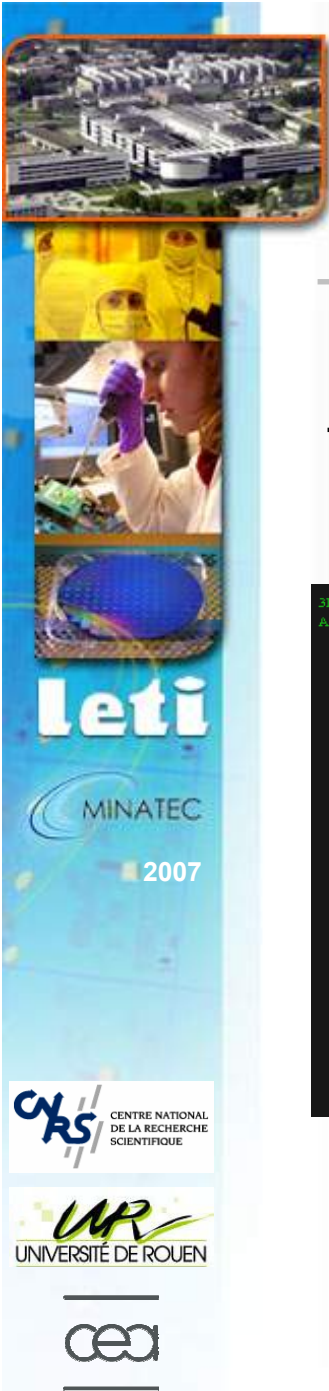


Courtesy: D. Cooper – CEA/LETI

holographic TEM  
 < 1nm  
 10<sup>16</sup> – 10<sup>20</sup> cm<sup>-3</sup>

# still mostly 2D

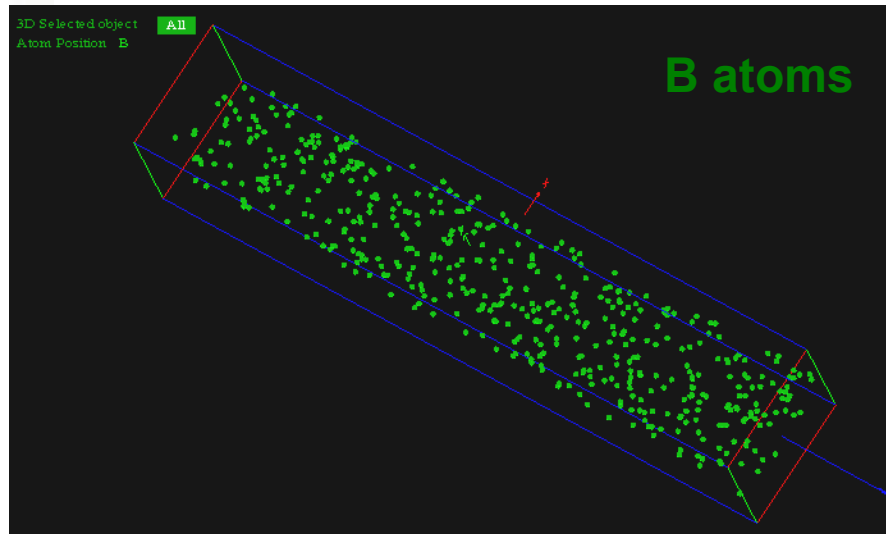
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# 3D dopant profile: how to measure it?

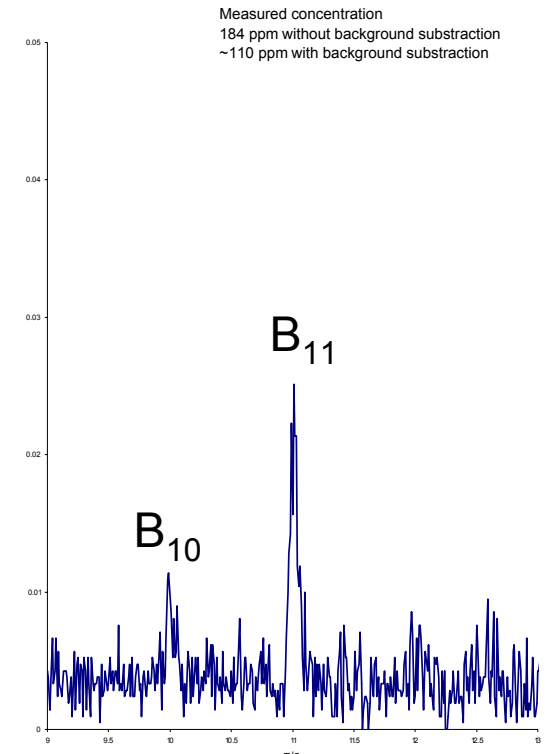
TEM tomography?

fs laser assisted tomographic atom probe



10 Matoms Si, 1000 atoms B

Courtesy: B. Deconihout et al. – Rouen Univ. & CNRS



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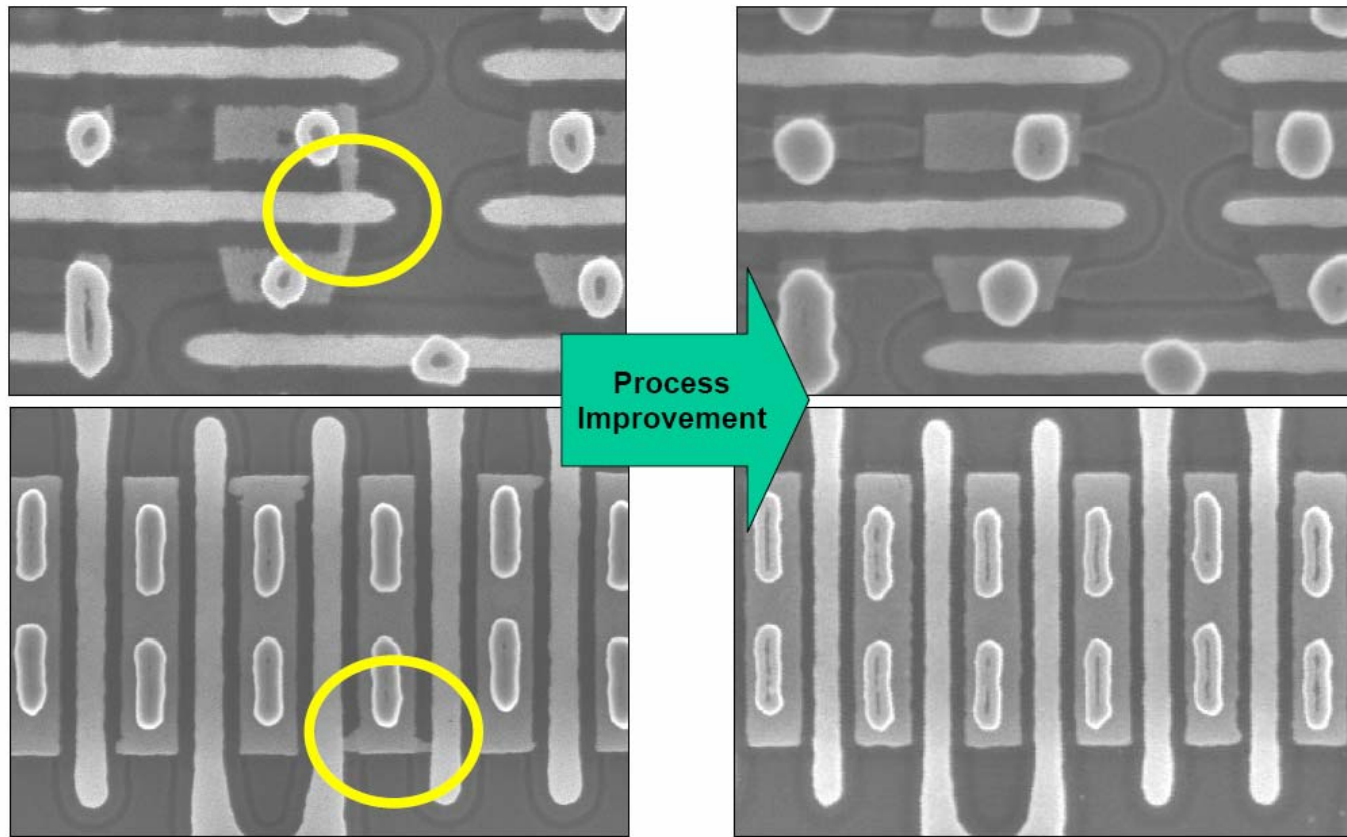


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# Salicide: stress-assisted diffusion



**Ni moves into the silicon; affected by strain**

Technology for Innovators™

TEXAS INSTRUMENTS

*from H. Stork, - 2005 Int. Conf. on Charact. and Metrology for ULSI Technol.*

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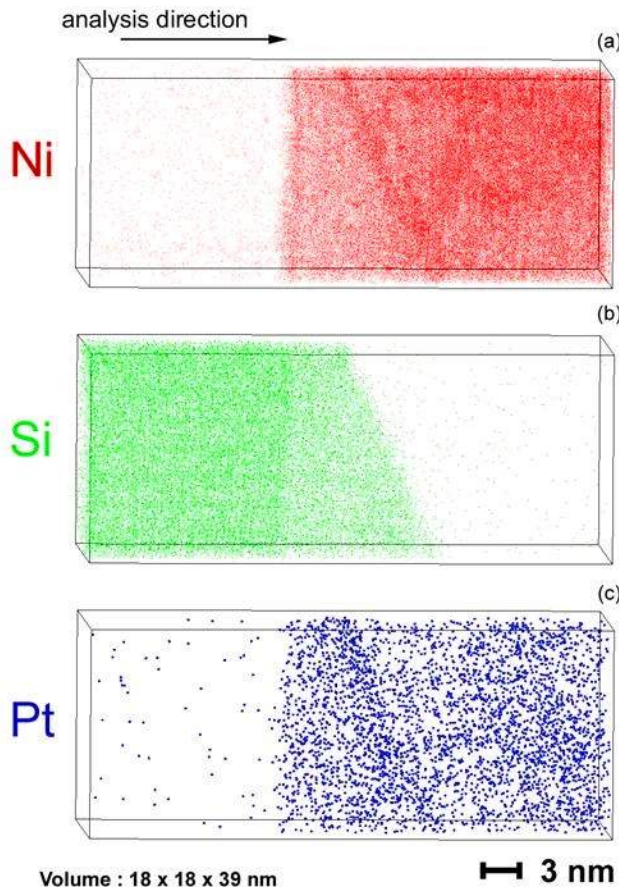
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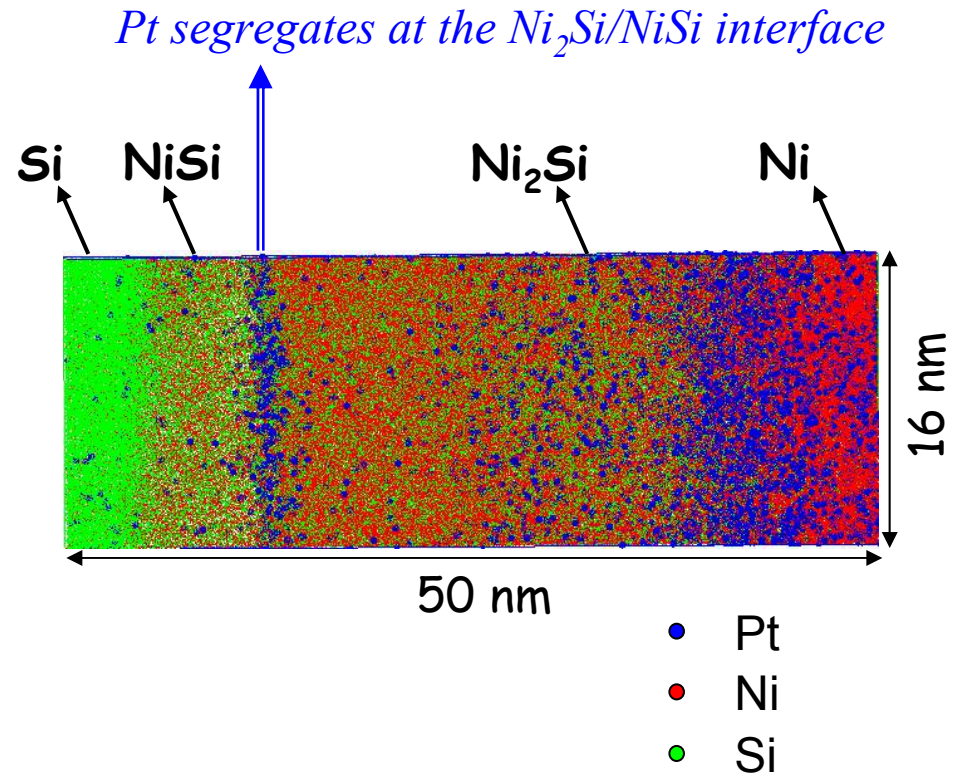
# NiPtSi 3D characterization

*as deposited*

*after 290°C 1h*



from K.Hoummada et al., APL 89 181905 (2006)



after O. Cojocaru, E. Cadel

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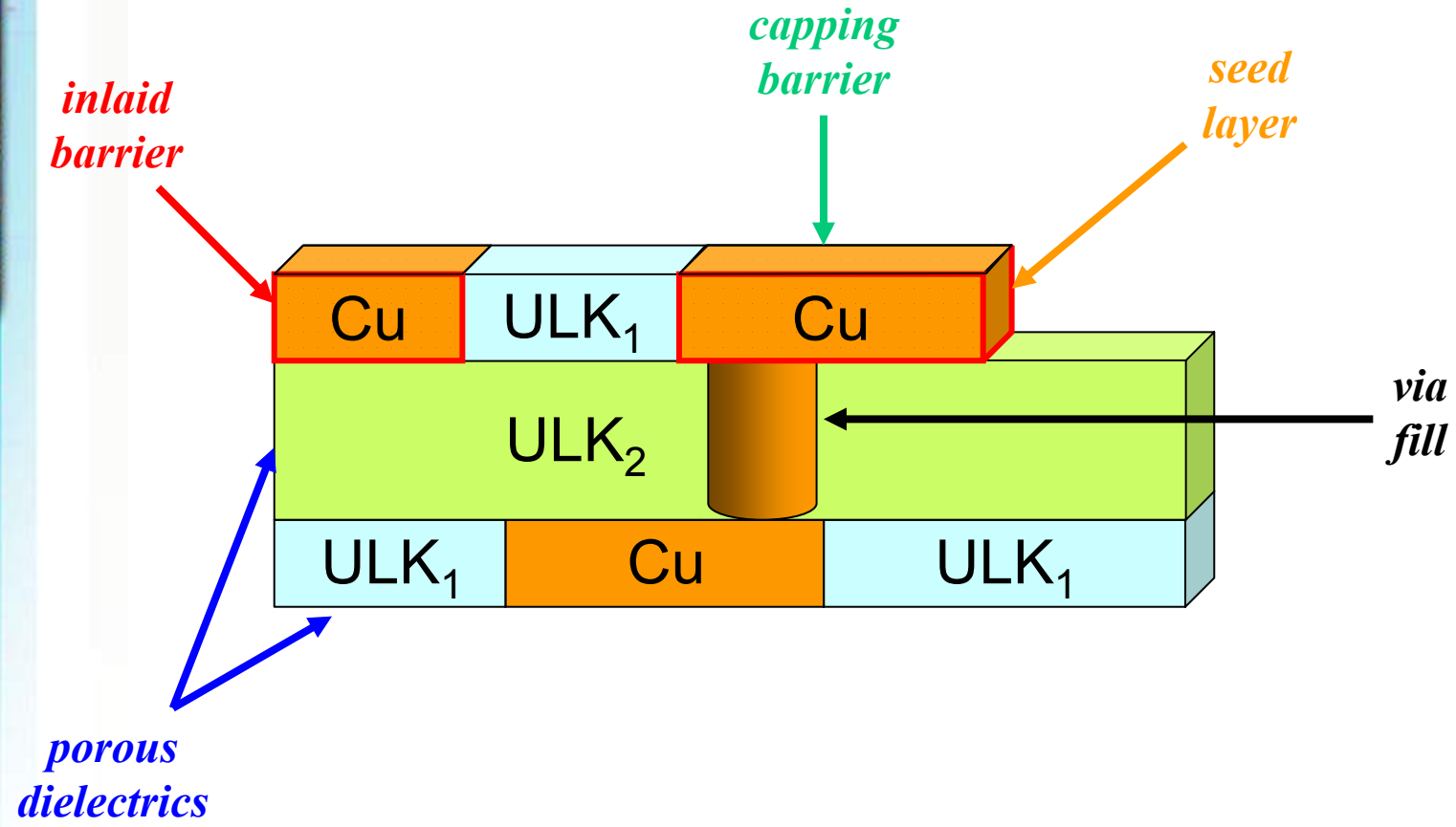
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# Interconnection challenges



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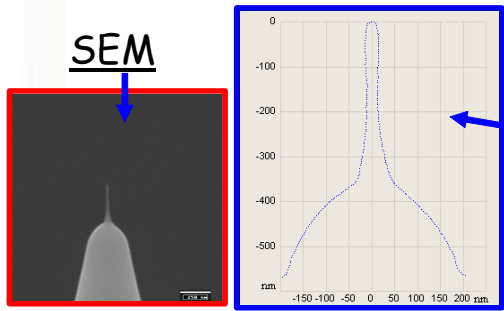


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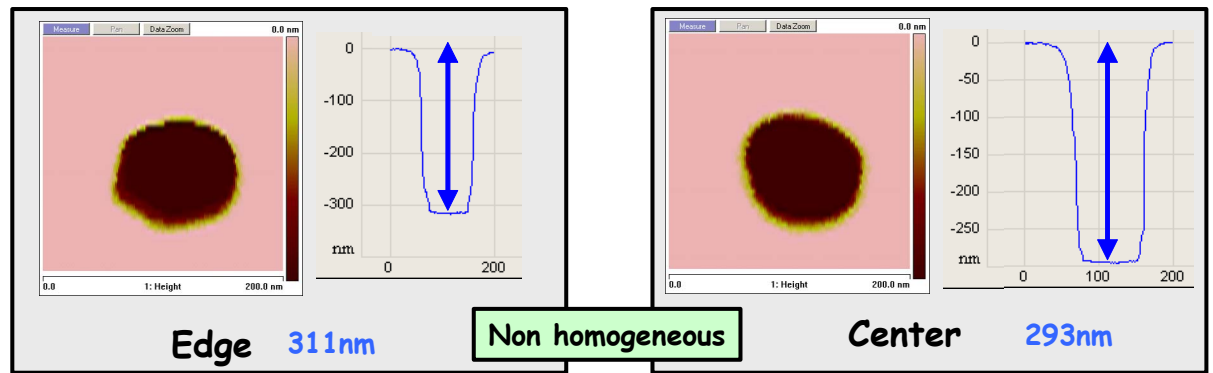
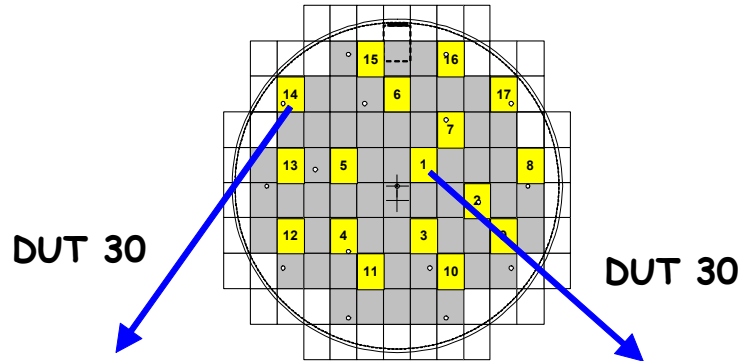
# 3D AFM via characterization



Cylindrical tip

X3D Tip Shape Reconstruction

Wafer mapping  
Statistical data

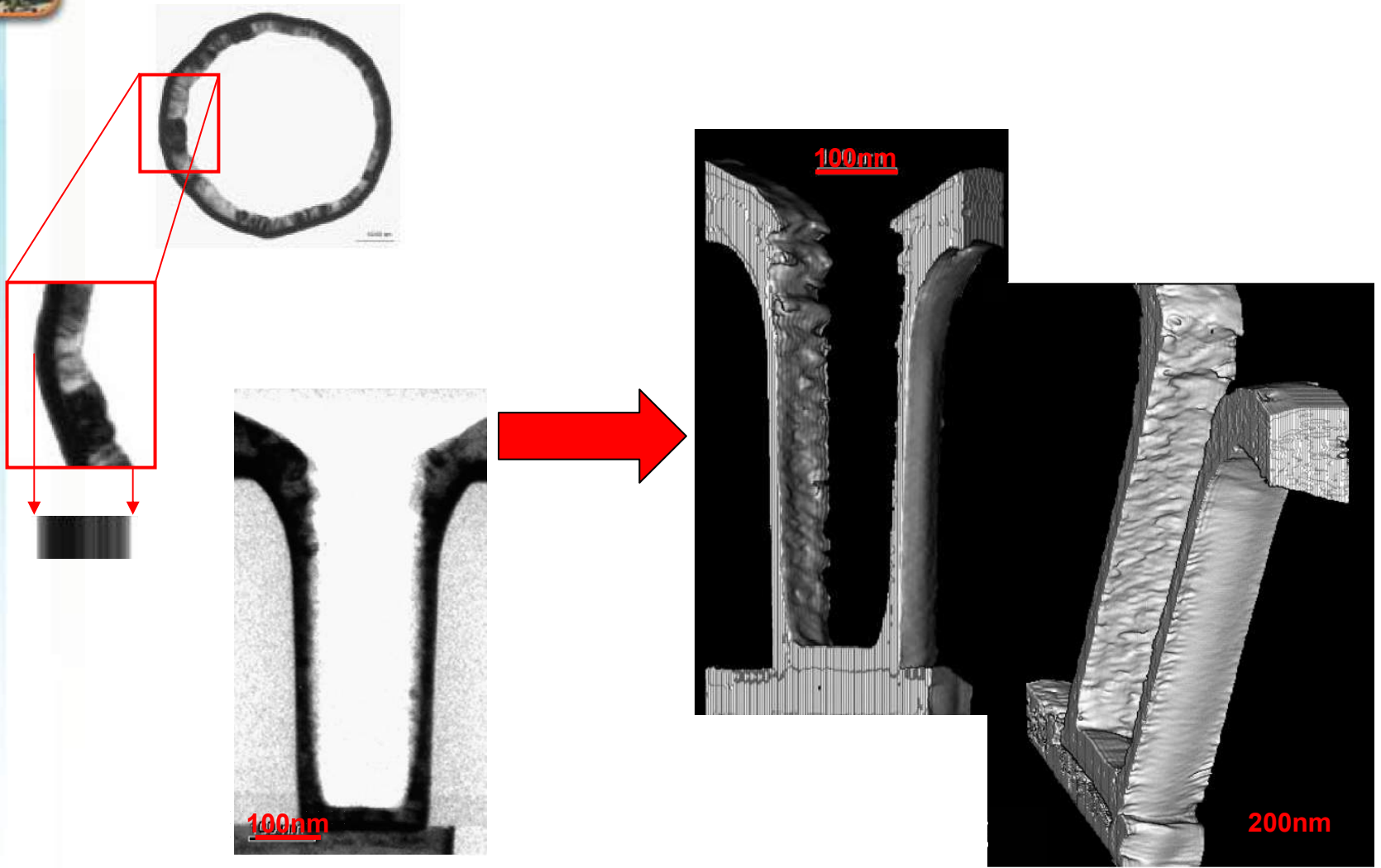


Courtesy: J. Foucher – CEA/LETI

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# Via barrier + seed TEM tomography



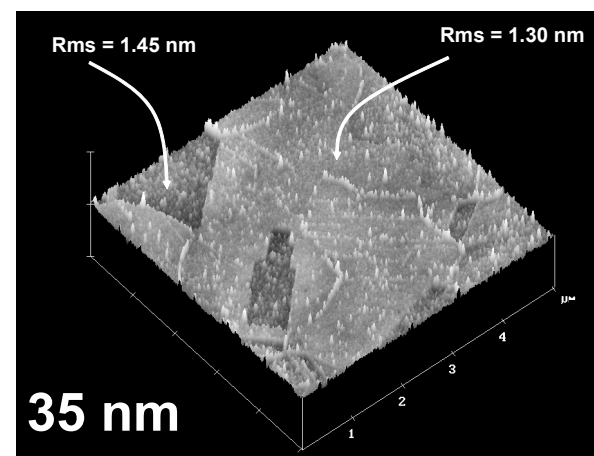
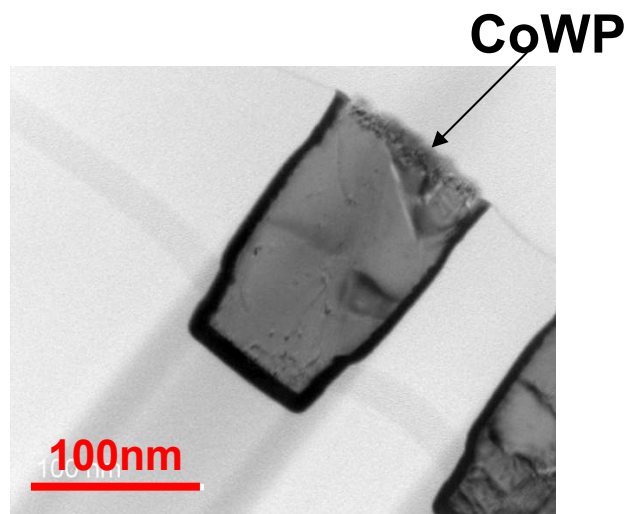
from H.Stegmann et al. ME 65 171 – 183 (2003)  
 & Science, Technology and Education of Microscopy: an Overview p.187  
 & from E. Zschech Future Fab Issue 14

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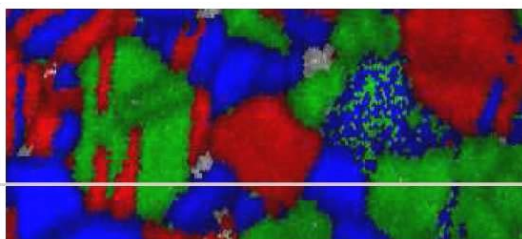
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# Electroless self-aligned barrier

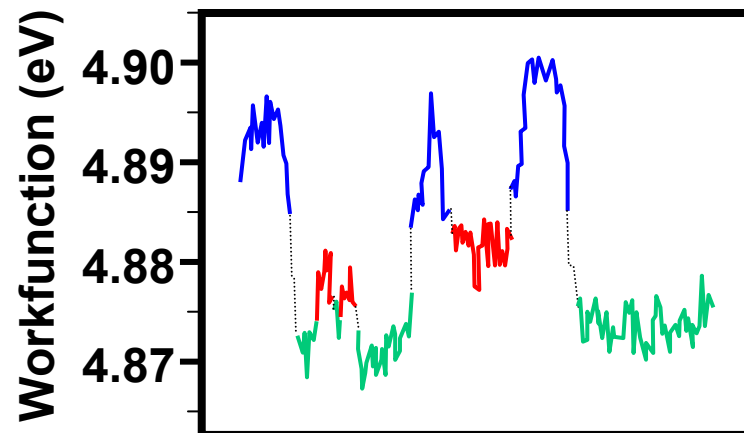
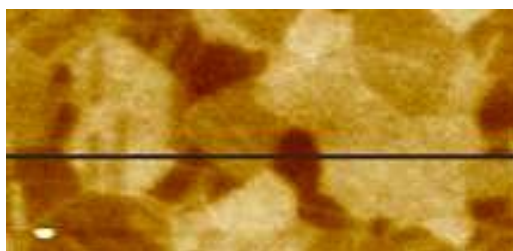


EBS

- <111>
- <100>
- <110>



KFM



from N.Gaillard et al. APL 89 154101 (2006)

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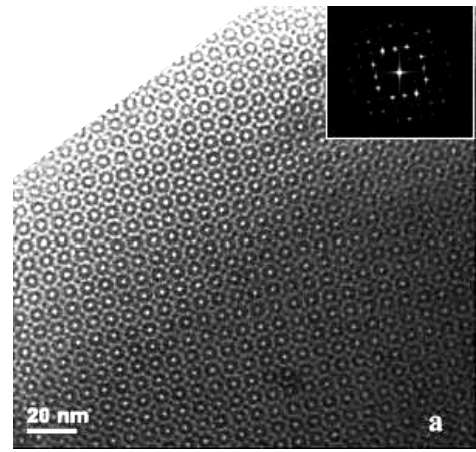
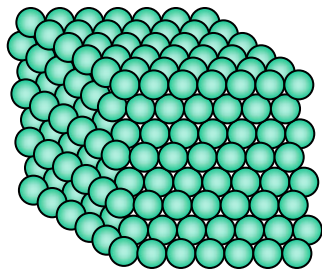
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# Which kind of ULK porosity?

**periodic**

**self-organized pores**



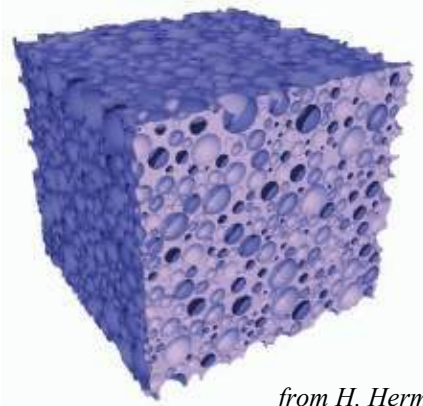
from Z.Zhang et al. *Microporous & Mesoporous Materials* 90 23-31 (2006)

**random**

**optimum closed pore system**

70% porosity  
 $f(R) \propto (R/R_0)^{-3.3}$

**physics of sandpile**



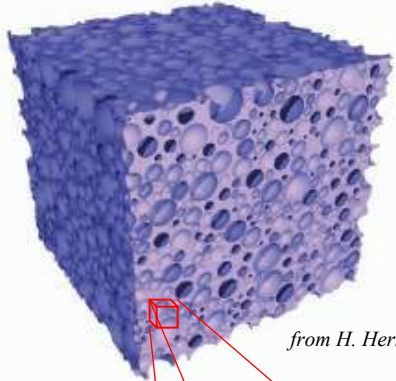
from H. Hermann (2004)

**What is optimum wrt. k value, process & mechanical properties?**

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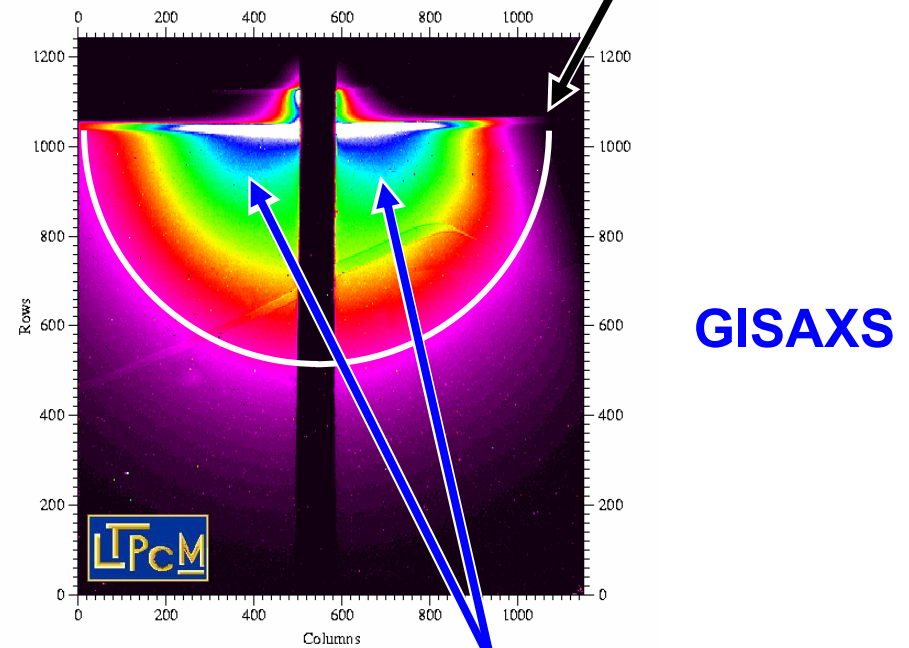


# ULK: understanding the porous structure



from H. Hermann (2004)

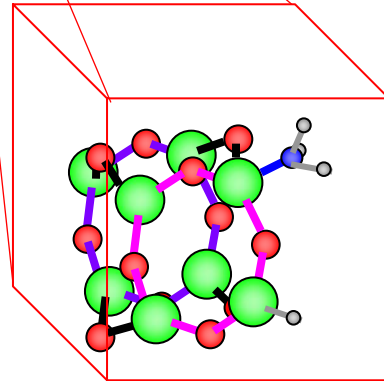
- Diffusion bump
  - ⇒ pore shape
  - ⇒ pore size



**GISAXS**

- Correlation peak
  - ⇒ distance between pores
  - ⇒ pore organization

- Si
- O
- C
- H



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# ULK: understanding the porous structure



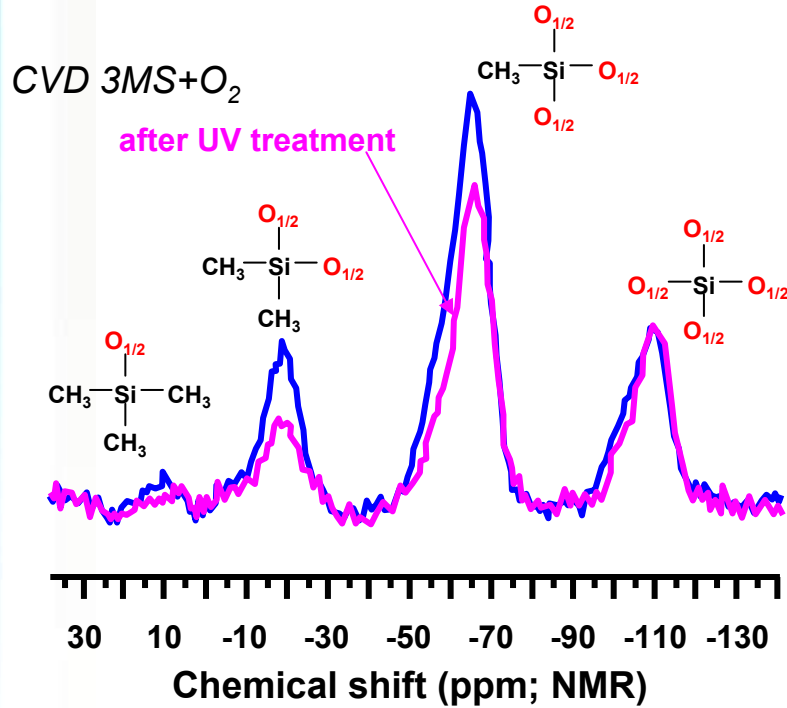
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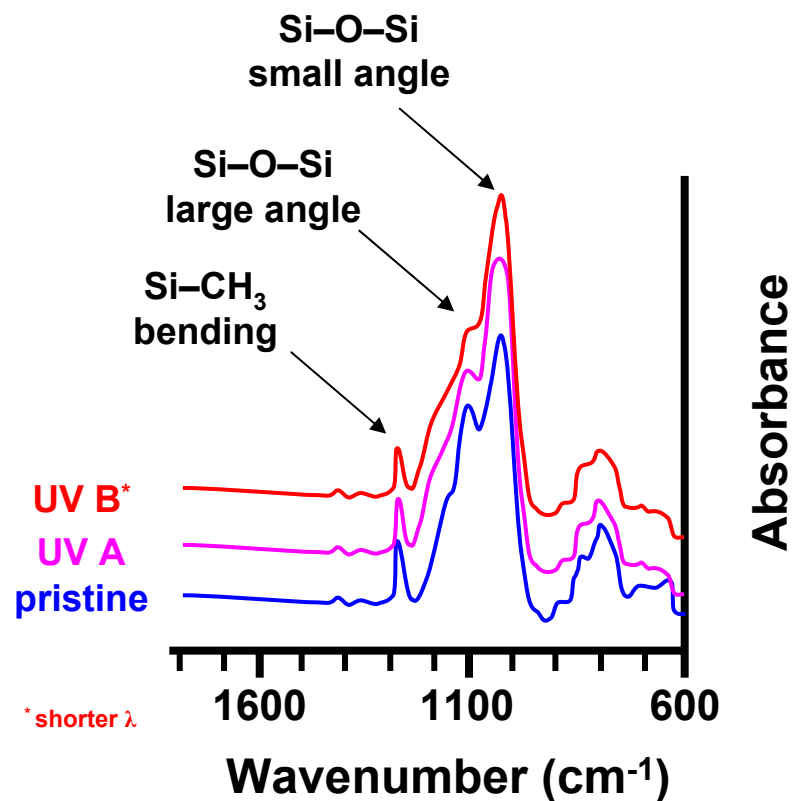
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axcelis



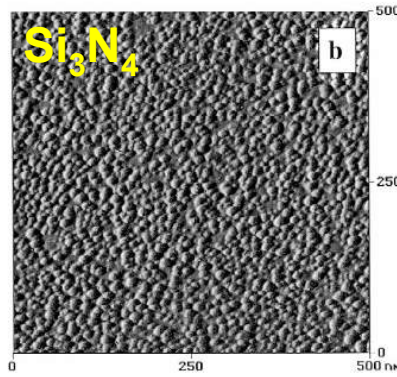
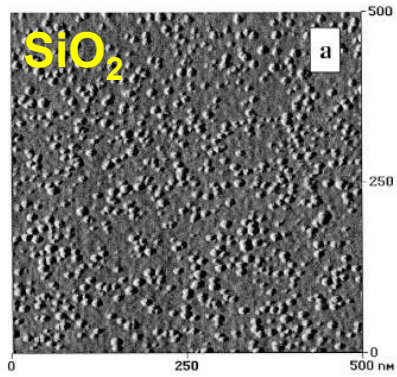
after F. Iacopi et al., J. Appl. Phys. 99 053511 (2006)



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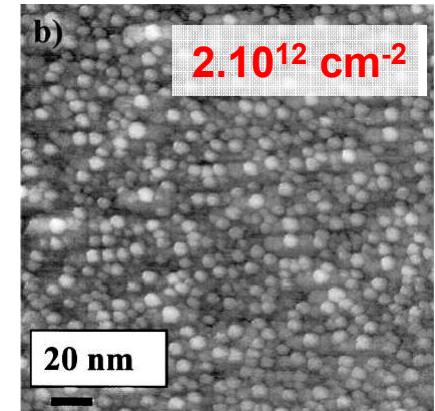


# Using nanocrystals for NVM

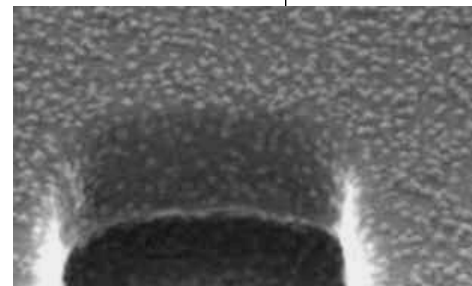
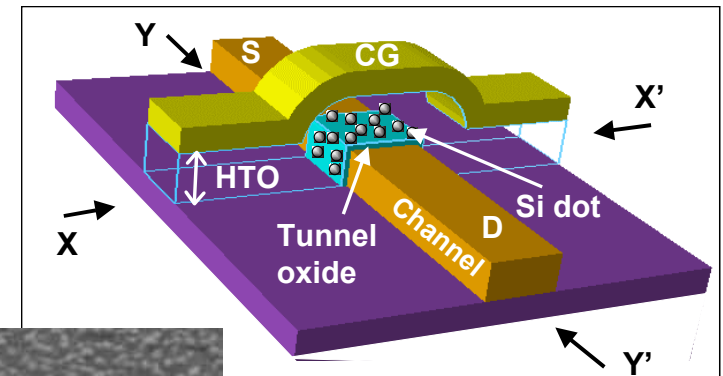


from T. Baron *Appl. Surf. Sci.* 164 29-34 (2000)

...targeting high dot density



from T. Baron *Appl. Phys. Lett.* 79 1175 (2001)

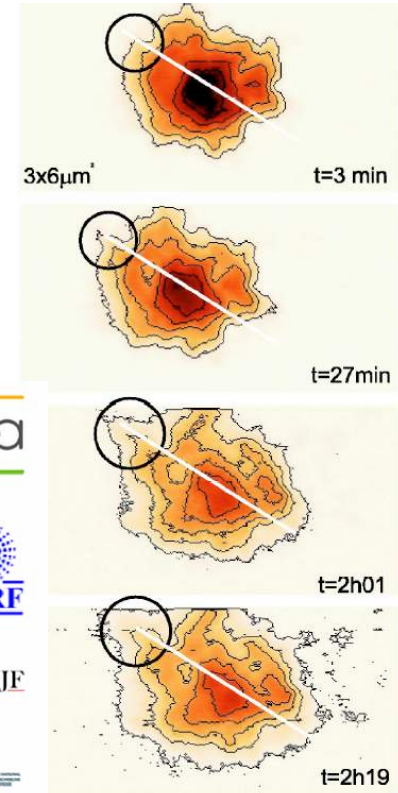
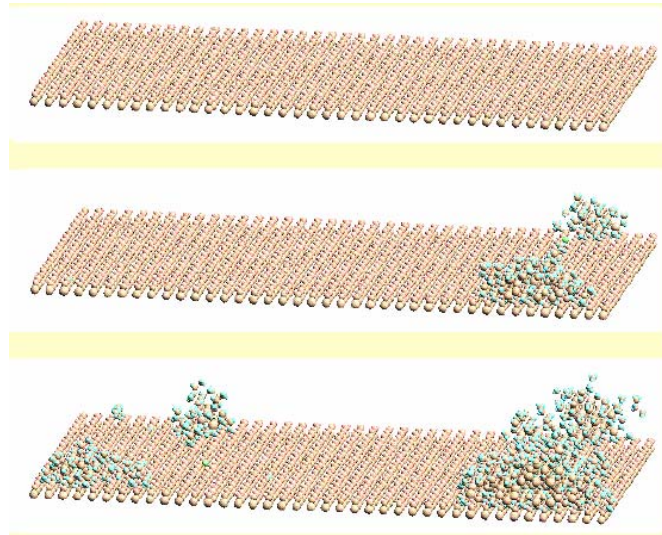
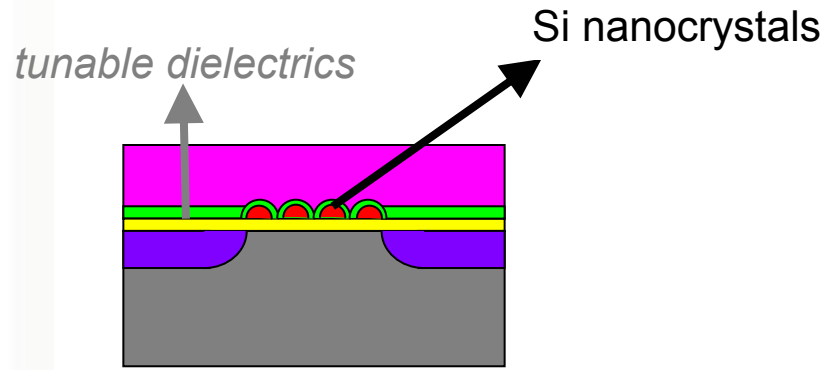


... & applied on complex 3D structures





# nc-NVM simulation & characterization



charge spreading by EFM  
*from R.Dianoux et al. Phys.Rev. B71 125303 (2005)*

atomistic simulation



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# MIM capacitor: material optimization

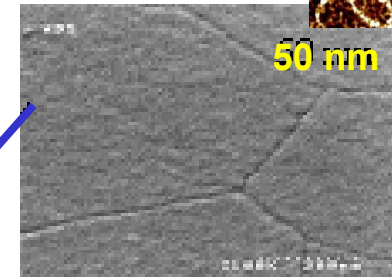
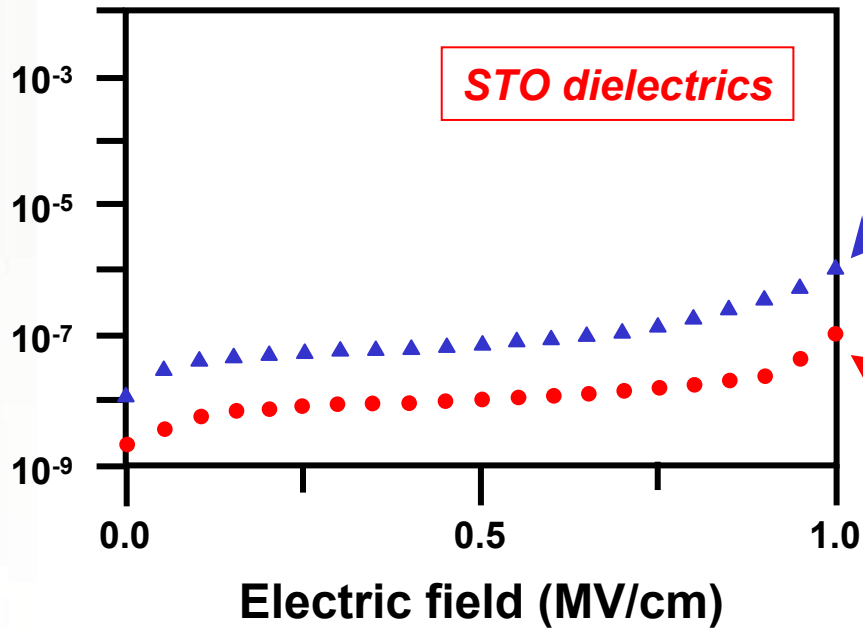


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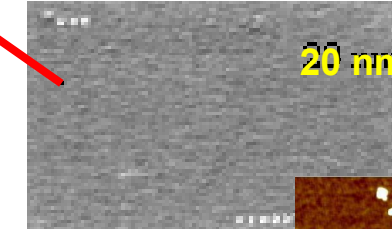
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Leakage current (A/cm<sup>2</sup>)

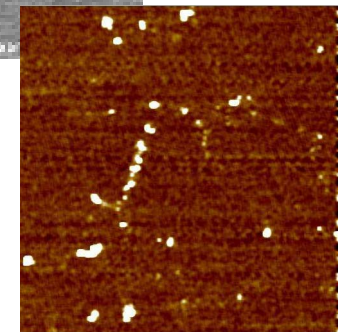
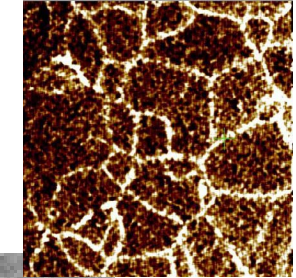


50 nm

SEM pictures



20 nm



TUNA



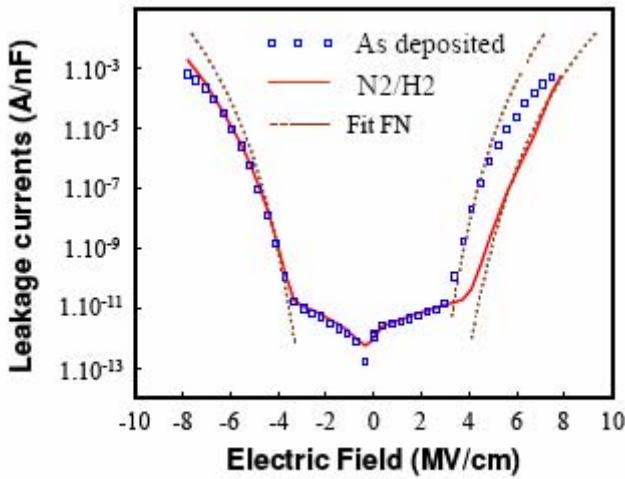
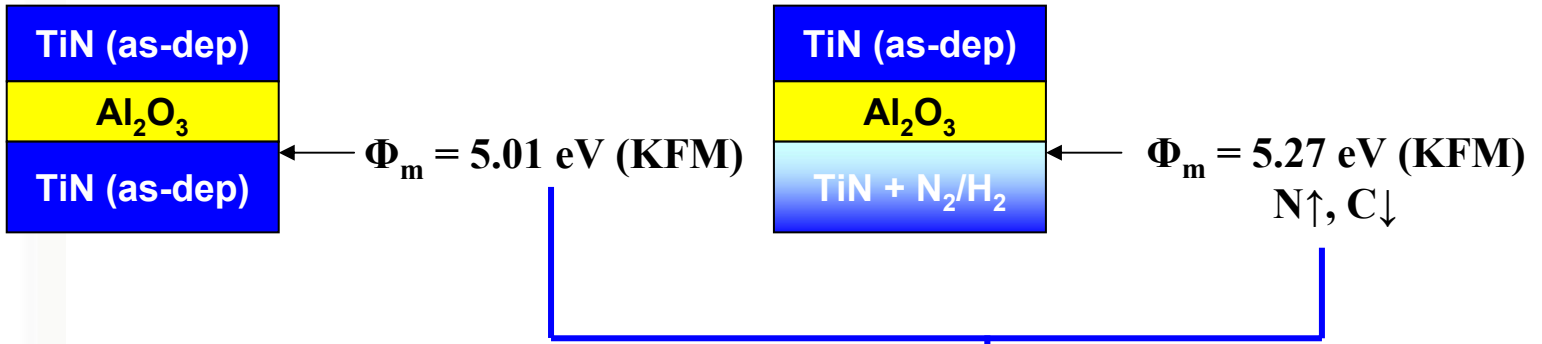
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# MIM capacitor: effect of the electrode material



Courtesy of Aurélie Bajolet (STM)

$\Delta\Phi_m = 0.26 \text{ eV (KFM)}$   
**consistent with**  
**the electrical measurements**  
 $[\Delta\Phi_m \approx 0.3 \text{ eV}]$

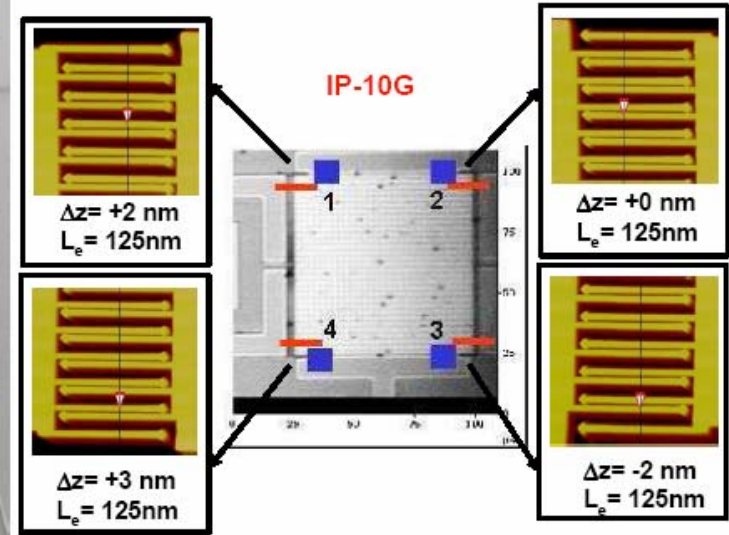
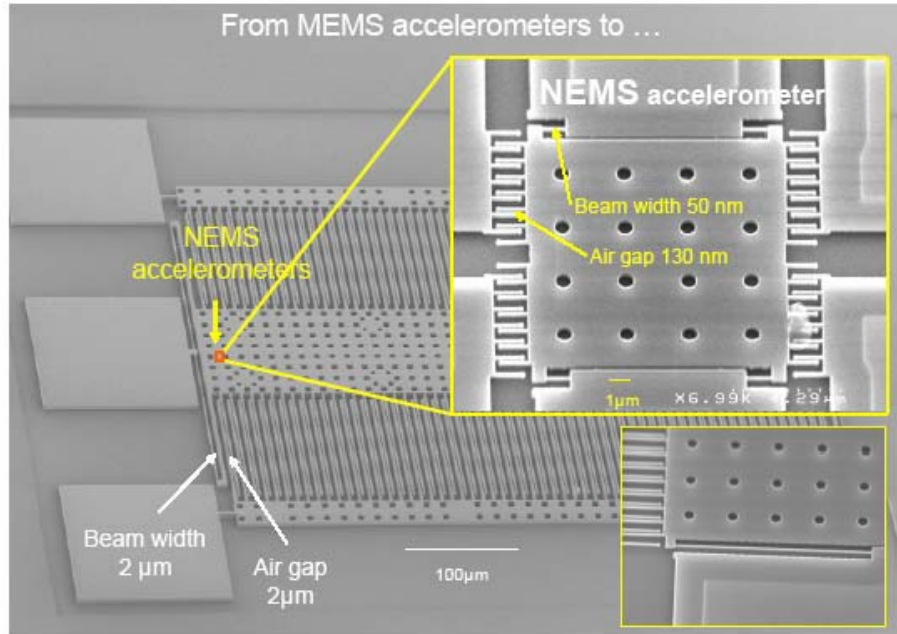


from N. Gaillard et al., MAM 2006

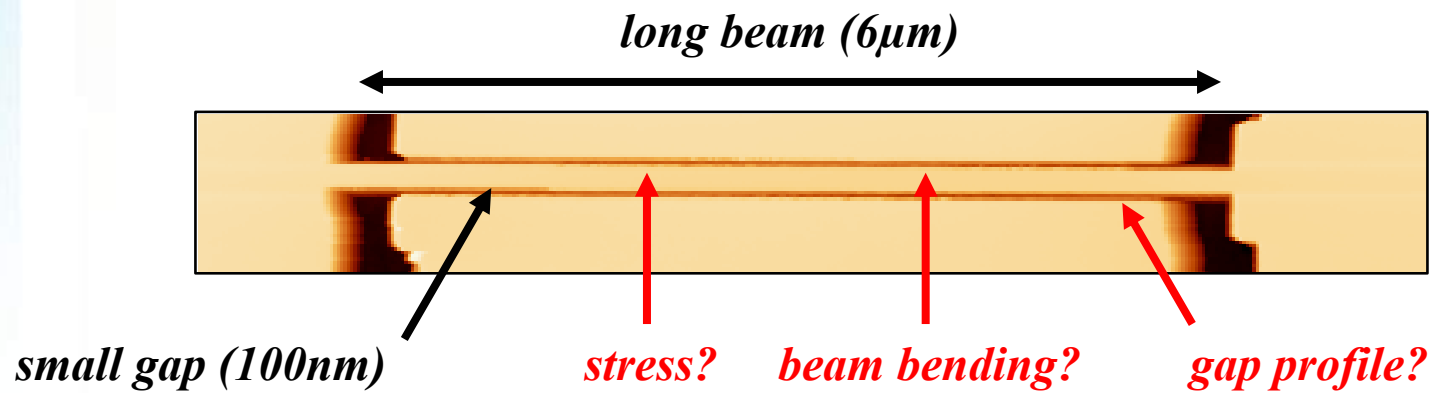
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# NEMS characterization

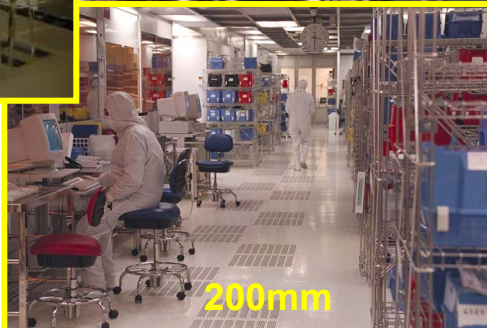
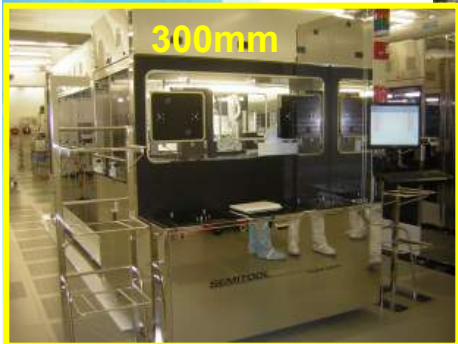


AFM characterization of NEMS



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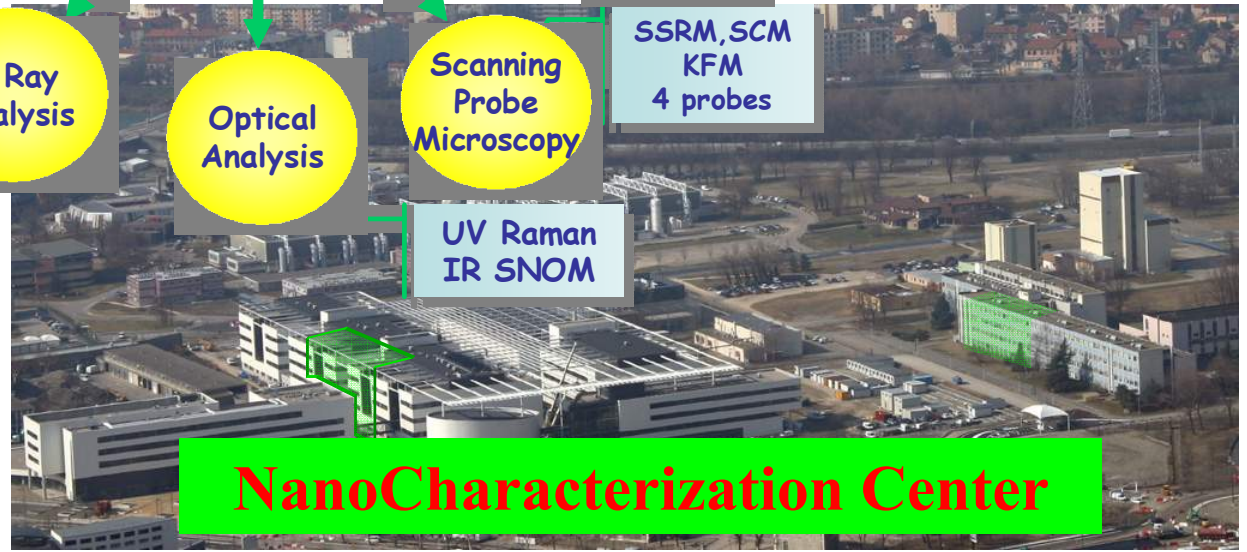
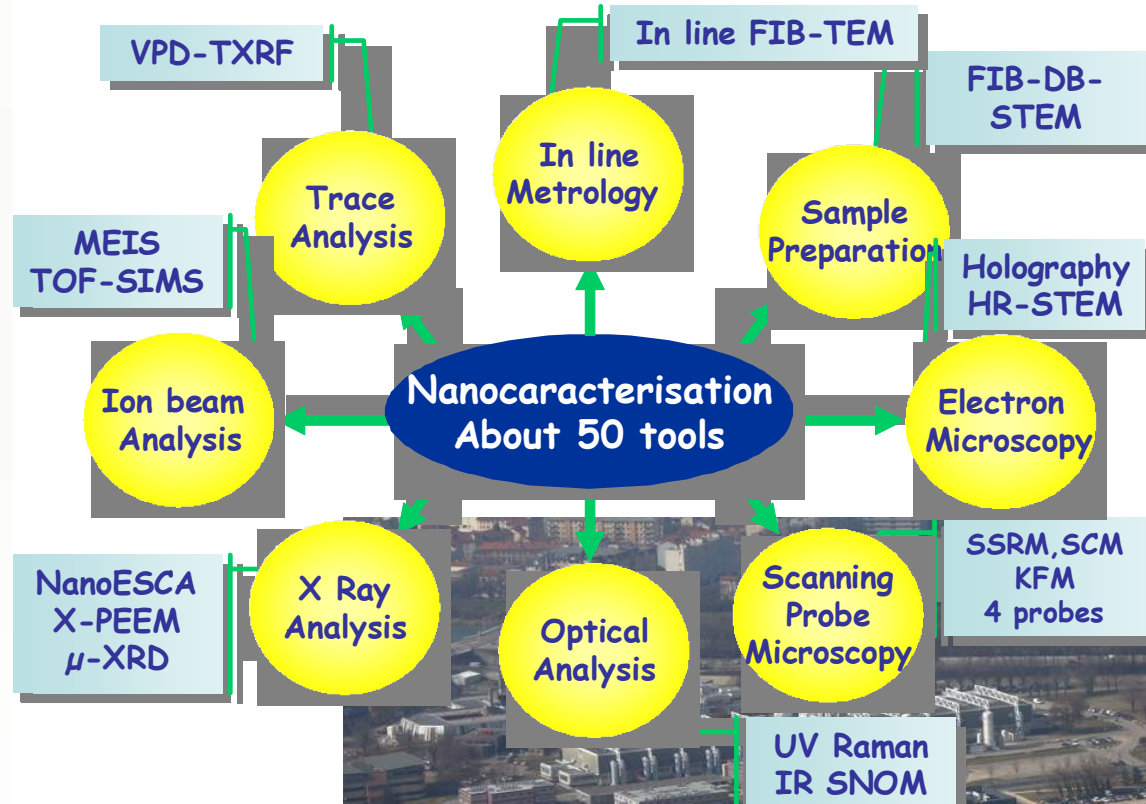
# Need of pooling resources together



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# Need of pooling resources together



**NanoCharacterization Center**



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# Outline

- A changing R&D landscape in nanoelectronics
- The European models, incl. CEA-LETI
- Trends in characterization

➔ Conclusion



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# Conclusion

- The microelectronic industry is on the verge of a major qualitative change
- More specialization and consolidation will happen in the next future
- New ways of R&D appear in a “coopetitive” environment
- Nanocharacterization for microelectronics will need to pool more resources in close proximity
- CEA-LETI developed a cooperation model robust to the present evolution



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**Thank you for your attention**



micro and nanoelectronics  
microsystem  
ambient intelligence  
biology and health  
image chain



# *Innovation for industry*

Loyalty  
Entrepreneurship  
Team work  
Loyalty Innovation  
Entrepreneurship  
Team work  
Innovation



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