Metrology Requirements & Challenges for Advanced FinFET Technology: Insight from TCAD Simulations

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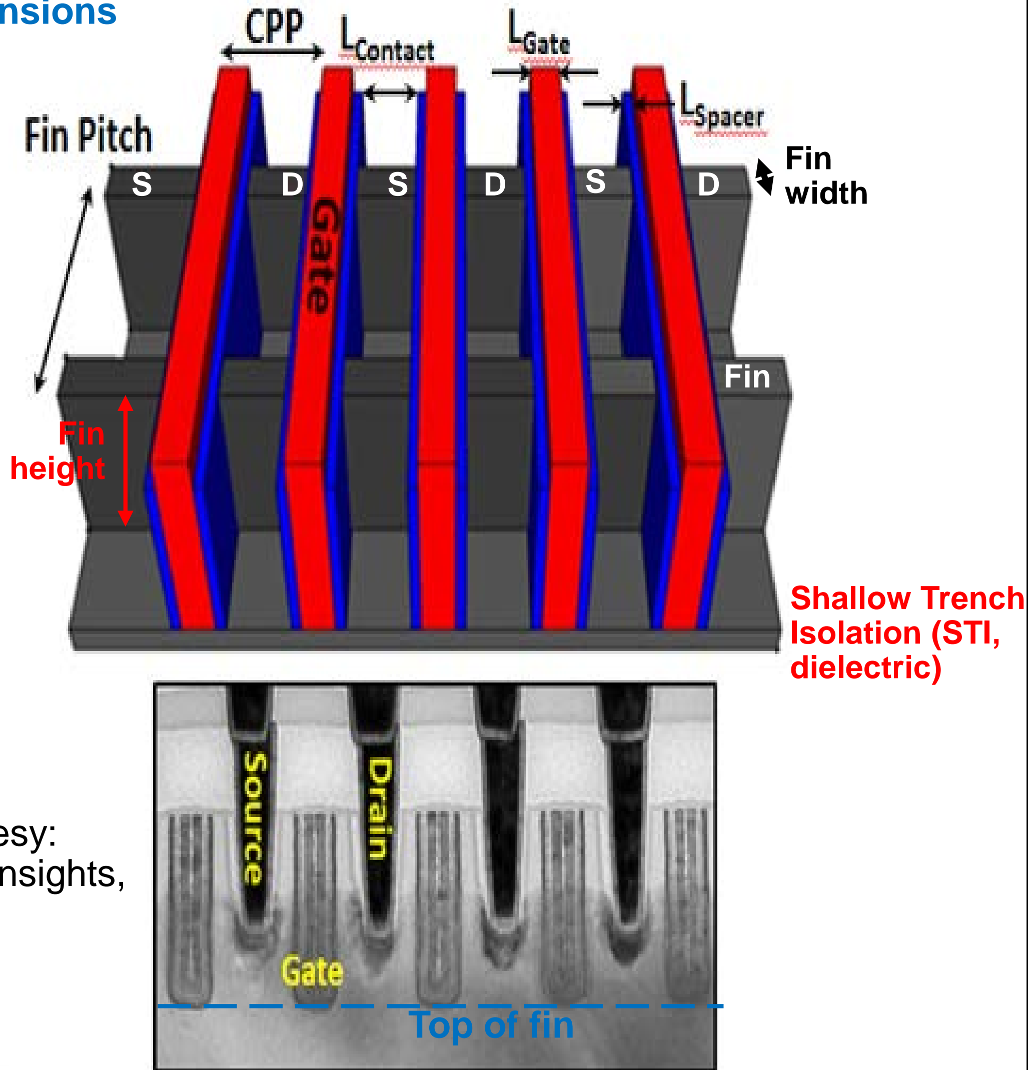
Introduction

- **FinFET architecture introduced to production at 22nm technology node, currently being scaled to 7nm node**
  - For scaled technologies at 22nm and beyond, FinFET enables improved electrostatics and performance compared to planar FET technology
  - Advanced FinFETs ➔ highly scaled dimensions, complicated 3D structures, and fully depleted operation
    - FinFET technology requirements go beyond what is required for previous planar FET technologies
    - TCAD simulations utilized here to understand technology requirements ➔ insight into metrology for FinFETs
    - Device and process integration insights also are utilized

Overall FinFET structure and key dimensions

Simplified, schematic overview of FinFET, showing key dimensions



Courtesy: Tech Insights, Inc.

TEM view of FinFET source and drain. This is a cross-section through the middle of one of the fins.

- **Fins are tall and narrow**
  - Gate wraps around fins on top and sides—because of narrow fins, gate control/electrostatic integrity is enhanced
- **This is a typical layout; number of fins with same gate is variable**
- **S=Source, D=Drain**
- **Fin pitch x CPP determines transistor density**
- **Active transistor is defined by Fin Height**
  - Weff=2 x Fin Height + Fin Width

Key FinFET device issues

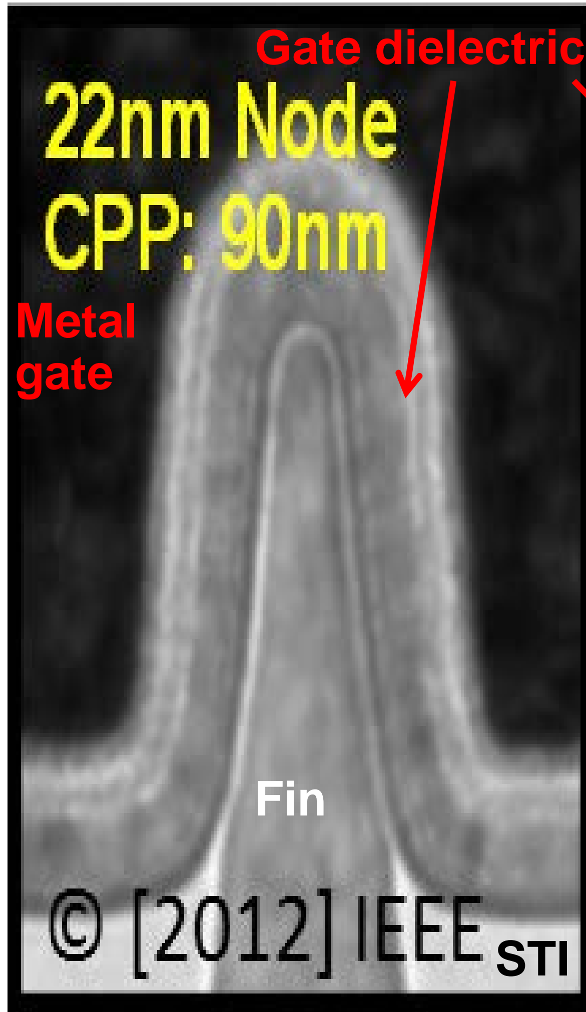
- **Electrostatics➔short channel effect and leakage control**
  - Characterized by subthreshold slope, SS, and drain induced barrier lowering, DIBL (Vtlin – Vtsat)
    - Because channel doping is low and fin width is narrow and gate surrounds fin on top and sides, geometry is key to controlling electrostatics
    - Lgate and Fin Width are critical; in particular, Lgate/(Fin Width) is particularly important. Rule of thumb: this ratio should be at least >1.5, and >2 is considerably better➔drive to smallest practical Fin Width
    - Vertical fin is most ideal here
- **Punchthrough leakage➔S-D leakage in the substrate below the active fin**
  - Must be effectively controlled with doping
- **Transport in the channel: mobility, channel doping, stress induced mobility enhancement, interface control**
- **Parasitic elements (R and C): reduce ability of the core FinFET to deliver performance**
  - Rexternal and Cov are important parameters here
- **Scaling impacts all of the above elements, and all of them must be controlled to optimize performance**

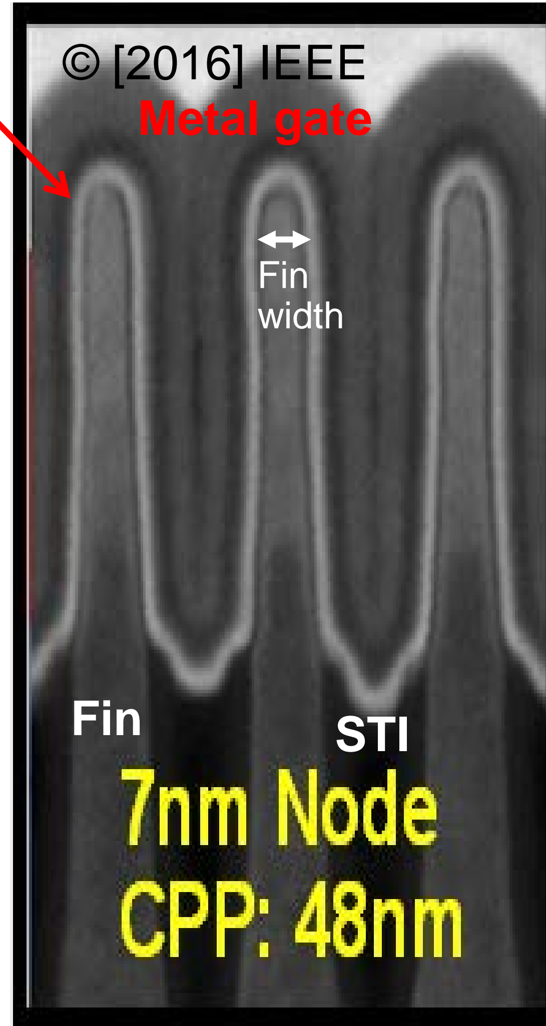
7nm TCAD evaluations

TCAD exploration of key variations

- **TCAD simulations were run to explore the impact of key variations on performance, electrostatics, and parasitics**
  - Devices simulated were representative 7nm nfets with Si channel
  - Devices were idealized, with analytical doping profiles and close to ideal, vertical fins
  - Results were analyzed in terms of overall technology requirements for performance, leakage, short channel control, etc.
- **Items examined directly with TCAD**
  - Fin sidewall tilt angle
  - Lgate
  - Fin width
  - Fin height
  - Doping in the substrate under the active fin: punchthrough leakage control

FinFET TEM cross-sections showing FinFET sidewall tilt angle





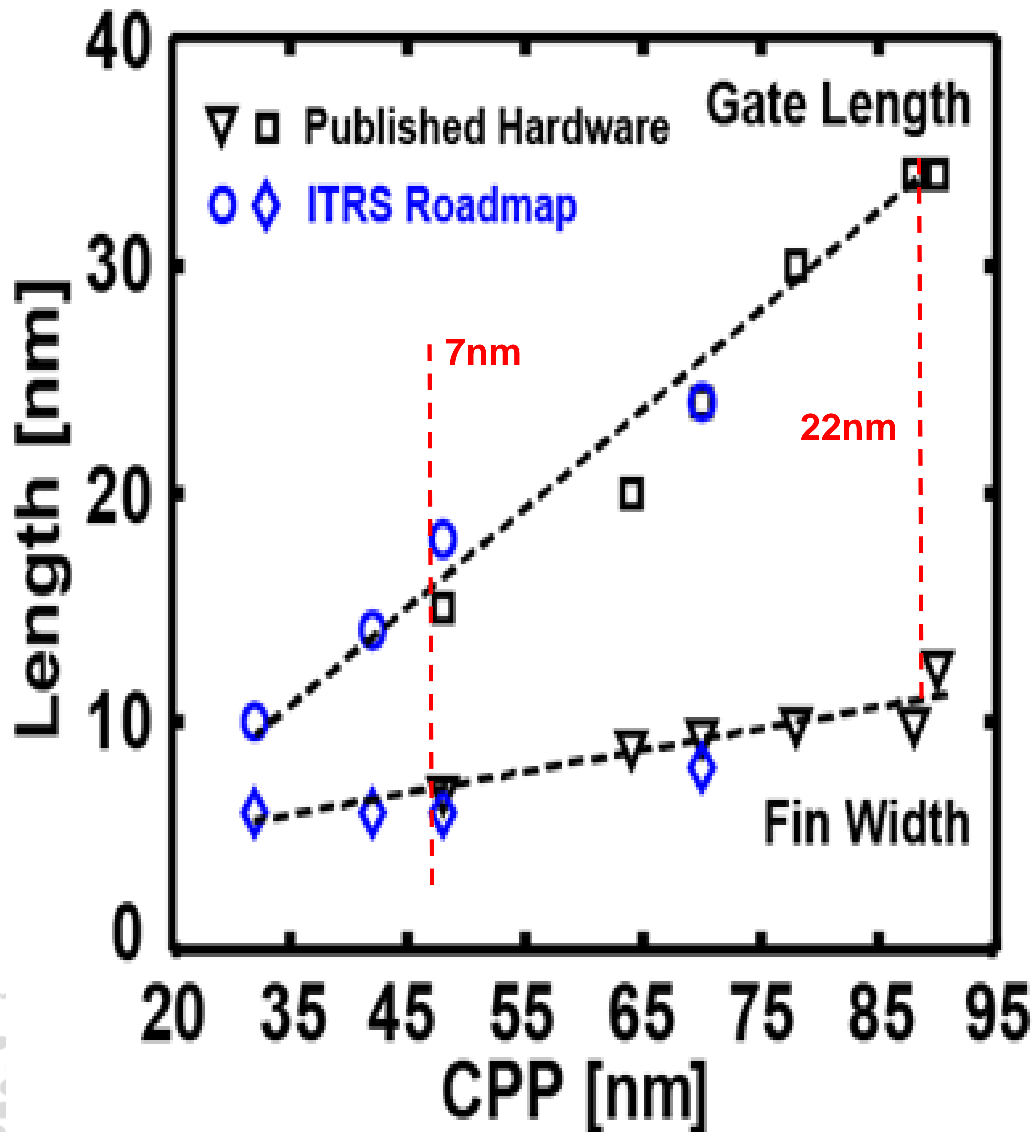
- The industry has significantly improved fin profile—at 7nm, very close to ideal vertical profile
- For 7nm, vertical fin profile➔ improved electrostatics and performance. Increased fin tilt angle will degrade electrostatics and performance

Variation in fin sidewall tilt angle, from TCAD

Tilt delta (nm)	Delta DIBL (mV)	Ioff (nA/um, relative: ratio)	Ieff (uA/um, relative:ratio)
0 (nominal)	0	1.00	1.00
2	10	3.68	0.95
4	20	8.16	0.89

- **"Tilt delta" is the difference between the fin width at the top and bottom of the active fin**
- **Short channel control, Ioff, and Ieff (performance) are all degraded by increased fin tilt**
- **From this, we clearly need to control tilt delta to better than 2nm**

FinFET gate length and fin width scaling versus CPP



- **Fin width is scaling more slowly than Lgate**
  - We are approaching ultimate fin width limits ~4-5 nm
- **Next, we'll look at the impact of varying Lgate and fin width**

TCAD results: variation in Lgate

Lgate (um)	Delta DIBL (mV, relative)	Ioff(nA/um, relative: ratio	Ieff (uA/um, relative: ratio)
0.013	7	2.71	1.05
0.014	2	1.45	1.02
0.015 (nom)	0	1.00	1.00
0.016	-6	0.53	0.97
0.017	-7	0.37	0.93

- **As Lg decreases**
  - Short channel control is degraded→DIBL increases (Vtsat decreases) and Ioff increases sharply
  - Ieff increases due to decreased Vt and decreased Lgate
  - From the above, Lg needs to be controlled to about 1nm (particularly for controlling Ioff)

TCAD results: Fin width variation

Delta FW (nm)	Delta DIBL (mV)	Ieff (uA/um, relative)
-1	-1	1.01
0 (nominal)	0	1.00
2	15	0.94
4	32	0.84

- **Delta FW is the change in fin width from the nominal, which is zero here**
- **DIBL increases sharply with DeltaFW, due to poorer short channel control**
- **Ieff decreases with DeltaFW, driven by the poor short channel control**
- **From the above, fin width needs to be controlled to 2nm or better**

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TCAD results: Fin Height variation

Change in Fin Height (nm)	Ceff (fF, relative: ratio)	Ieff (uA/fin, relative: ratio)	Ieff/Ceff~Performance (GHz, relative: ratio)
-2	0.9813	0.9680	0.9864
-1	0.9902	0.9800	0.9897
0, Nominal	1.0000	1.0000	1.0000
1	1.0118	1.0200	1.0081
2	1.0216	1.0360	1.0141

- **Weff, the effective device width, varies with Fin Height➔Ieff/fin increases, but so does Ceff**
- **Electrostatics unaffected**
- **Performance increases slowly with Fin Height**
- **From the above, control of fin height to 2nm is clearly adequate**

Doping in the substrate: to control punchthrough leakage

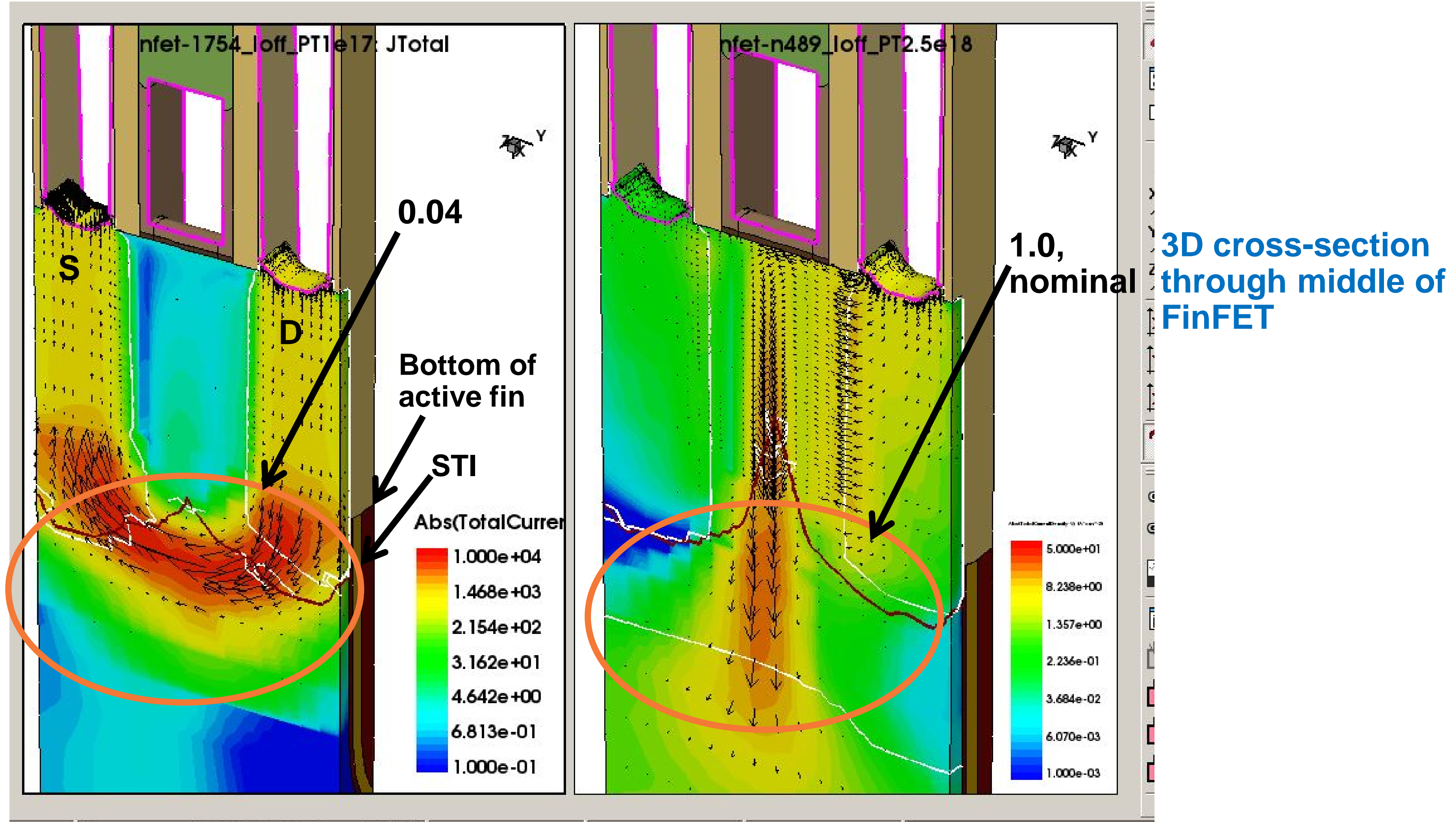
- **Simulated substrate doping varied from high value (nominal) down to low values**
  - Typically, a special implant ("punchthrough stopper") is utilized to dope the substrate below the active fin
  - FinFET channel is relatively lightly doped
- **Punchthrough leakage (in the substrate, from source to drain): monotonically increased as substrate doping decreased**

Ioff versus substrate doping: punchthrough leakage, from TCAD

	Substrate concentration (normalized)	Ioff (normalized: ratio)
Nominal	1.00	1.0
	0.40	15.3
	0.20	167.9
	0.04	5444.7

- **Ioff increase is due to increasingly strong punchthrough with decreased doping**
- **From the above, we need to be able to control the substrate doping**
  - An important practical issue here is loss of dopant to the STI oxide

TCAD plot: substrate (punchthrough) leakage, Vg=0 & Vd=Vdd: relative substrate doping = 1.0 (nominal), 0.04



3D cross-section through middle of FinFET

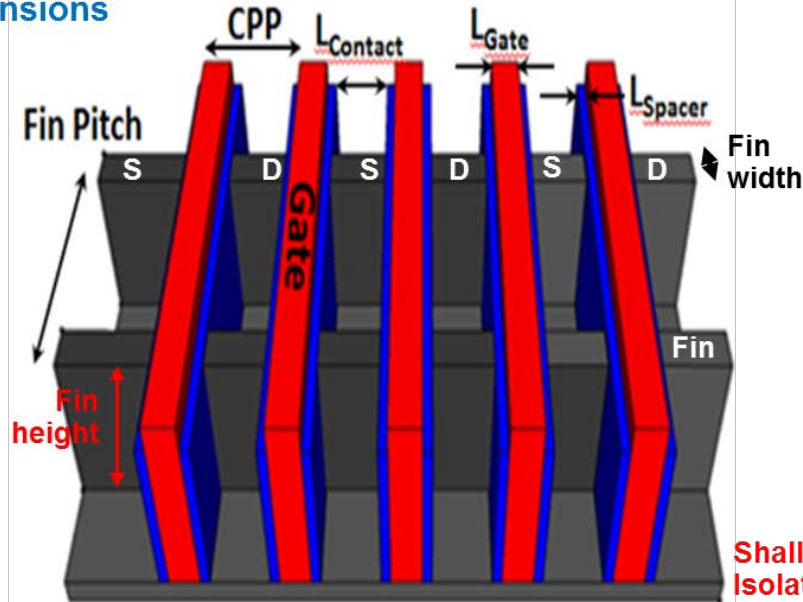
- **With low doping, depletion region reaches from D to S and punchthrough (PT) leakage current flows below the active fin**
- **With high (nominal) doping, depletion region is much reduced and PT leakage is cut off**

Other key issues

Other key issues: Lcontact

- **With scaling, reduced size of CPP, spacer width, and Lgate impacts Lcontact (see below)**
  - Lcontact = CPP – Lgate -2 * LSpacer
  - Rcontact is dependent on Lcontact, and Rcontact is an important component of parasitic resistance, Rexternal
  - For 7nm, TCAD indicates nominal Rcontact ~40ohm-um, which is undesirably high
  - *Controlling the CPP and spacer width as well as Lgate so that Lcontact can be controlled is important*

Simplified, schematic overview of FinFET, showing key dimensions



Shallow Trench Isolation (STI, dielectric)

Other key issues: Pitch walking and stress enhanced mobility

- **Pitch walking**
  - An important practical issue with advanced optical lithography: defined as unequal spacing from left to right in an array with nominally equal spacing (see below)
  - This is an issue with both fin and gate arrays—it is important to control it, especially for gate arrays
    - For gate arrays, on the side with shorter spacing, the contact length will be significantly shortened and hence the Rcontact will be considerably larger. This is particularly problematic for the source side
- **Strain**
  - To enable desired performance for advanced technology nodes, enhanced mobility has been deployed
  - The enhanced mobility comes from the appropriate stress (MPa) applied in the channel. This comes from straining the channel, typically by utilizing films of different composition and hence different atomic spacing
  - An important issue here is minimizing strain relaxation➔ensuring the strain is preserved throughout the process flow
  - Measuring the strain profile is clearly important

Pitch walking illustrated

Array without pitch walking

Array with pitch walking

Overall summary, metrology potential approaches

Overall summary, including metrology approaches (1)

#	Parameter	Technology requirement	Destructive: potential approach	Non-destructive: potential approach	Comments
1	Fin width	Control to ≤1nm	TEM	Hybrid metrology (OCD, CD SEM); CD AFM	Fin width CD critical to short channel effect control
2	Fin edge slope	≤2nm difference--top to bottom	TEM	Hybrid metrology (OCD, CD SEM)	Fin taper critical to short channel effect control
3	Spacer width, contact width	Control to ≤2nm	TEM	Hybrid metrology (OCD, CD SEM)	This controls transistor density and impacts Rexternal
4	Metal gate length	Control to ≤1nm	TEM	Hybrid metrology (OCD, CD SEM)	Metal gate length critical to short channel effect control and transport
5	Fin pitch, Contacted Gate Pitch (CPP)	Control to ≤2nm	TEM, SEM	Hybrid metrology (OCD, CD SEM); CD AFM	These pitches control transistor density and impact Rexternal

- Blue items above : technology requirement comes directly from TCAD simulations

Overall summary (2)

*	Parameter	Technology requirement	Destructive: potential approach	Non-destructive: potential approach	Comments
6	Pitch walking	Control to ≤2nm	TEM	Hybrid metrology (OCD, CD SEM); CD AFM	Pitch walking particularly impacts Rexternal
7	Gate metal to contact spacing	Control to ≤2nm	TEM	Hybrid metrology (OCD, CD SEM); CD AFM	This will affect overlap capacitance,
8	STI width	Control to (2-4) nm	TEM, SEM	Hybrid metrology (OCD, CD SEM); CD AFM	This will affect electrical isolation between transistors
9	Vertical doping profile in active fin	Ability to measure vertical doping profile in thin fins	1.5D SIMS* (sea of fins) or Atomic Probe (single fin)→doping profile. SCM or SSRM-carrier profiles	Transistor electrical test	Critical to controlling mobility, transport in the transistor
10	Vertical doping profile below active fin	Ability to measure vertical doping profile in thin fins	1.5D SIMS* (sea of fins) or Atomic Probe (single fin)→doping profile. SCM or SSRM-carrier profiles or SCM or SSRM	Transistor electrical test	Adequate doping below channel is needed to control leakage below active fin

- *Advanced SIMS technique for measuring doping profile in Fins

Overall summary (3)

#	Parameter	Technology requirement	Destructive: potential approach	Non-destructive: potential approach	Comments
11	S-D lateral profile	Spatial control to ≤1nm	2D profile: SCM or SSRM	Transistor electrical test	Control of this profile is critical to short channel control and transport.
12	Active fin height: STI recess	Control to ~2nm	TEM	-	This is critical to FinFET Ieff & Ceff ==>performance
13	Gate dielectric: thickness of layers and uniformity along fin	Control to a few angstroms	TEM	Electrical: tinv	This is critical to FinFET tinv==>short channel control, gate leakage, reliability, and mobility/transport
14	Gate work function metal: thickness and uniformity along fin	Control to a few angstroms	TEM	Electrical: Vt	This is critical to FinFET threshold voltage and its variability==> electrostatics and performance
15	Measurement of strain profile	Measure profile, especially in the channel	NBD + Electron Holography	XRD	This is critical to get enhanced mobility, which is important for meeting performance goals

Summary, conclusions

- **Technology requirements for 7nm FinFETs were examined using**
  - Direct TCAD simulations for several of the key requirements
  - General process integration and device knowledge
- **The technology requirements drive metrology needs**