Stanford University

Nanotechnology Overview

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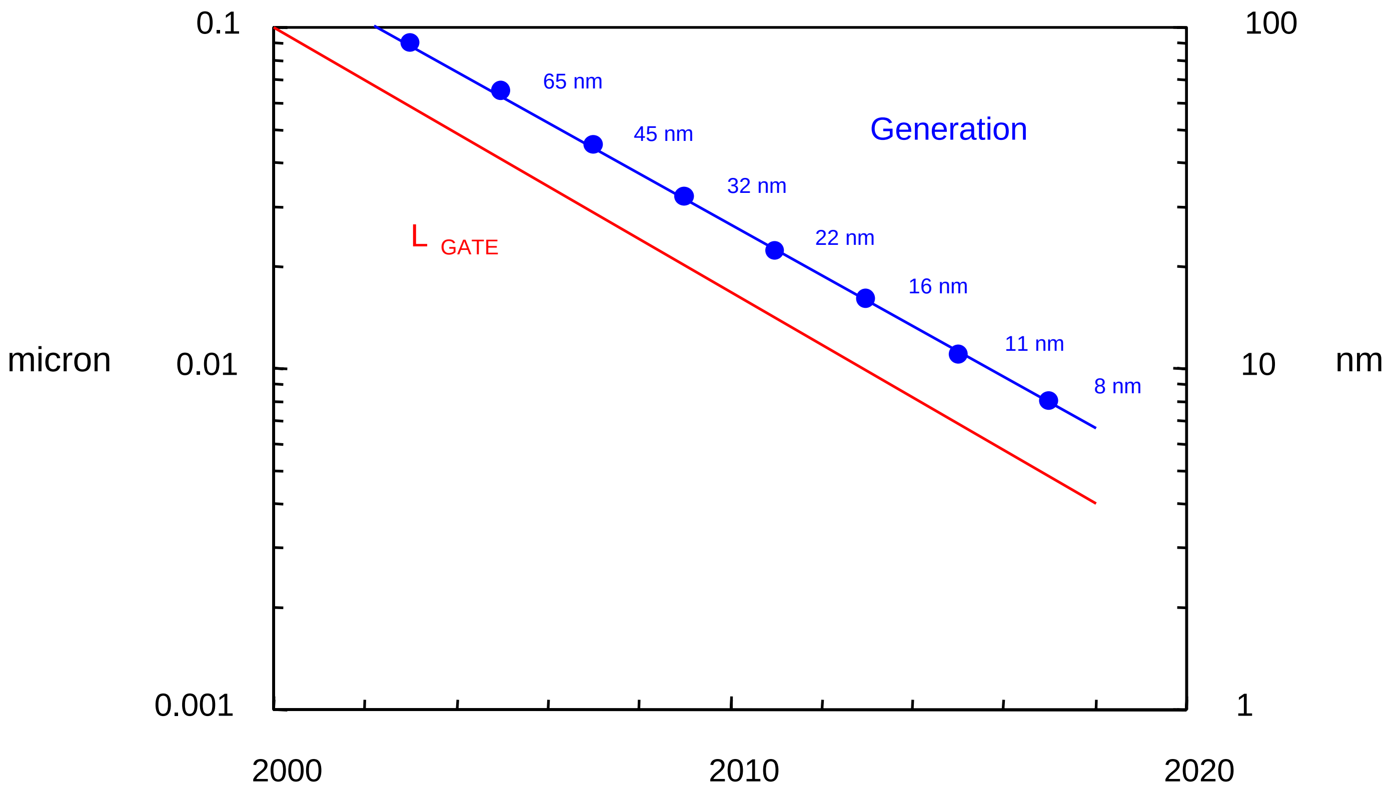
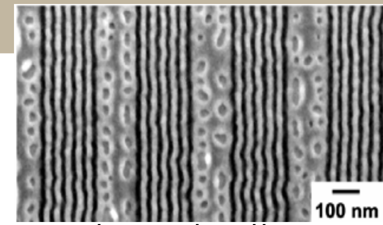
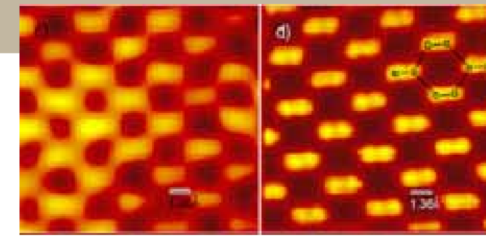
Nanoelectronics – Si CMOS

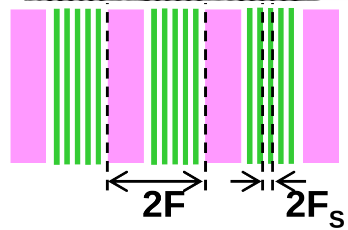


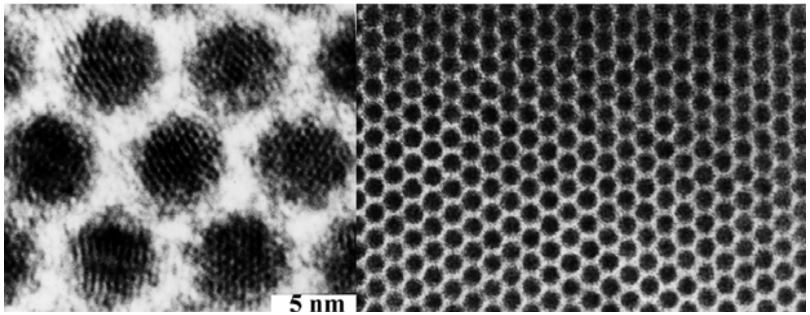
Courtesy of Intel Corp.

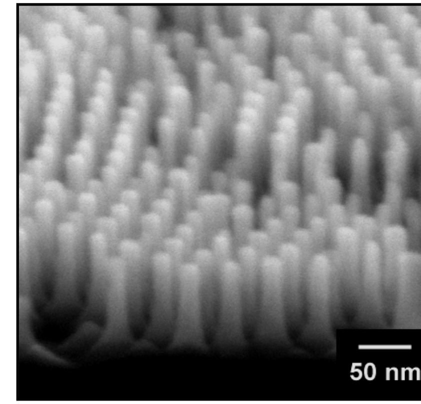
Nanotechnology

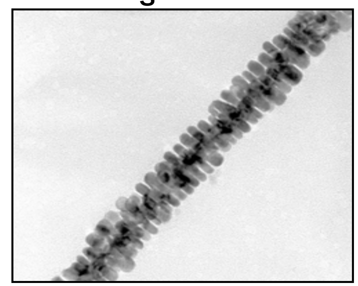




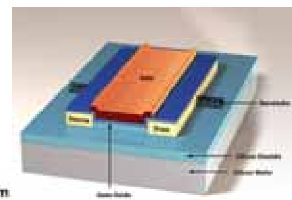


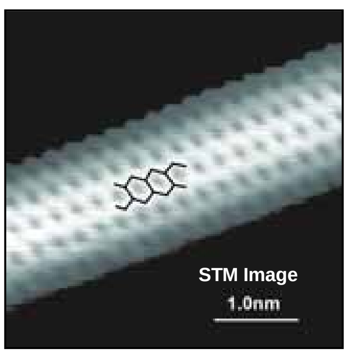


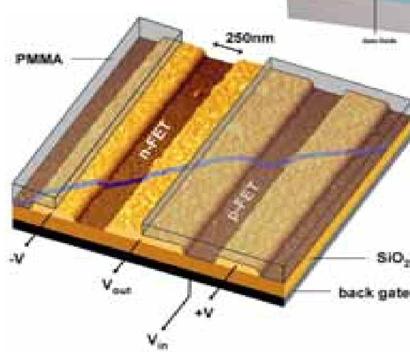


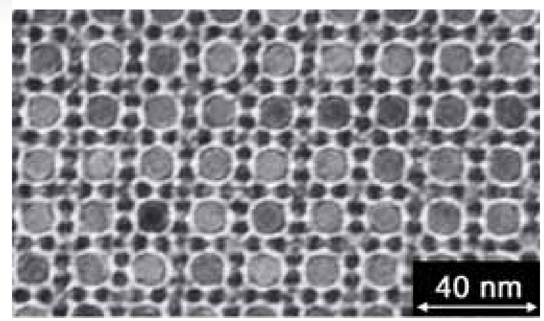


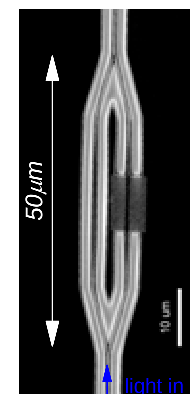
Figures courtesy of IBM Research

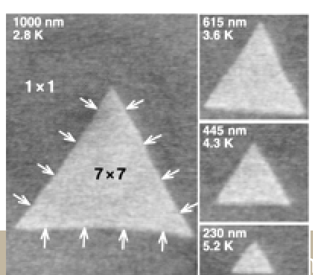


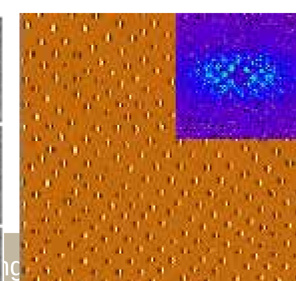


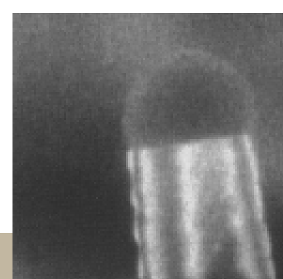


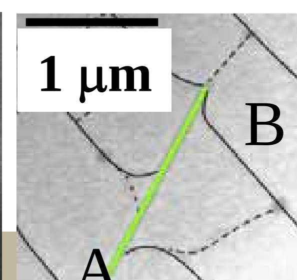


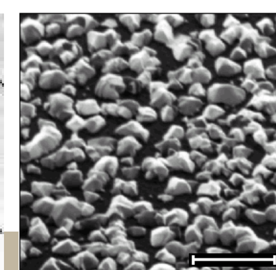


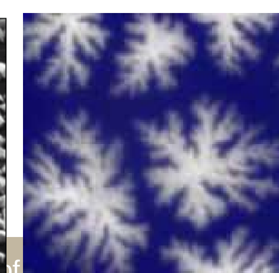




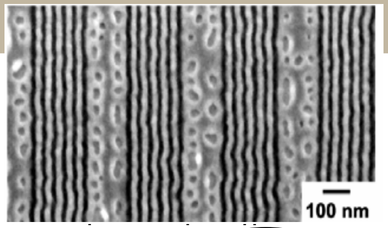


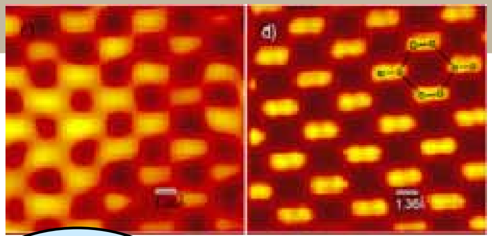






Nanotechnology

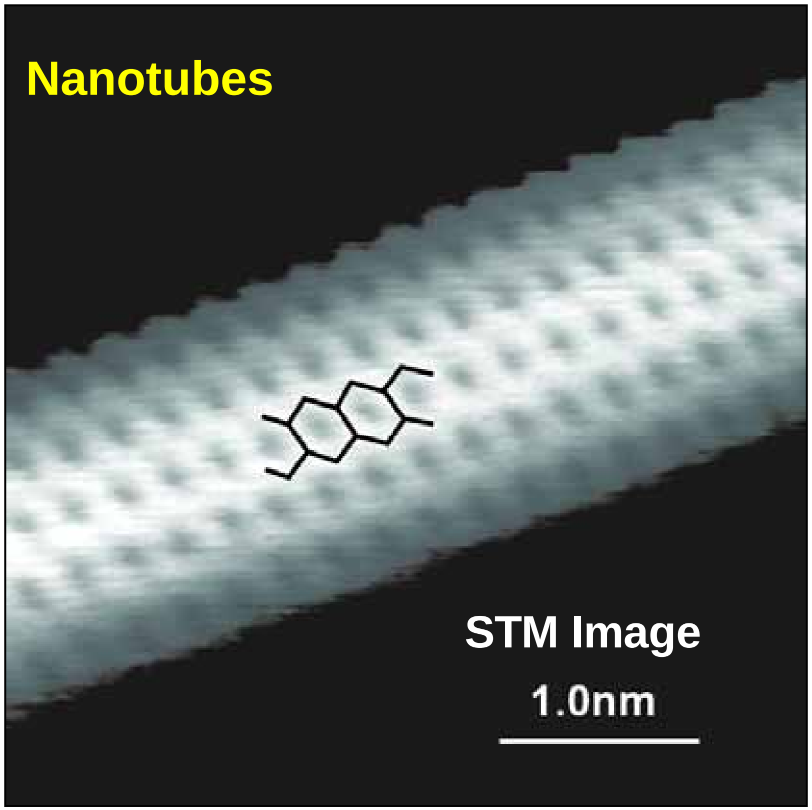


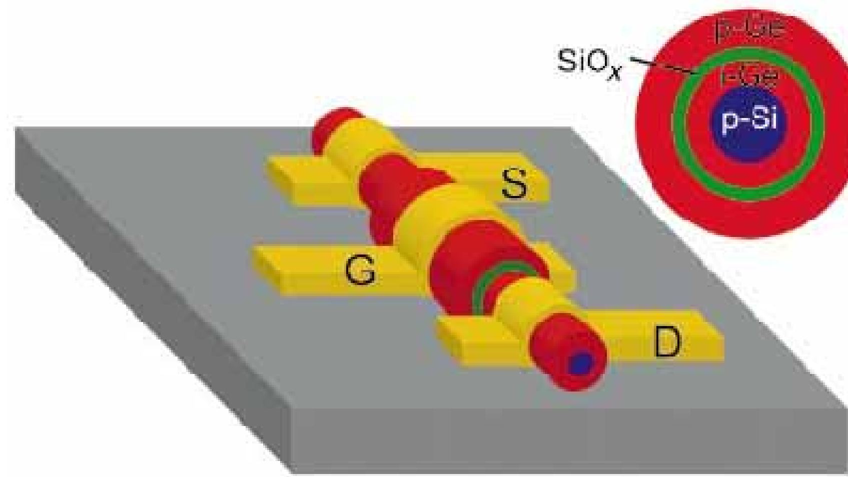


Key Challenges

- **Power / performance improvement and optimization**
- **Variability**
- **Integration**
  - Device, circuit, system

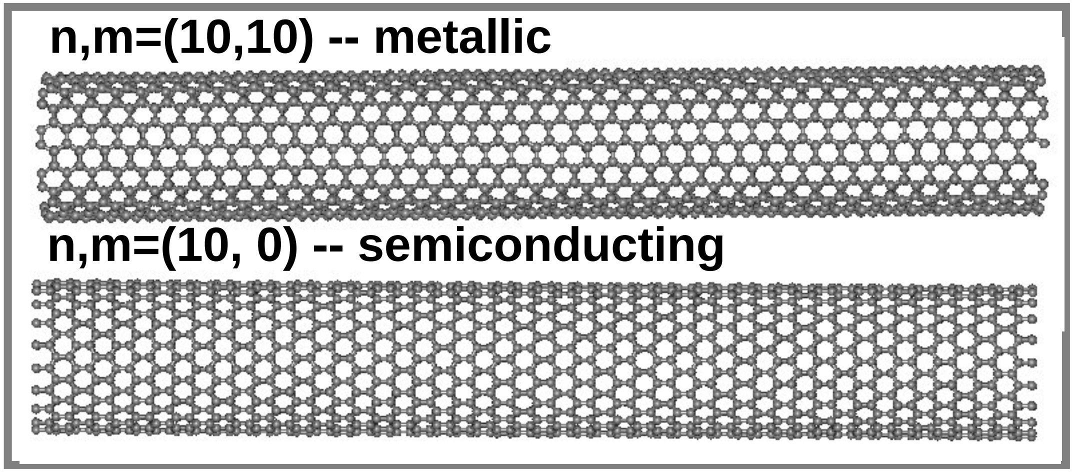
Nanotubes and Nanowires

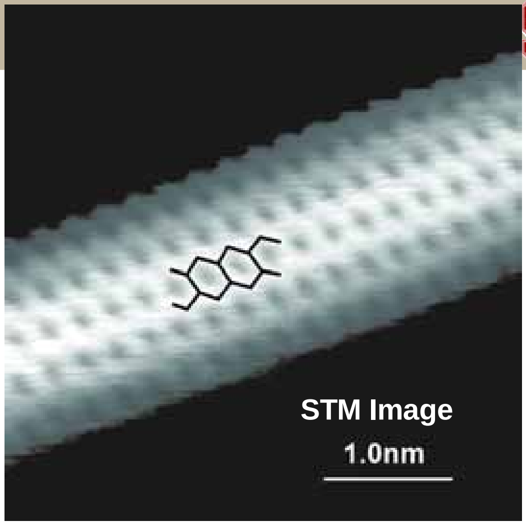




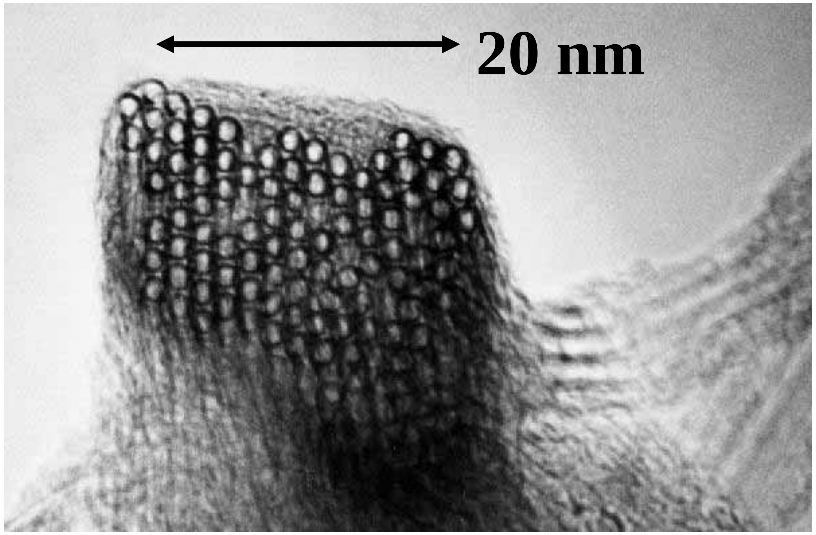
Nanowire

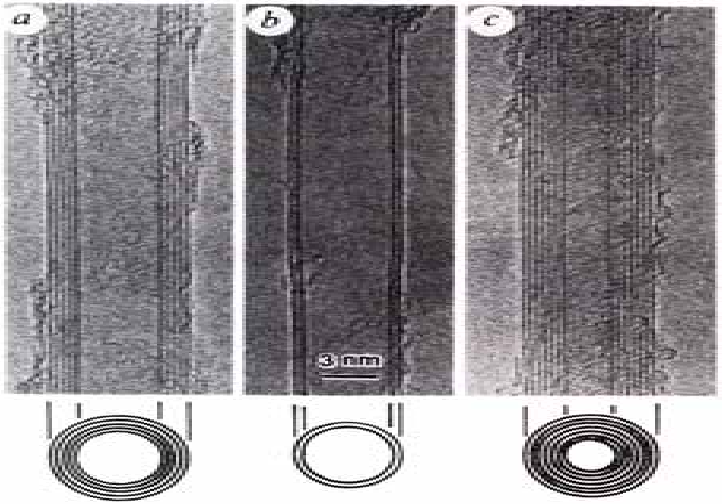
CNT Families and Structure





Diameter: ~1 nm
Length: several µm

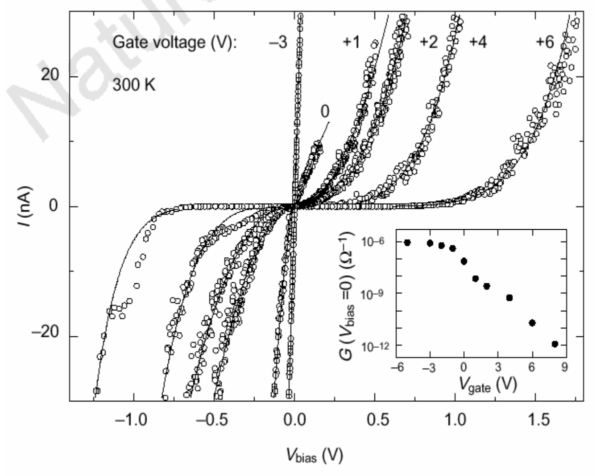




B.I.Yakobson and R.E.Smalley,American Scientist **85** (1997) 324

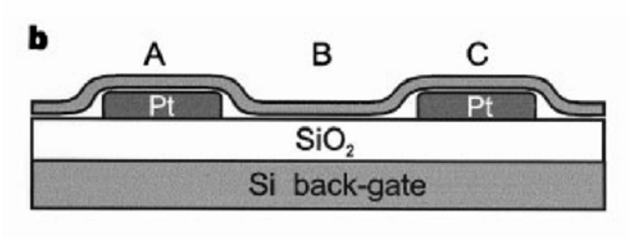
S.Iijima, Nature **354** (1991) 56

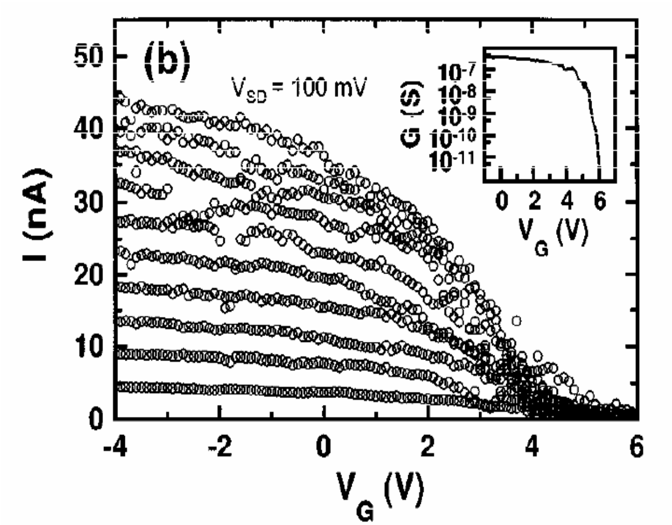
1998 Carbon Nanotube FETs



Tans *et al.* Delft University
Nature 393, 49 (1998)

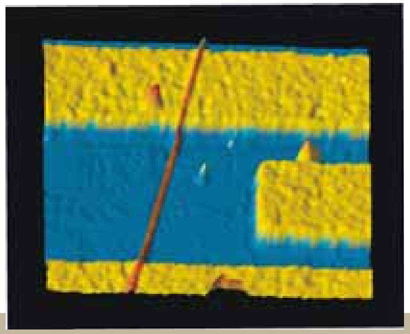
→ **P-type, high contact resistance**

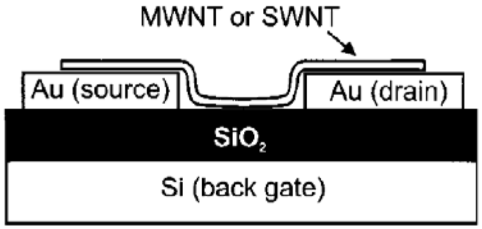




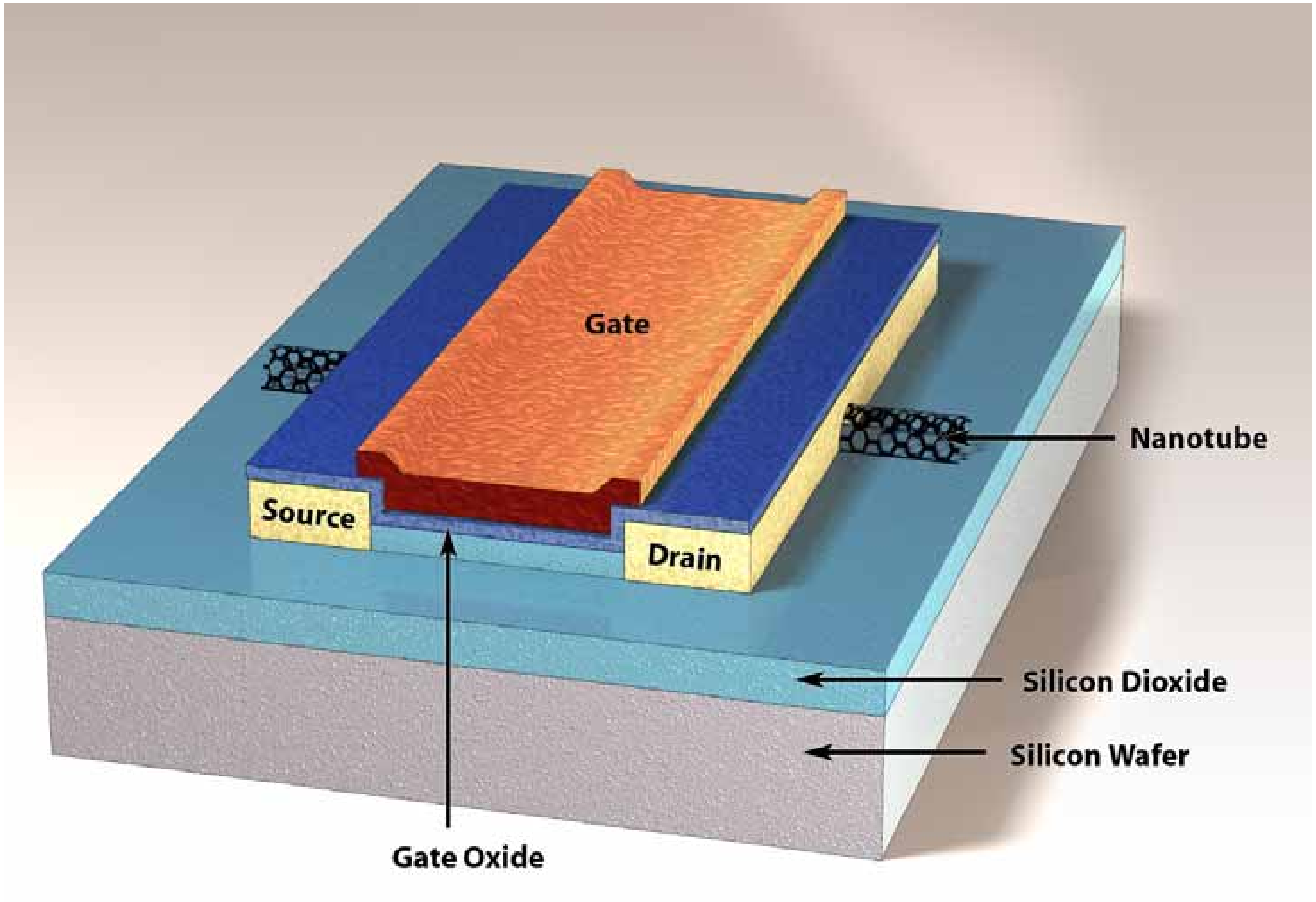
Martel *et al.* IBM
App. Phys. Lett. 73, 2447 (1998)

→ **P-type, high contact resistance**



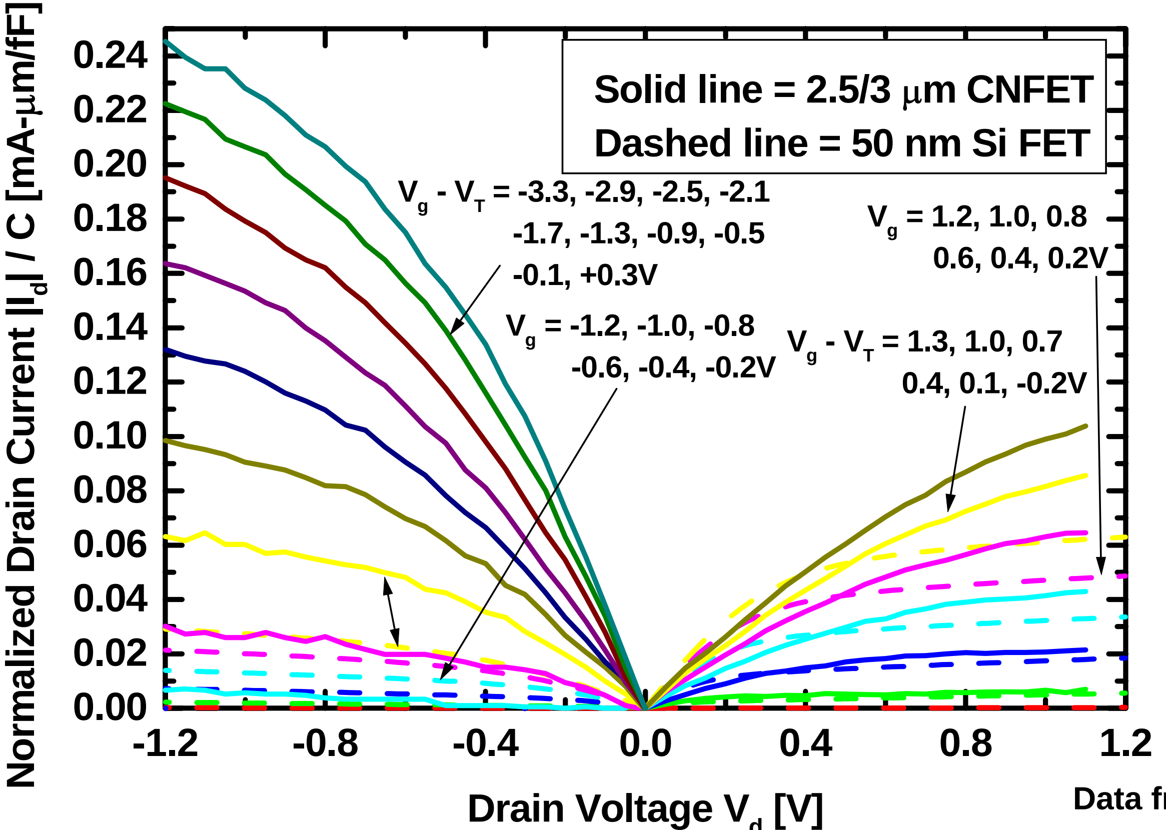


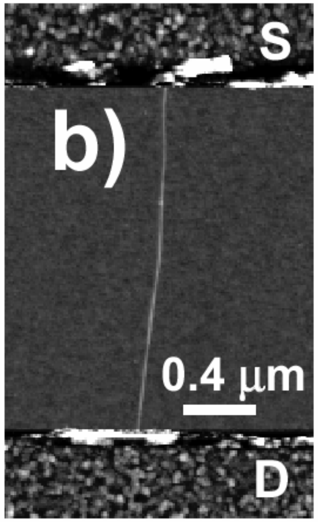
Carbon Nanotube FET



Carbon Nanotube FET

- Drain current normalized by gate capacitance



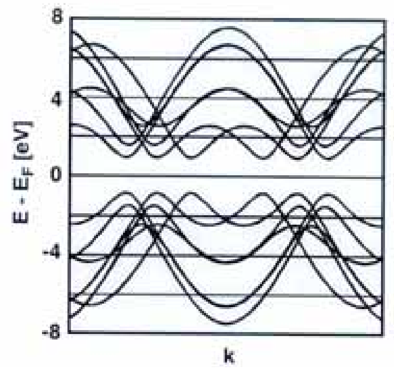


Data from:

S. Huang et al, *IEDM*, p. 237, 2001.

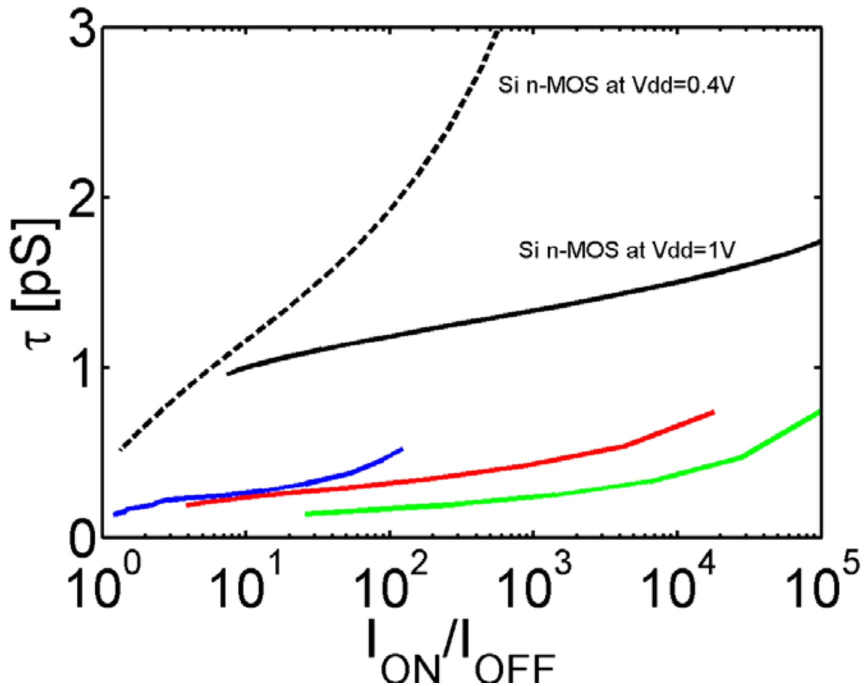
A. Javey et al., *IEDM*, p. 741, 2003.

Carbon Nanotube FET is Promising...



- CV/I, G_{msat}/C are comparable to or better than Si nFET
- Chemical synthesis controls a key dimension
  - think of this as an ultra-thin body SOI with body thickness and device width controlled to atomic precision
- Band structure of CNFET:
  - Symmetric band structure
    - electron and hole transport should be identical
    - balanced nFET and pFET
  - Thermal velocity / source injection velocity of CNFET higher than Si FET
  - However, density of states is lower - lower gate capacitance
- Carrier transport is one-dimensional - reduced phase space for scattering
- Wrap-around (“double”) gate - thicker gate oxide possible
- All bonds are satisfied, stable, and covalent
- Device is not “wed” to a particular substrate - 3D plausible
- Circuit design infrastructure preserved - no need to reinvent circuits

CNFET vs. Si MOSFET



CNTFETs (V_{DD} = 0.4V)

p-CNT MSDFET (Javey)

p-CNT MSDFET (projected)

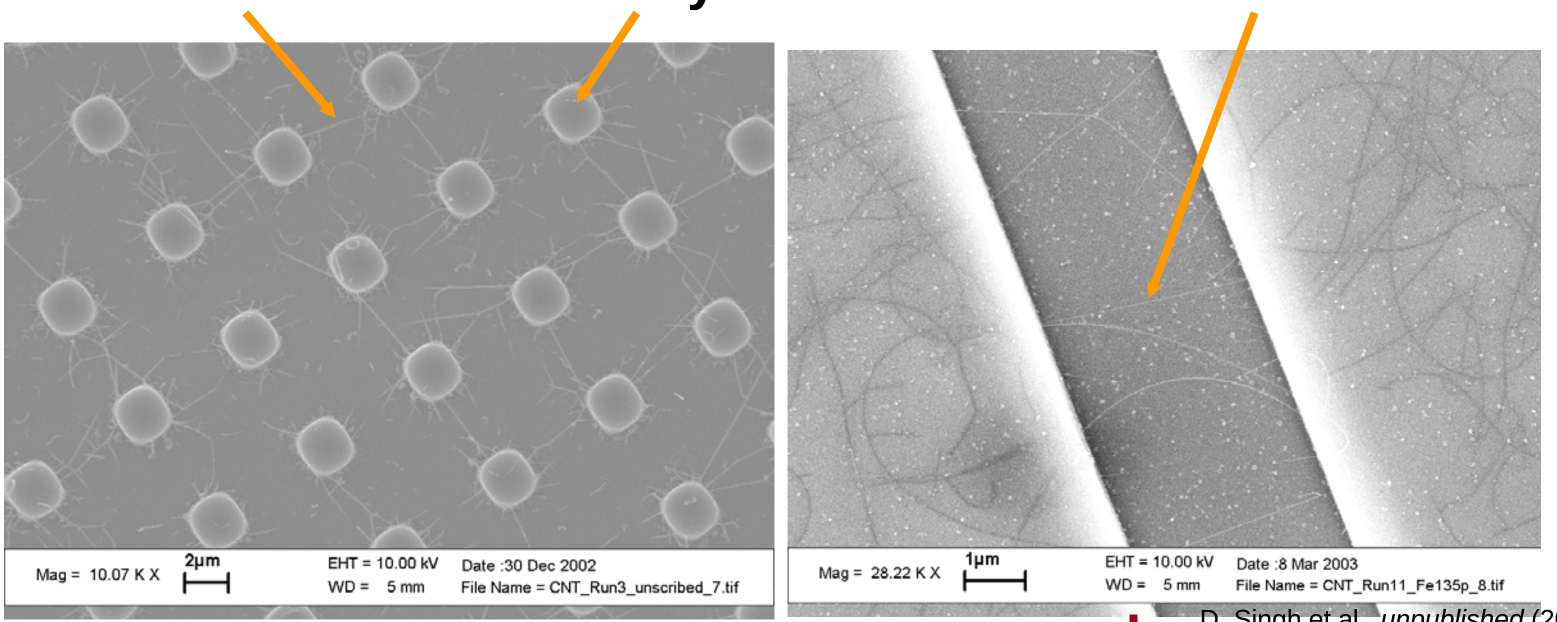
CNT MOSFET (projected)

Source: M. Lundstrom, *IBM Post-CMOS Deep Dive*, Sept 21-22, 2004.

Si n-MOS data is 70 nm L_G from 130 nm technology from Antoniadis and Nayfeh, MIT

Key Issue: Materials and Fabrication

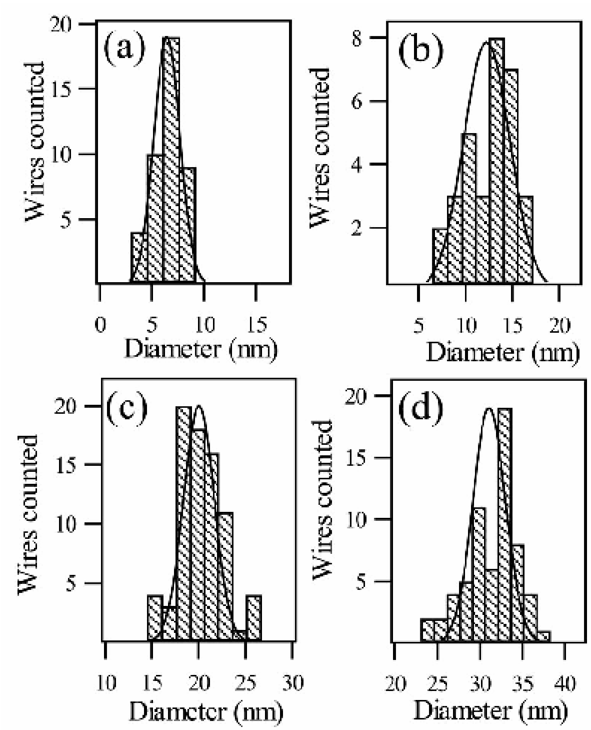
- Right kind of tube (electronic properties) at the right places (placement, orientation), doping
- Low parasitic capacitance/resistance, compact device (including isolation) structure
- Process compatibility with Si CMOS

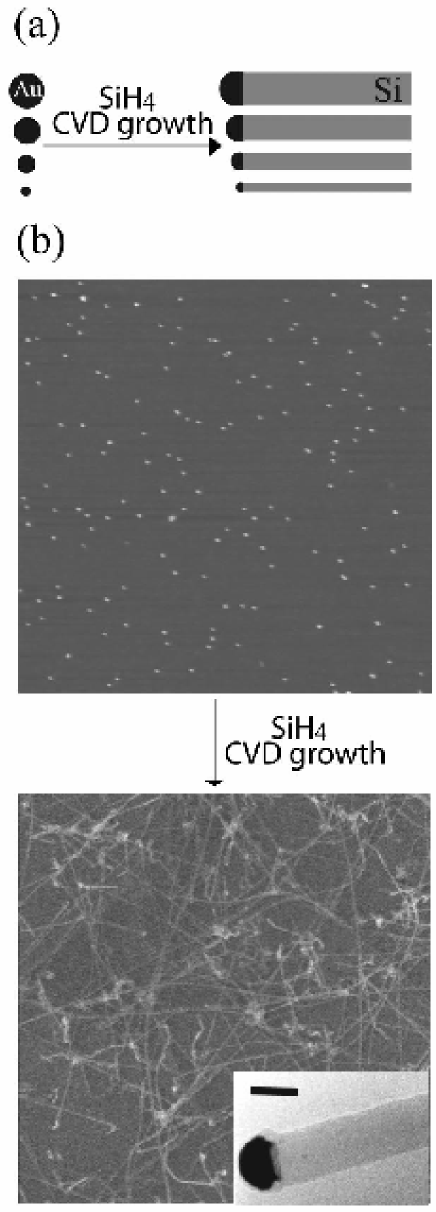


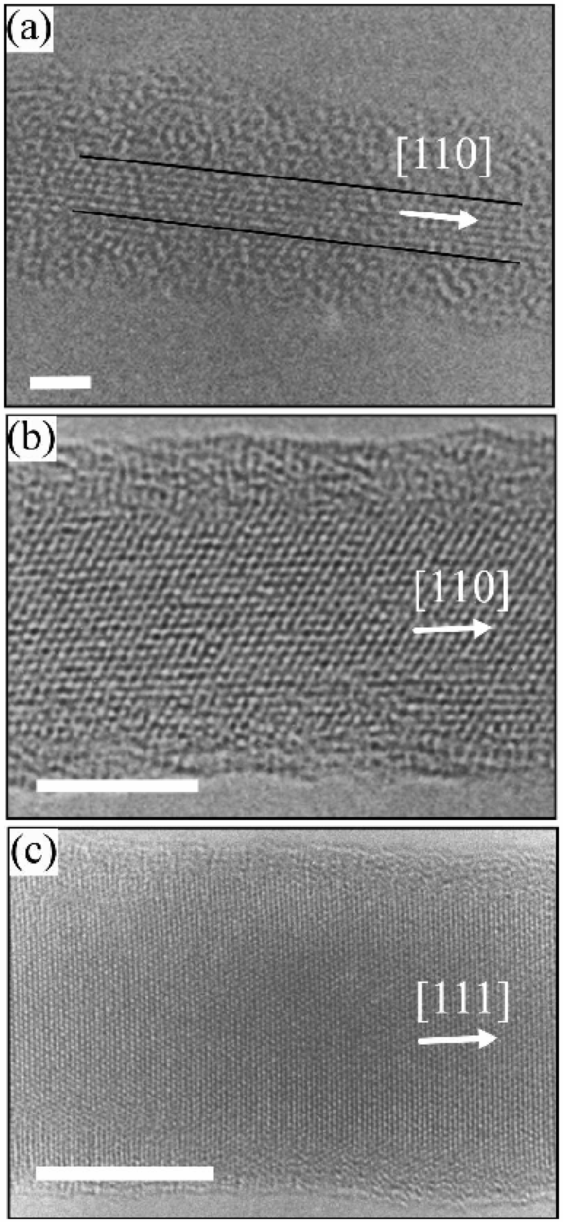
- D. Singh et al., *unpublished* (2003)

Si Nanowire Growth

- **Catalyst size controls nanowire size**







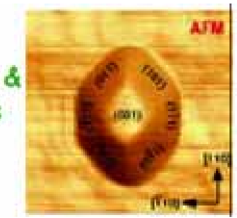
Y. Cui...C. Lieber et al., *Appl. Phys. Lett.*, 78, p. 2214 (2001)

Courtesy of Lars Samuelson, Lund University, 2004.

Nanowires – 3D Heterogeneous Integration Fabric

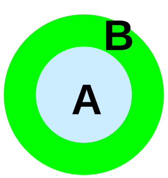
Formation of heterostructure interfaces between lattice mis-matched materials, e.g. InAs/GaAs (7%) & InAs/InP (3.5%): a comparison between 2D epitaxial growth and wire growth

Lattice mis-match → Growth by 2D epitaxy → SK-islands & dislocations



Wire geometry → 1D wire growth → Radial strain relaxation

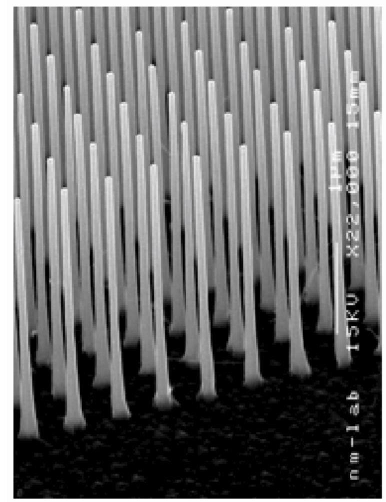
Switching of growth species in an optimal fashion allows abrupt interfaces to form



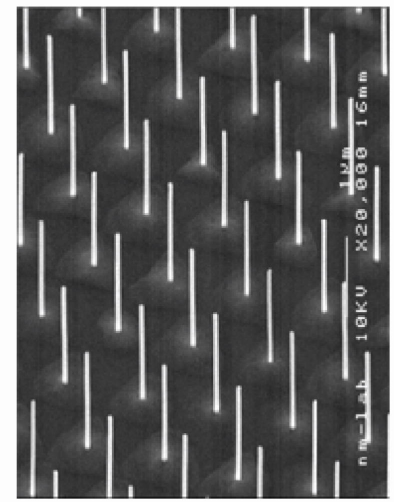
Core-shell

Axial hetero-epitaxy

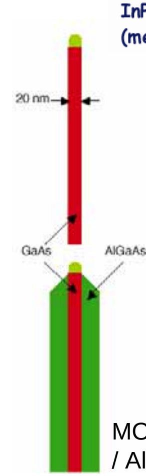
Growth from patterned catalysts



InP nanowire array grown by MOVPE (metal-organic vapor phase epitaxy)

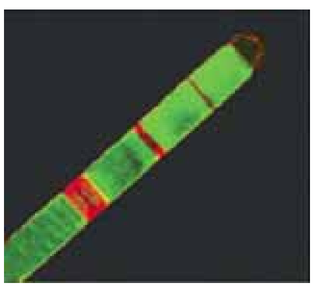


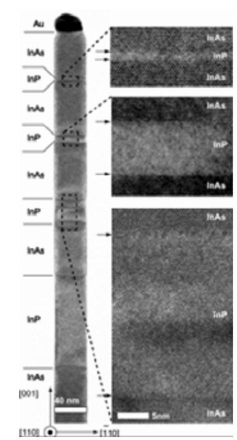
InAs nanowire arrays grown by CBE (chemical beam epitaxy)



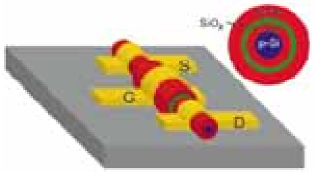
MOVPE growth of GaAs (core) / AlGaAs (shell) nanowire

InP/InAs nanowire

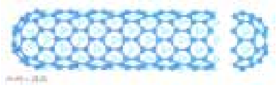




1D Channel FET:



Nanowire



Nanotube

- **1D semiconductors (nanotube, nanowire)**
  - Chemical synthesis controls the critical dimension (reduces variation due to quantum confinement)
  - Self-assembly or directed growth – new manufacturing methods
  - Nanowire (Si, Ge, III-V, II-VI) is the next logical step after Si FinFET
    - Bandgap engineering and strain engineering tricks still possible
    - Both lateral (along axis) and radial (core-shell) engineering possible
  - Excess noise for 1D conductors may be problematic – needs study

Nanotubes and Nanowires

- **Net: basic science has progressed to a level where engineering work is feasible**

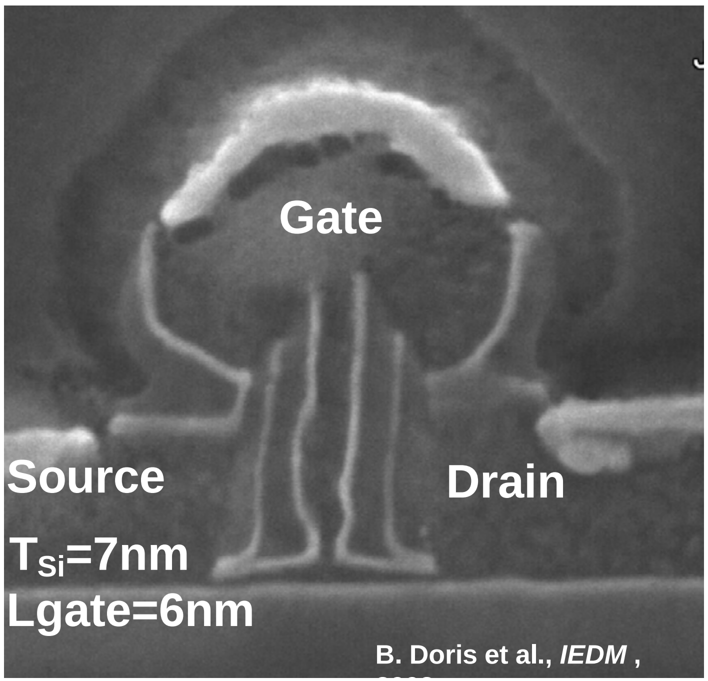
Molecular Electronics

As defined by the conceptual creators Aviram and Ratner [1], molecular electronics is the "study of molecular properties that may lead to signal processing" [2]. However, making molecular electronics into a functioning, manufacturable technology will require revolutions in circuit architecture, fabrication, and design philosophy in addition to gaining a fundamental understanding of conduction and electronic interactions in single molecules.

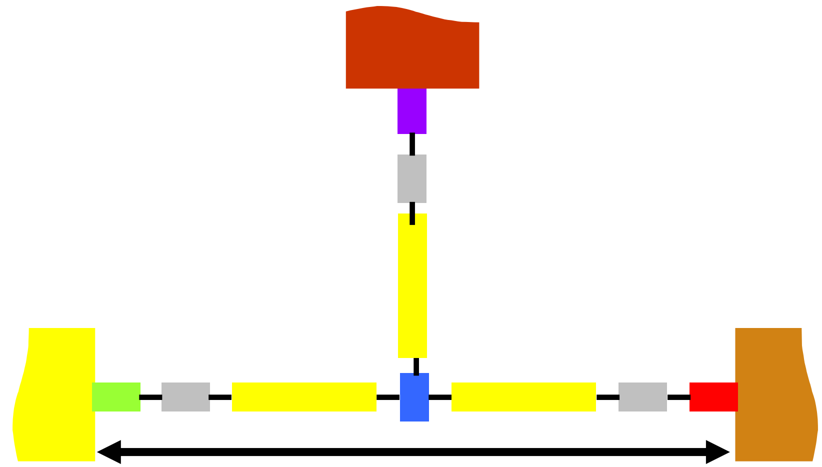
B. Mantooth, P. Weiss, *Proc. IEEE*, 91, p. 1785 (2003)

Molecules = Small ?

Si FET



Molecular Device



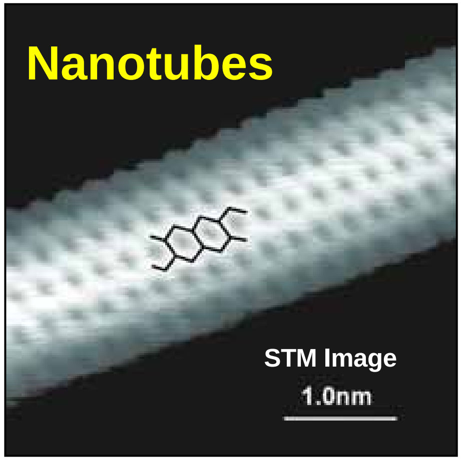
L >2.5 – 3 nm

- **All devices are governed by electrostatics and eventually limited by tunneling**

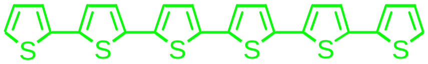
- difficult to be much smaller than 2 - 3 nm

Molecules

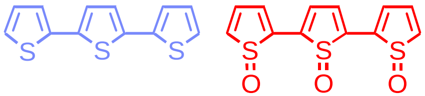
Lower manufacturing cost
New functionality



Organic Systems



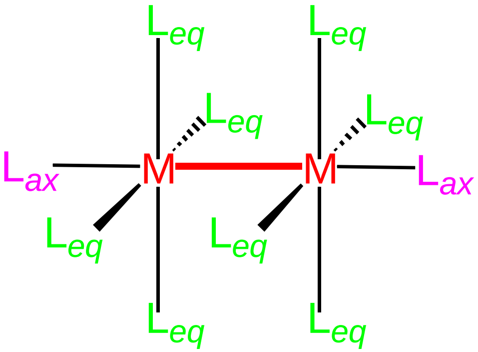
Wires



Donor   Acceptor

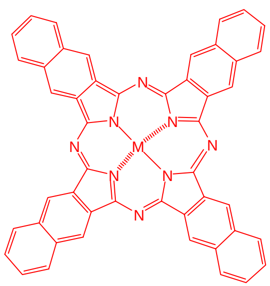
Bridges

Metal-metal bonded supramolecules

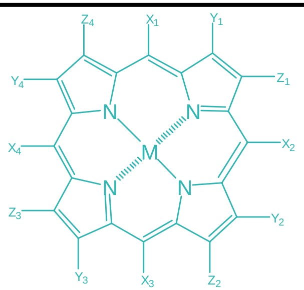


M = V, Nb, Cr, Mo, W, Tc, Re, Fe, Ru, Os, Co, Rh, Ir, Ni, Pd, Pt, Cu, Ag …

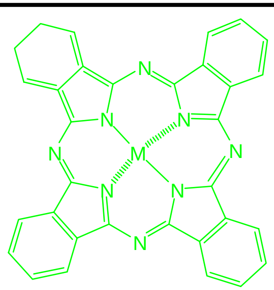
Ligands chosen to tailor:
- **Electronic coupling between dimetal units**
- **Electrochemistry**
- **Solubility**
- **Structure ….**



Naphthalocyanine



Porphyrin



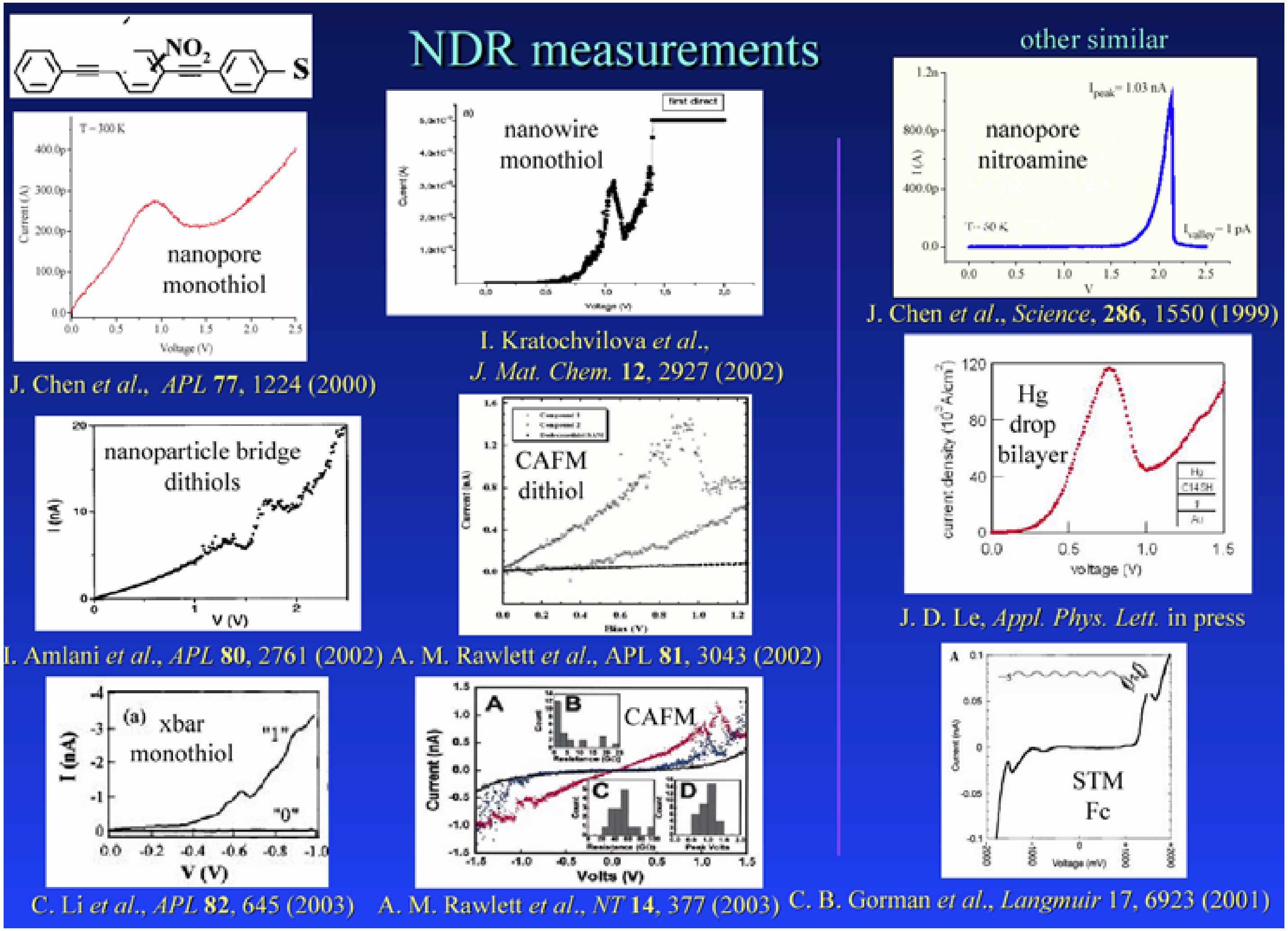
Phthalocyanine

- **tailor metal center**
- **tailor ligands off peripherary**
- **link to form chains or onto surfaces**
- **stack vertically**

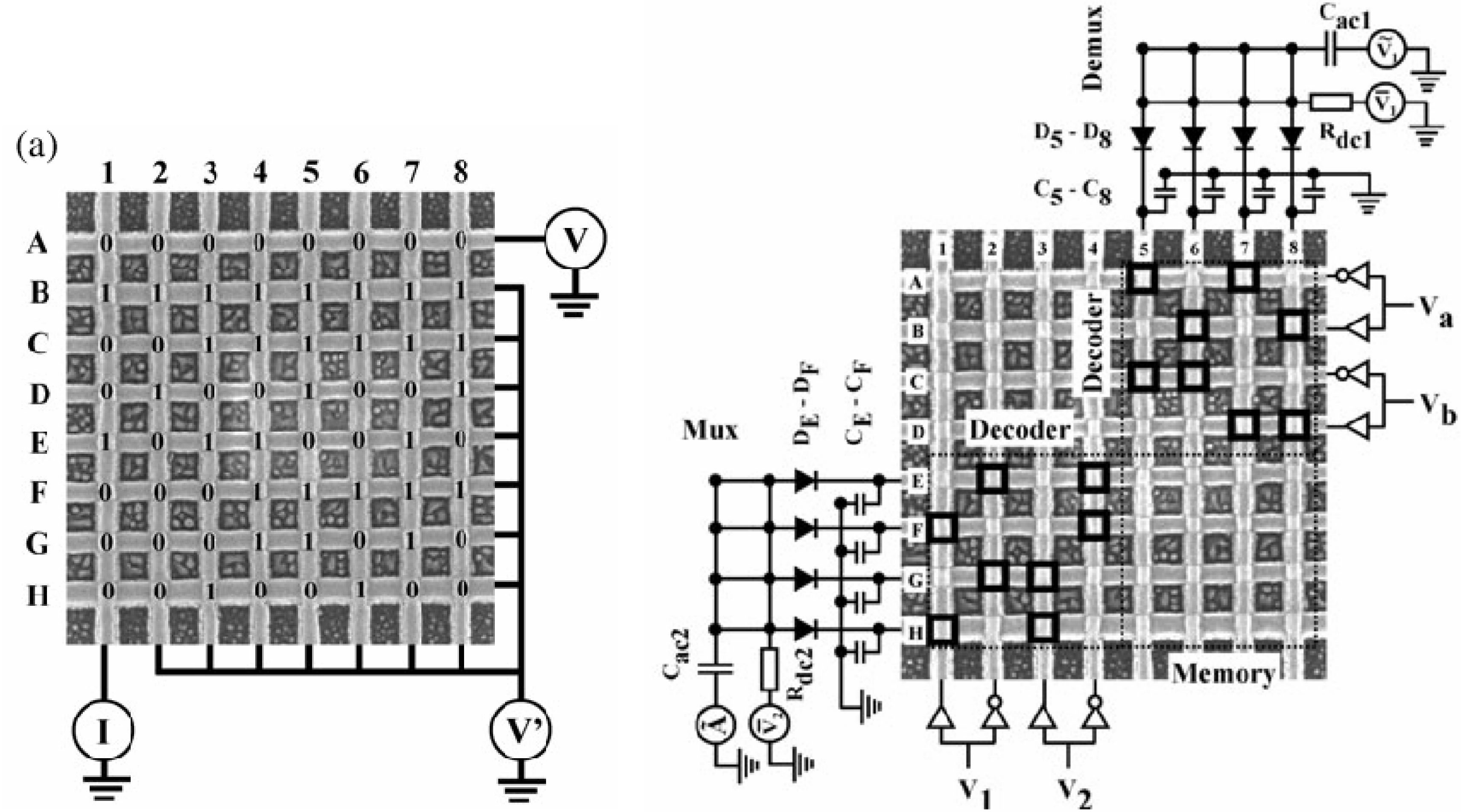
Organo-metallic
Akin to Biological Systems

M. Reed, NNI/SRC Workshop on *Silicon Nanoelectroincs and Beyond*, Oct 2003.

Two-Terminal Electrical Measurements

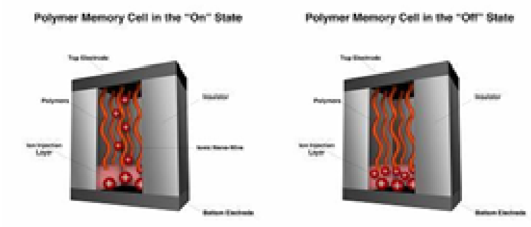


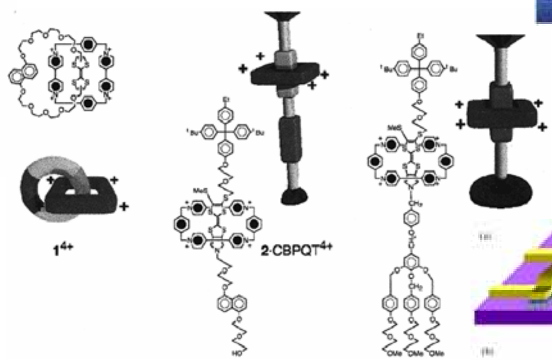
Molecular Memory and ROM-Based Logic

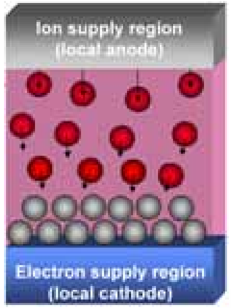


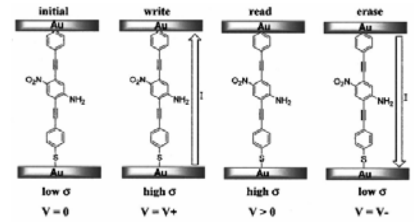
Y. Chen...J.F. Stoddart, R.S. Williams et al., *Nanotechnology*, 14, p. 462 (2003)

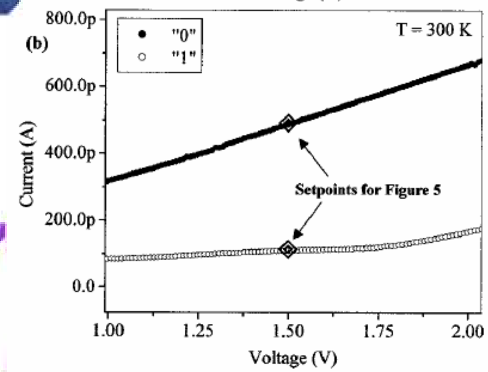
Hysteresis – A Dime a Dozen

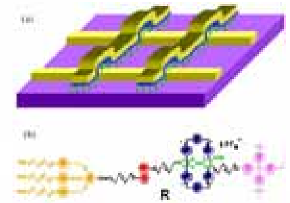


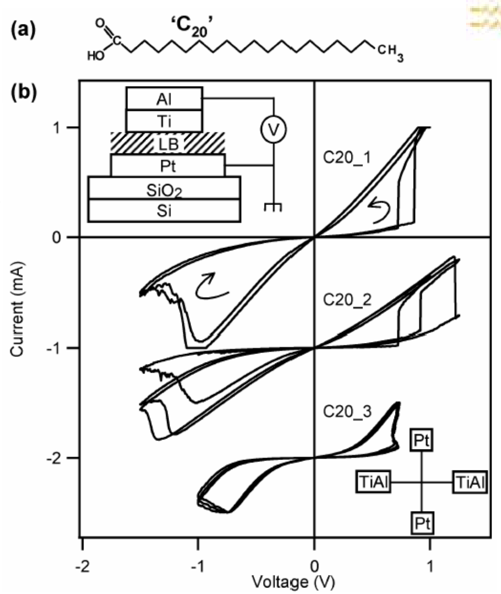


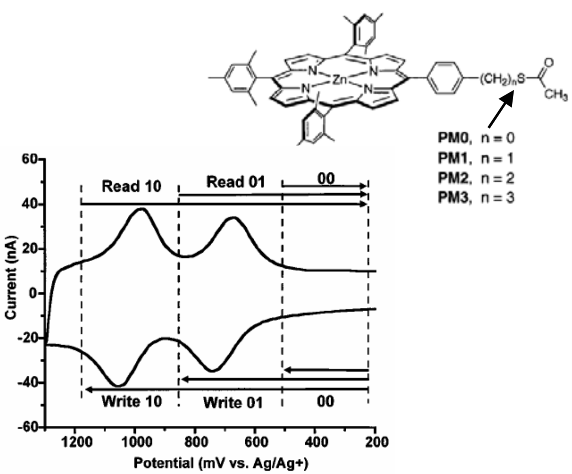


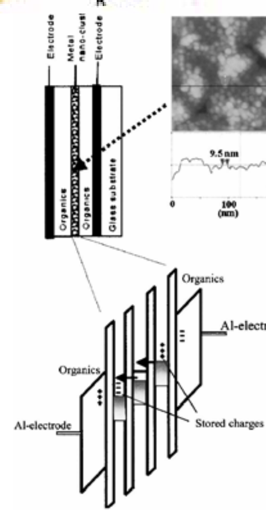


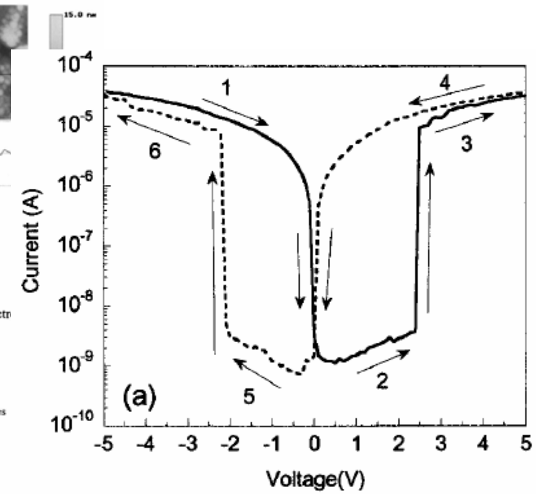










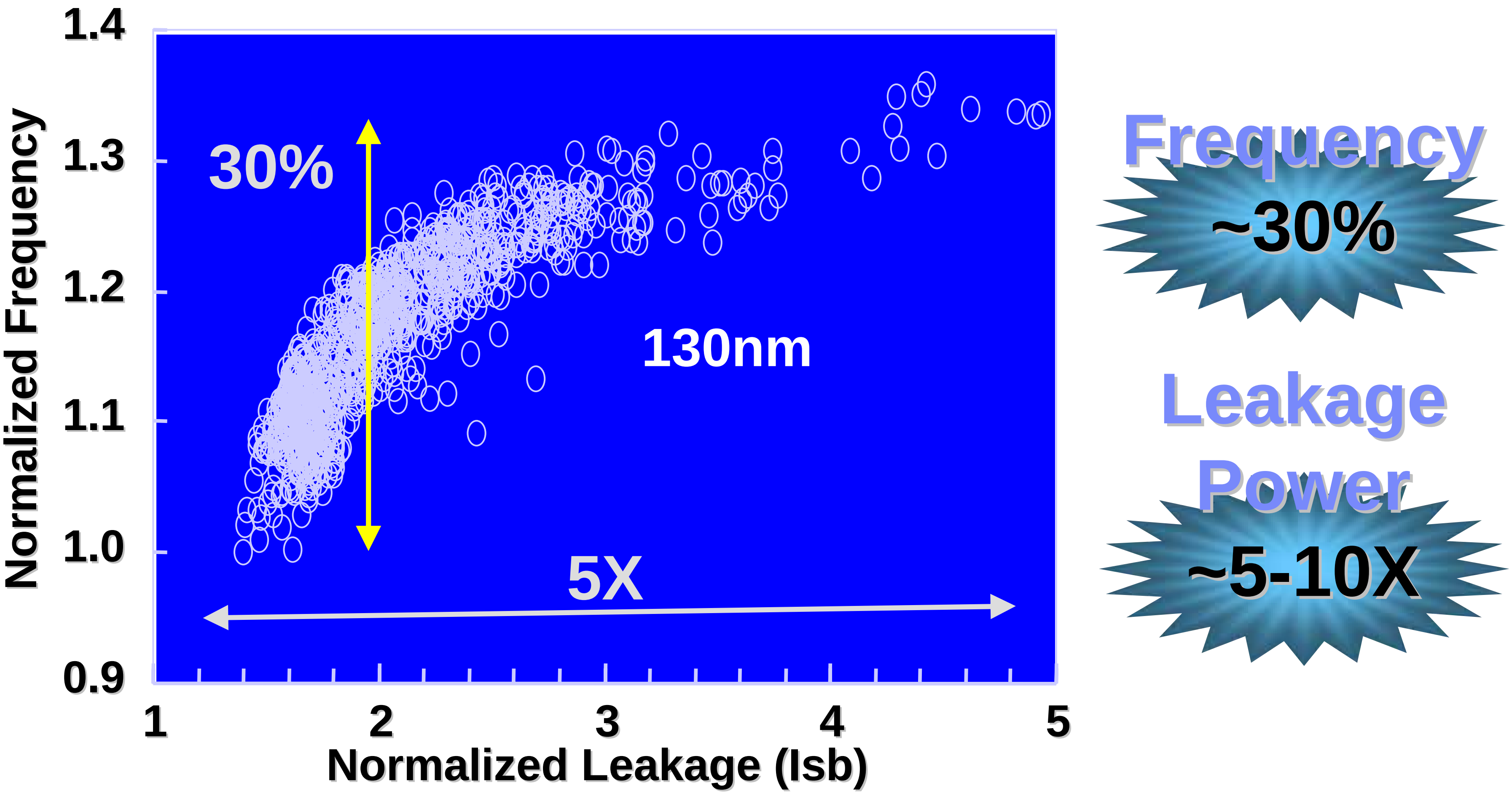


Key Challenges

- **Power / performance improvement and optimization**
- **Variability**
- **Integration**
  - Device, circuit, system

Nanomaterials

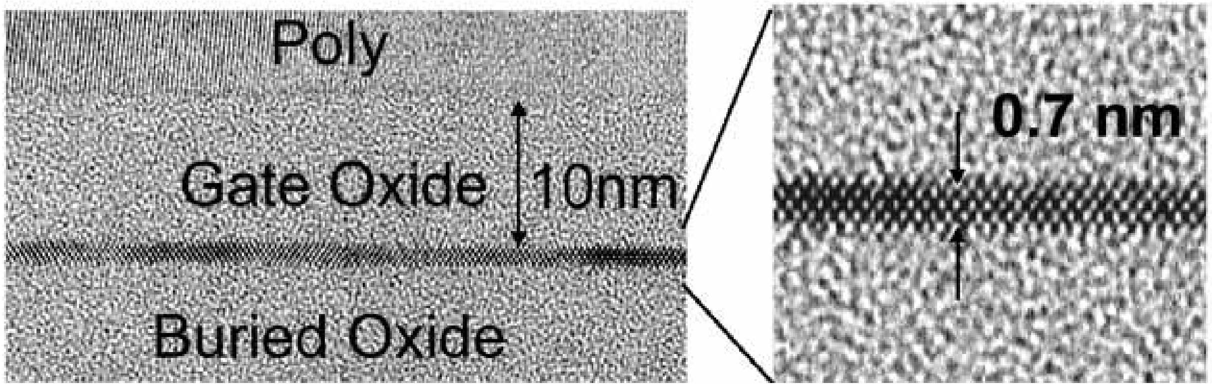
Impact of Statistical Variations



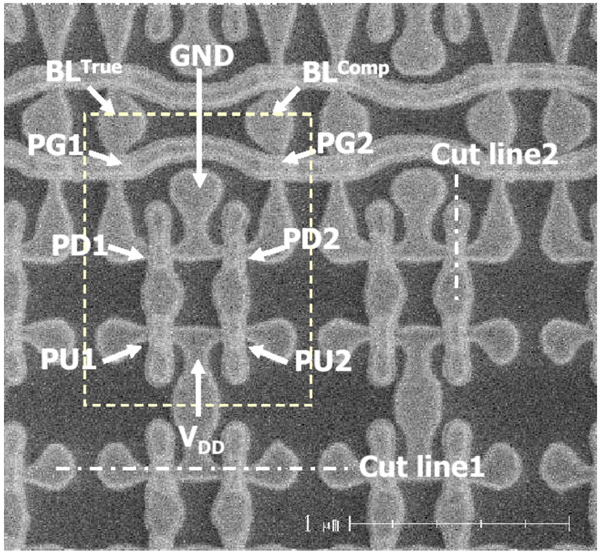
Courtesy of Intel Corp.

P. Gelsinger, *41st Design Automation Conference (DAC)*, June 8, 2004.

Can These be Fabricated for 10 nm FET ?



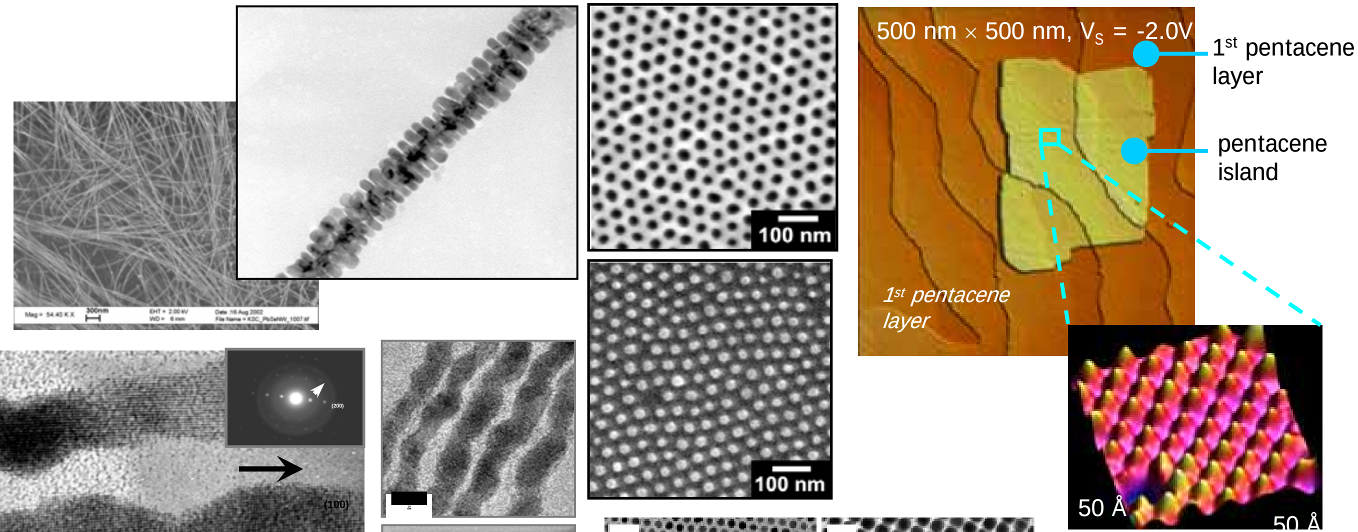
Source: Toshiba,
K. Uchida et al., *IEDM* 2003

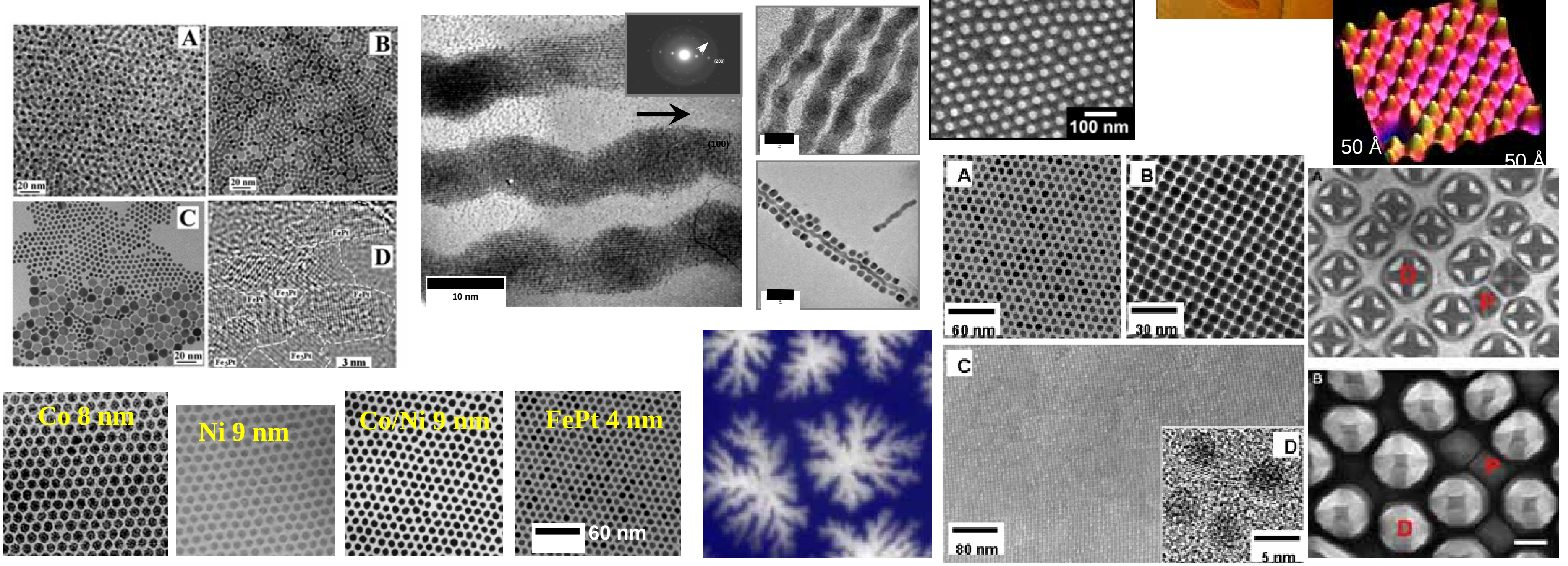


Source: Samsung
J.-H. Yang et al., *IEDM* 2003

Nanomaterials

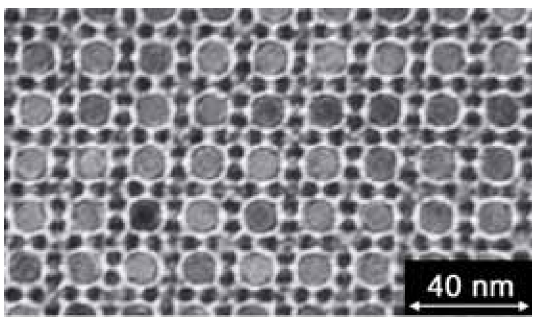
Courtesy of IBM Research

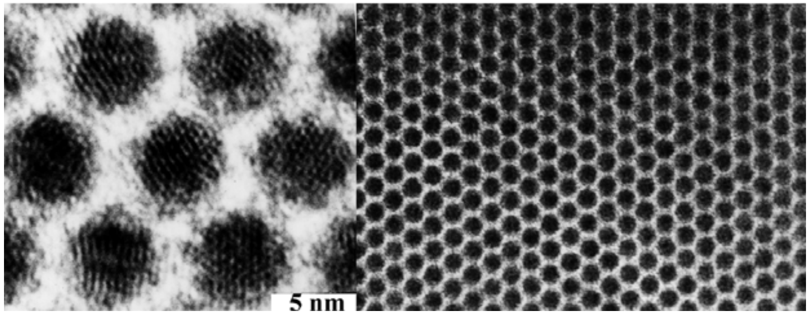




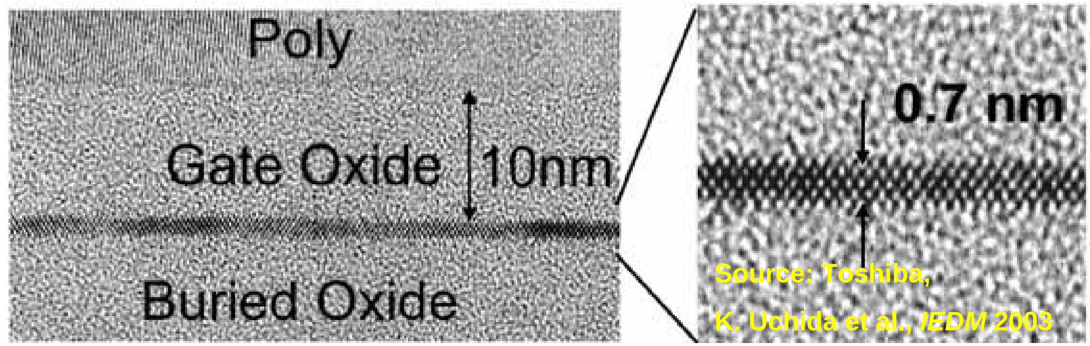
Nano for Si Technology – Nano, Now !

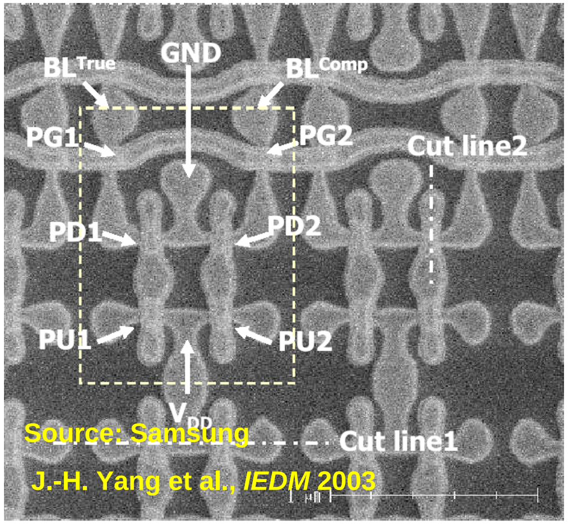
Use techniques that produce these:





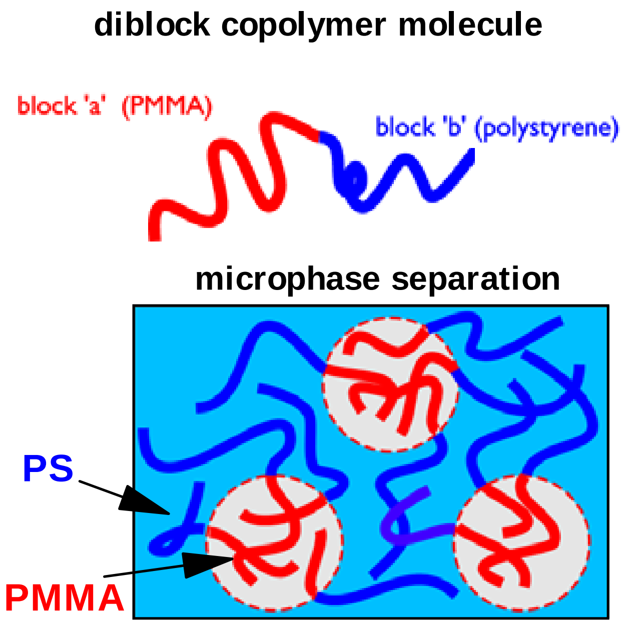
To make these structures

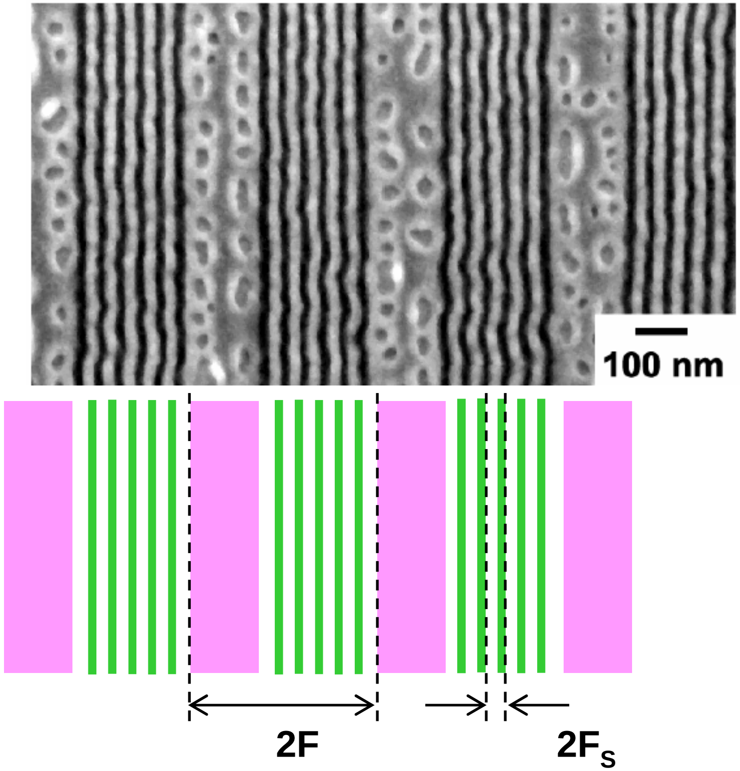




Lithography Subdivision

- Templated assembly of nanostructures
- Combines top-down lithography with bottom-up assembly
- Provides feature registration with larger, irregular features



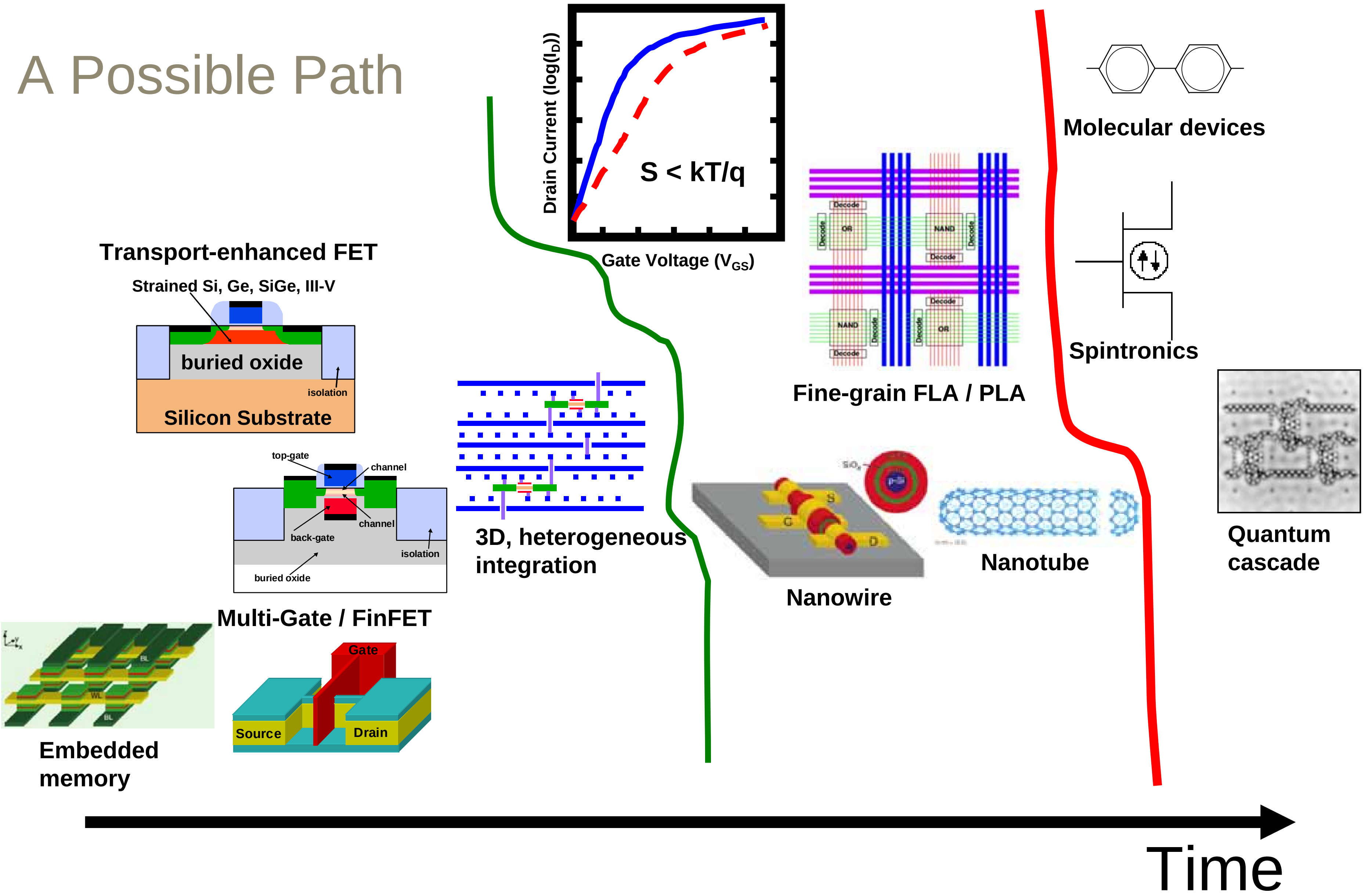


C. Black et al., *IEEE Trans. Nanotechnology*, p. 412 (2004).

Metrology and Characterization

- **Cannot manufacture if we cannot measure what we make**
- **Wish list**
  - Fast AFM
    - The equivalent of the CD SEM
  - Defect recognition for new materials
    - nanotube, nanowire, organic molecules
  - Defect repair
  - Characterization methods for soft materials

A Possible Path



Questions? Please contact:

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