Semiconductor Research Corporation

PIONEERS IN COLLABORATIVE RESEARCH®

NRI nanoelectronics RESEARCH INITIATIVE

Overview of the Nanoelectronics Research Initiative:

An Industry-Government-University Innovation Partnership

Dr. Jeff Welser
Director, SRC Nanoelectronics Research Initiative
IBM Almaden Research Center

May, 2009

Semiconductor Research Corporation

A Family of Distinct, Related Program Entities

Global Research Collaboration

Ensuring vitality of current industry

Focus Center Research Program

Breaking down barriers to extend CMOS to its limits

Nanoelectronics Research Initiative

Beyond CMOS –identify next information element

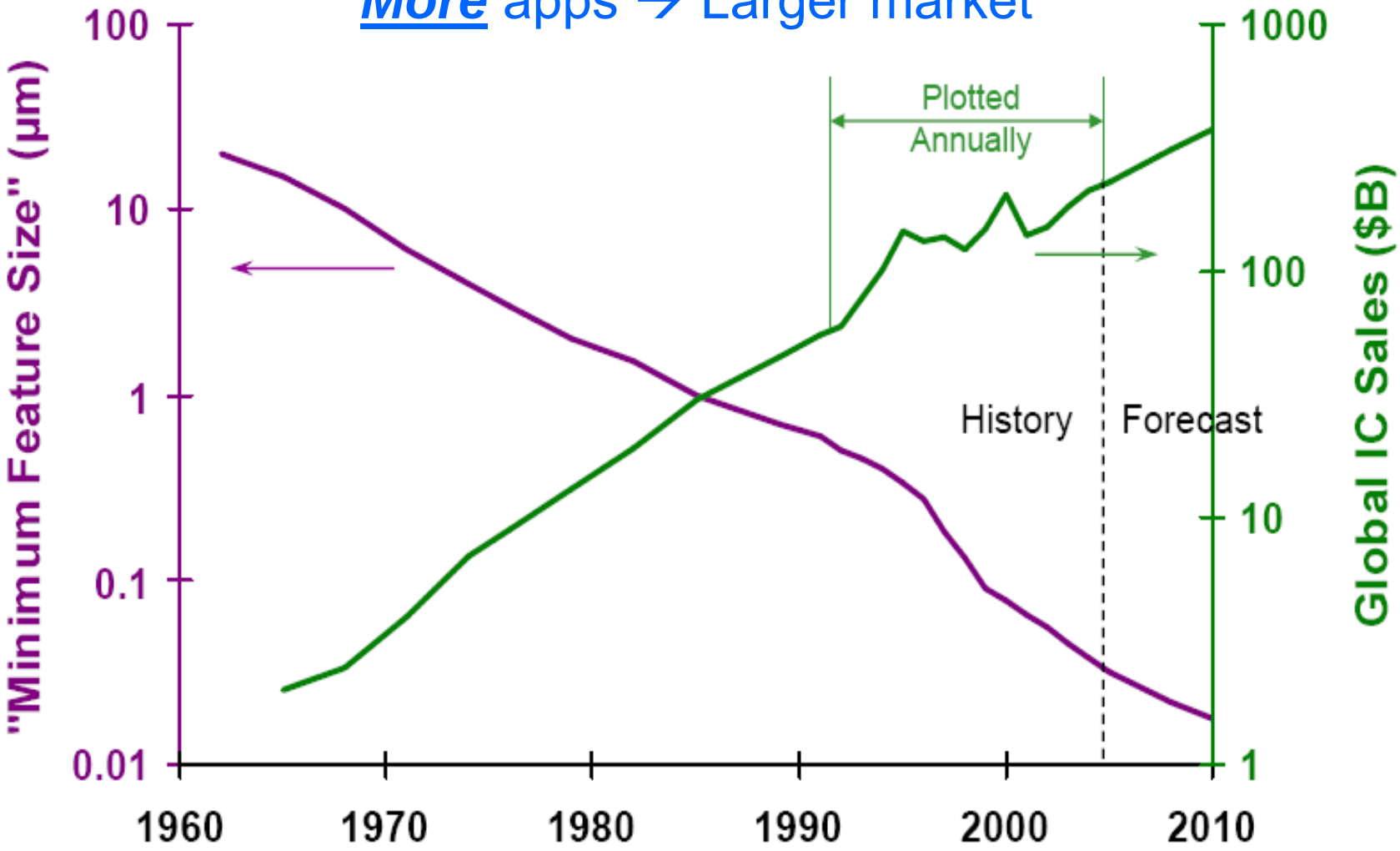
Attracting and educating the next generation of innovators and technology leaders

Topical Research Collaborations

Topic(s) chosen by participants

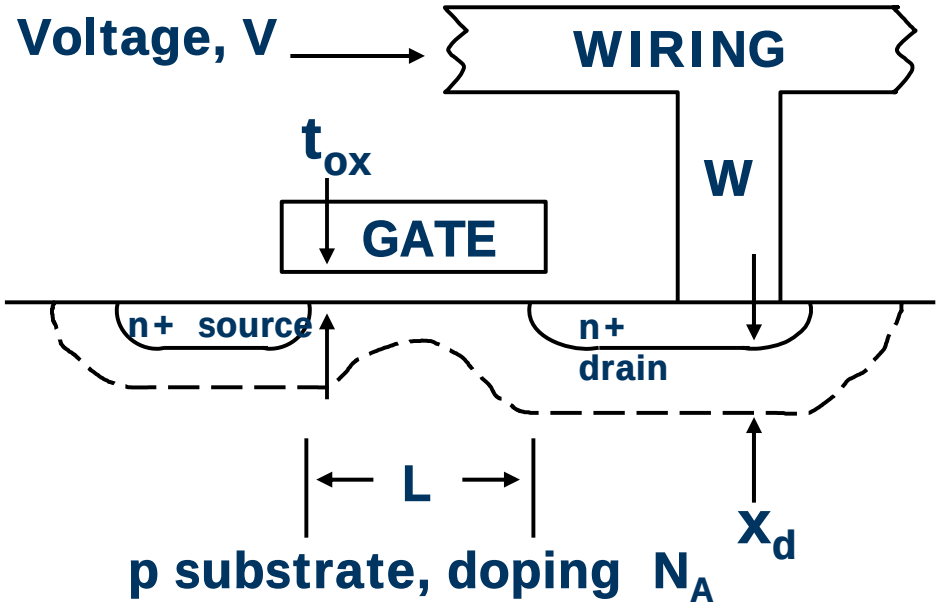
Scaling *Drives* the Industry

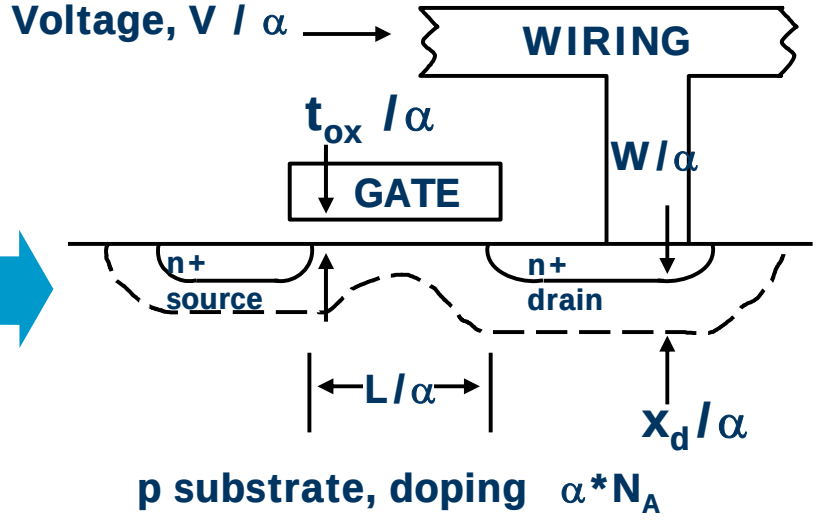
Smaller features → Better performance & cost/function → ***More*** apps → Larger market

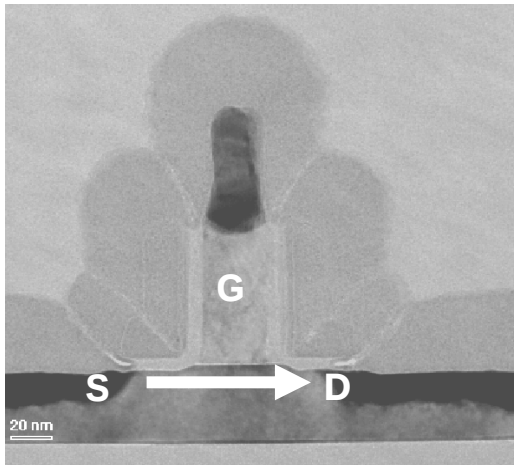


Transistor Scaling

Dennard, et al., 1974







RESULTS:

Higher Density:	α^2
Higher Speed:	α
Lower Power:	$1/\alpha^2$
per circuit	
Power Density:	**Constant**

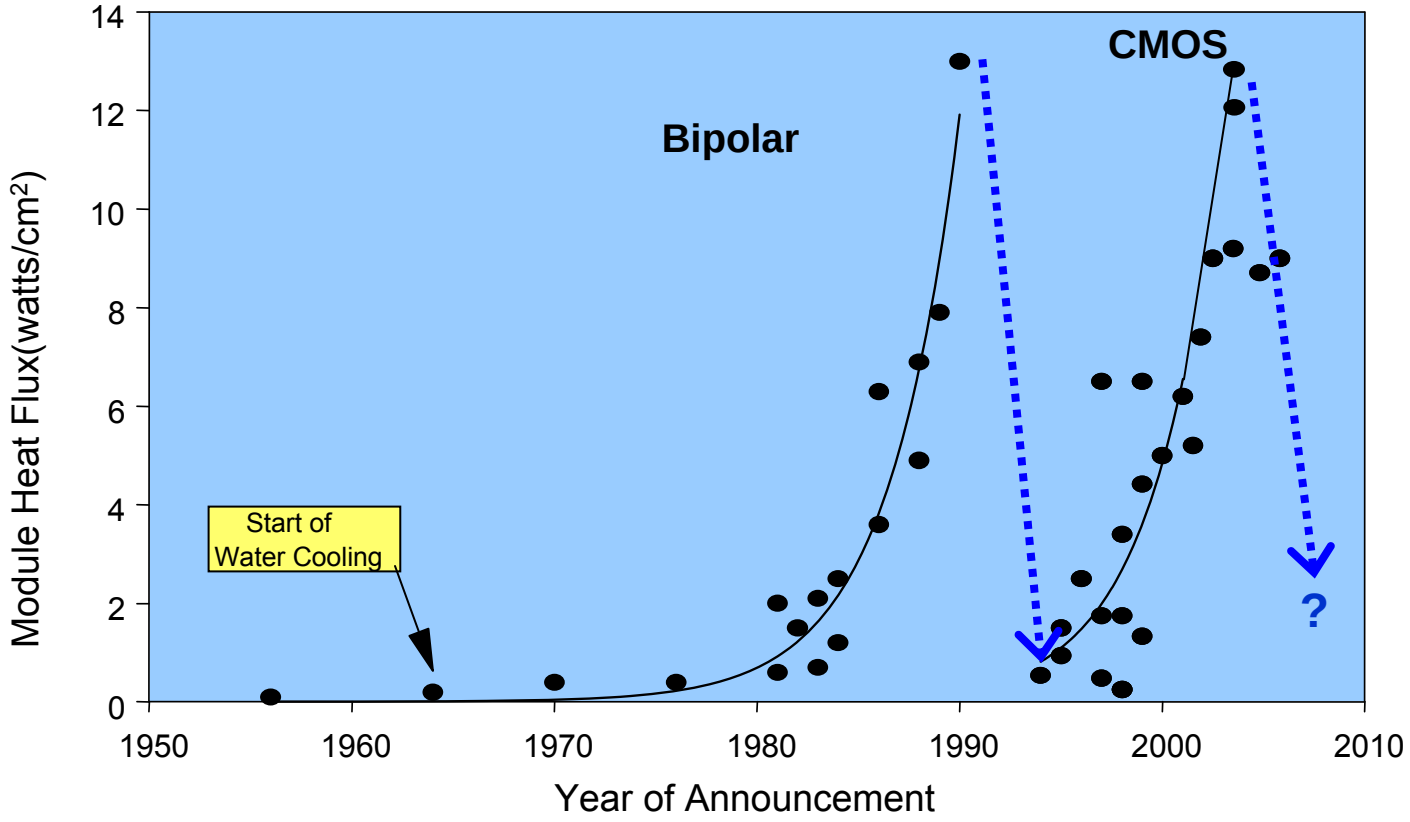
Implications for Nanoelectronics Circuits

- **Circuit heat generation is the main limiting factor for scaling of device speed and switch circuit density**

- Scaling to molecular dimensions may not yield performance increases
  - We will be forced to trade-off between speed and density
- Optimal dimensions for electronic switches should range between 5 and 50 nm
  - Likely achievable with Si – easily within the scope of ITRS projections
- Going to other materials for FETs will likely achieve only "one-time" percentage gains

➢ ***Need a new device mechanism or computation architecture to enable a new scaling path***

Has This Ever Happened Before?



- 2005 ~ 2015: New technology enhancements
  - Continued CMOS shrinking, multi-core chips, 3D packaging, new memory devices, etc.
- > 2015? : New device? → NRI's Goal

NRI Mission Statement

- **NRI Mission: Demonstrate novel computing devices capable of replacing the CMOS FET as a logic switch in the 2020 timeframe.**
  - These devices should **show significant advantage over ultimate FETs** in power, performance, density, and/or cost to enable the semiconductor industry to **extend the historical cost and performance trends** for information technology.
  - To meet these goals, NRI pursues **five research vectors**, focused on discovering and demonstrating new devices and circuit elements for doing computation.
  - Finally, it is desirable that these technologies be **capable of integrating with CMOS**, to allow exploitation of their potentially complementary functionality in heterogeneous systems and to enable a smooth transition to a new scaling path.

Beyond CMOS Logic: What to look for?

- **To beat the power problem requires:**
  - **A device with a lower energy, room temperature switching mechanism**

    or
  - **A system that operates out of equilibrium or recovers operation energy as part of the logic computation**

- **Required characteristics:**
  - **Scalability**
  - **Performance**
  - **Energy efficiency**
  - **Gain**
  - **Operational reliability**
  - **Room temp. operation**

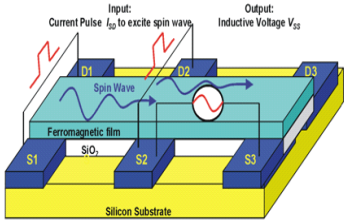
- **Preferred approach:**
  - **CMOS process compatibility**
  - **CMOS architectural compatibility**

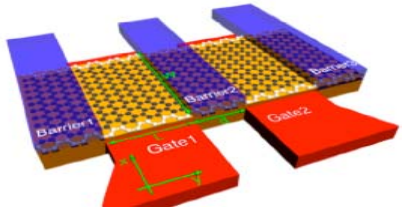
Alternative state variables

- **Spin–electron, nuclear, photon**
- **Phase**
- **Quantum state**
- **Magnetic flux quanta**
- **Mechanical deformation**
- **Dipole orientation**
- **Molecular state**

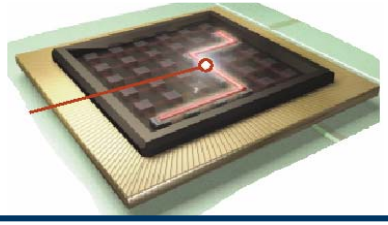
NRI Primary Research Vectors

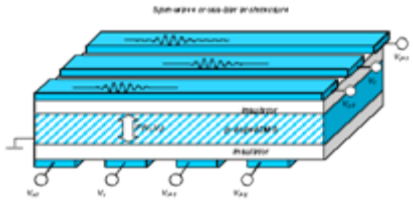
- **NEW DEVICE**
  Device with alternative state vector



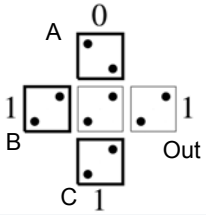


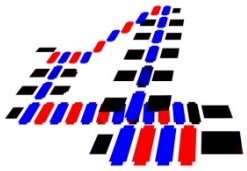
- **NEW WAYS TO CONNECT DEVICES**
  Non-charge data transfer



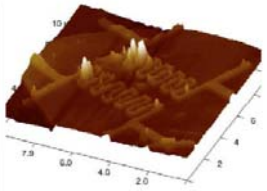


- **NEW METHODS FOR COMPUTATION**
  Non-equilibrium systems

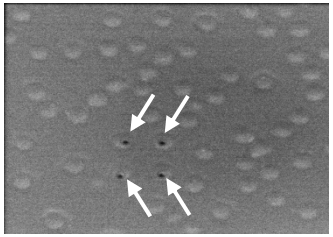




- **NEW METHODS TO MANAGE HEAT**
  Nanoscale phonon engineering



- **NEW METHODS OF FABRICATION**
  Directed self-assembly devices



Nanoelectronics Research Initiative Milestones

- 2001-2004: Defining Research Needs
  - ITRS-Emerging Research Device Technical Working Group
  - NSF-SRC Ind-Academia-Govt "Silicon Nanoelectronics and Beyond" Workshops
  - SIA Technology Strategy Committee workshops
  - ➢ *Defined 13 Research Vectors for finding the "next switch"*
  - ➢ *SIA Board passes resolution for formation of NRI*
- Current Member Companies:

GLOBALFOUNDRIES IBM intel Texas Instruments Micron

- Sep 2005: First NRI and NRI-NSF Solicitations released
- Jan 2006: Research Programs started

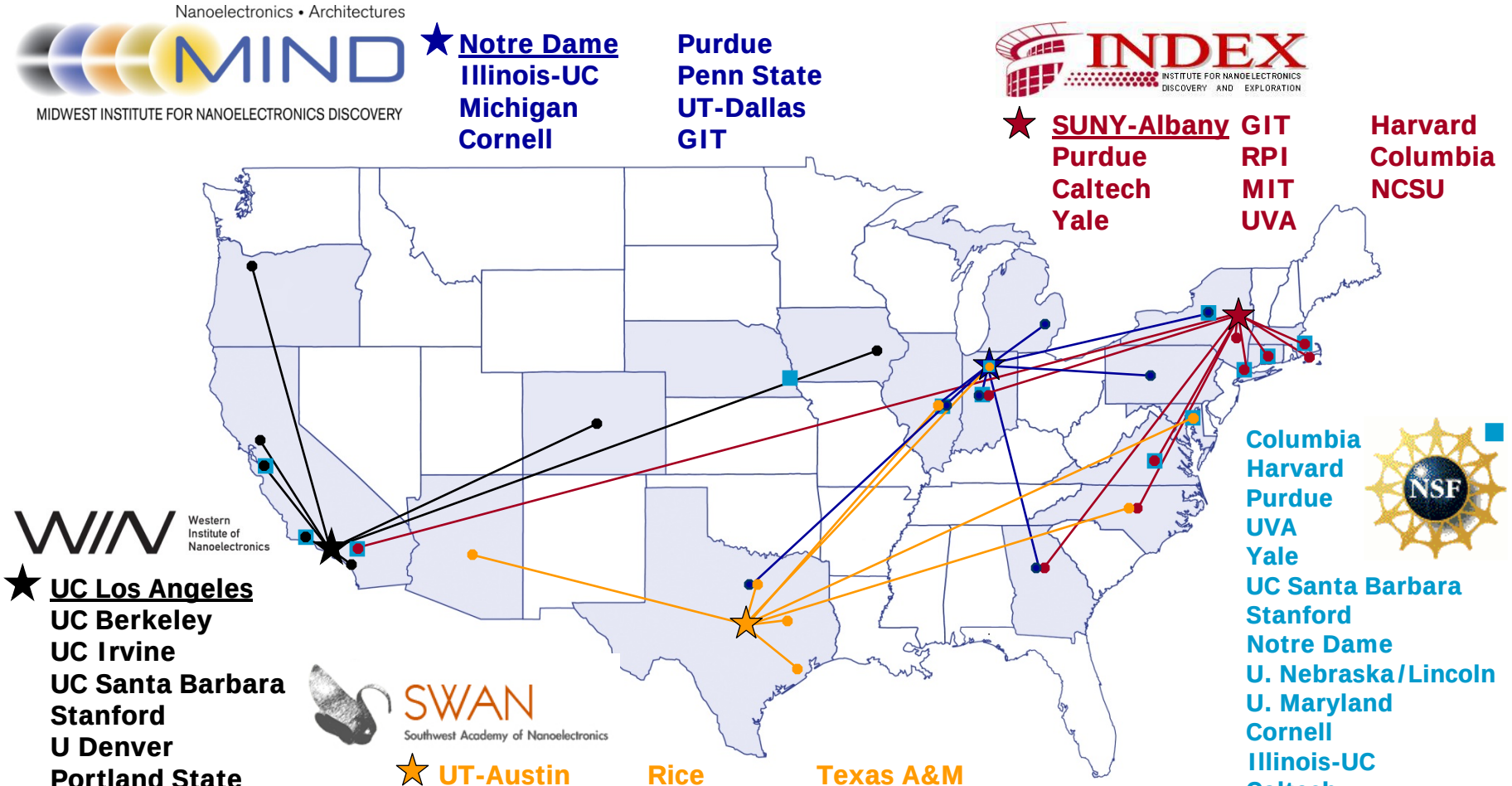
NSF

- Sep 2007: NIST joins NRI

NIST

- NRI partnership model highlighted in as sidebar in the National Nanotechnology Initiative (NNI) Strategic Plan (NNCO, 1/08)

NRI Funded Universities



Over 30 Universities in 18 States

NSF-NRI Projects

Co-funding Projects at NSF Nanoscience Centers

Columbia NSEC	*2008: Novel Device Arch. based on Quantum Transport Phenomena in Graphene*
Harvard NSEC	*2008: Tunable Ultra-fast Conductance Switching through External Fields*
Purdue NCN	*2007: Exploratory Theory, Modeling, and Simulation for the NRI* *2008: Experimental Realization of Low-power Transistors with Negative Capacitors*
UVA MRSEC	*2007: Coherent Spin Dynamics in Single Ion-doped Semiconductors: Towards a Coherent or Quantum Spin Switch*
U. Nebraska MRSEC	*2007: Multiferroic Interfaces: New Paradigms for Functional Switching*
Yale MRSEC	*2007: Design and Fab of Magnetic-based Devices with Complex Oxide Materials*
Maryland MRSEC	*2007: Pseudospintronics (UT-Austin)* *2008: Controlling the Electronic Properties of Graphene*
Cornell NSEC	*2007: Controlled Orbital Hybridization in the CNT Quantum-Modulated Transistor*
Stanford NSEC	*2008: Ultra-Low Power Pseudospintronic Switching in Bilayer Graphene at Room T*
Caltech MRSEC	*2008: Graphene Atomic Switches for Ultracompact Logic Devices and NV Memory*

- Funding 12 projects at 10 centers
  - Will announce more projects for 2009 shortly

NRI-NIST Interaction:

Full Partners in NRI Centers

- Leveraging industry, university, and both state & fed government funds, and driving university nanoelectronics infrastructure

WIN Western Institute of Nanoelectronics	**INDEX** Institute for Nanoelectronics Discovery & Exploration	**SWAN** SouthWest Academy for Nanoelectronics	**MIND** Midwest Institute for Nanoelectronics Discovery
UCLA, UCSB, UC-Irvine, Berkeley, Stanford, U Denver, Iowa, Portland State	**SUNY-Albany**, GIT, RPI, Harvard, MIT, Purdue, Yale, Columbia, Caltech, NCSU, UVA	**UT-Austin**, UT-Dallas, TX A&M, Rice, ASU, Notre Dame, Maryland, NCSU, Illinois-UC	**Notre Dame**, Purdue, Illinois-UC, Penn State, Michigan, UT-Dallas, Cornell, GIT
Theme 1: Spin devices Theme 2: Spin circuits Theme 3: Benchmarks & metrics Theme 4: Spin Metrology	Task I: Novel state-variable devices Task II: Fabrication & Self-assembly Task III: Modeling & Arch Task IV: Theory & Sim Task V: Roadmap Task VI: Metrology	Task 1: Logic devices with new state-variables Task 2: Materials & structs Task 3: Nanoscale thermal management Task 4: Interconnect & Arch Task 5: Nanoscale characterization	Theme 1: Graphene device: Thermal, Tunnel, and Spin Theme 2: Interband Tunnel Devices Theme 3: Non-equilibrium Systems Model / Meas. Theme 4: Nanoarchitecture

NIST – NRI Projects

- NIST partnership expanding with joint project collaborations
  - Starting new projects and influencing existing NIST collaborations

PI	Center	Project	NIST Collaborator
Eric Pop	MIND	Avalanche impact ionization in semiconducting carbon nanotubes	Curt Richter
Karl Berggren	INDEX	He Ion Microscope	Mike Postek
Alain Diebold	INDEX	Optical measurement of Phonons in Graphene and their connection to electron mean free path	Ward Johnson Vinod Tewary
Robert Geer	INDEX	Nanoscale electrical measurements and SPM of Graphene	Joe Kopanski
Julia Greer	INDEX	Graphene mechanical properties	Ward Johnson
Phillip First	INDEX	Atomic-scale electrical metrologies specifically for graphene	Joseph A. Stroscio; Mark D. Stiles
Philip Kim	INDEX	Studying quantum Hall effect in graphene as a resistance standard	David Newell

WIN Technical Plan

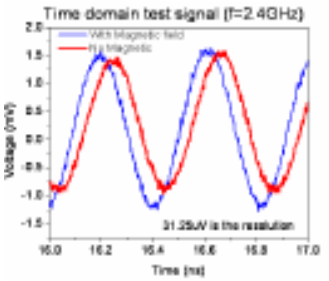
Western Institute of Nanoelectronics

THEME/Category	Focus	Task/Project
Devices	Spin Wave Devices	➢Spin Wave Superposition ➢Multiferroic based Spin logic
	Magnetic Dot Logic	➢Magnetic Coupling of Magnetic Nanoparticles ➢2D and 3D Magnetic Dot Logic
	2-terminal Spin Devices	➢Magneto-resistive Devices ➢Spin-Torque Devices ➢Multiferroic spin valves and junctions ➢Pseudospintronic graphene valves
	3-terminal Spin Devices	➢Spin FET based on MnGe (thin film and nanowire) ➢Spin Hall Effect devices ➢3-terminal TMR/GMR devices ➢Pseudospintronic oscillators/memory/CMOS integration
Device/Device Coupling & Interconnect	Resonant Coupling	➢Spin coupling using super-conducting resonators ➢Cavity Control of Spin Interaction
	Spin Wave Bus	➢Spin Wave interconnects
Metrics and Benchmarks	Spintronics Performance Metrics & Limits	➢Circuit Design and Performance Metrics for Spintronic ➢Benchmarking and Criteria for WIN devices ➢Metrics for New Switch concepts Evaluation
Metrology	Spin Characterization	➢Single Spin Detection – Kerr Rotation ➢X-ray magnetic circular dichroism (XMCD) ➢Kerr Rotation using Tip Enhanced Near-field Microscopy ➢Scanning Transmission X-ray Microscopy (STXM)

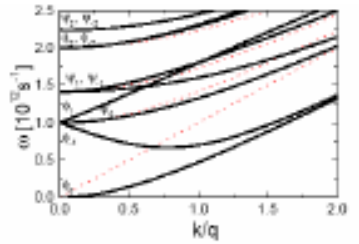
Spin Wave Device Research

Multiple PI's

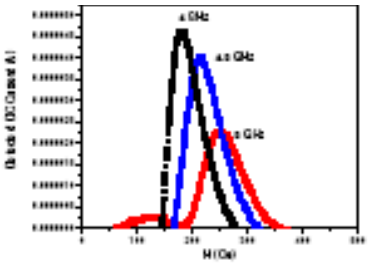
Western Institute of Nanoelectronics



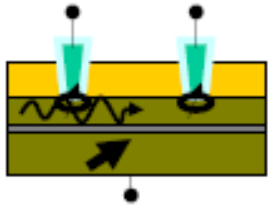
Modulation of spin wave by magnetic field



Simulation of spin wave generation by electric field (UC Berkeley)

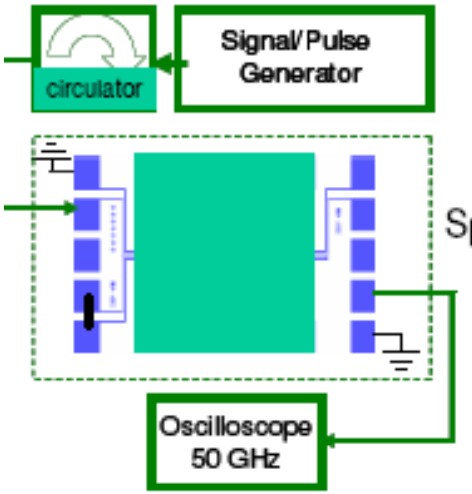


Demonstration of Spin Rectification via spin valve (UCLA)

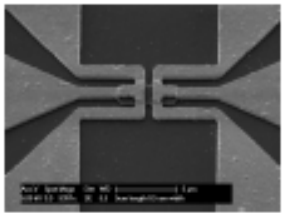


Spin Wave amplification (Staford)

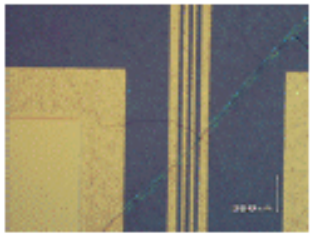
2006 → **2007** → **2008/09**



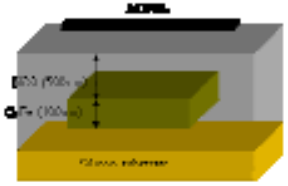
Established spin wave characterization



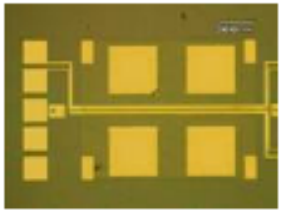
Spin Waveguides (UCSB)



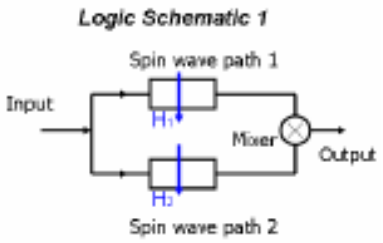
Fabricated structures using PZT and BFO



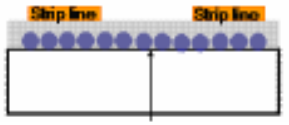
Design spin wave devices and gates



Structures to reduce Eddy Currents



Spin wave circuits (UCSB/UCLA)

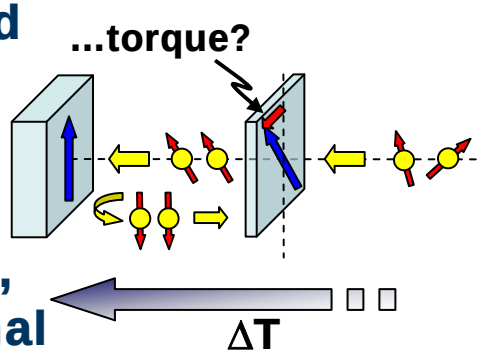


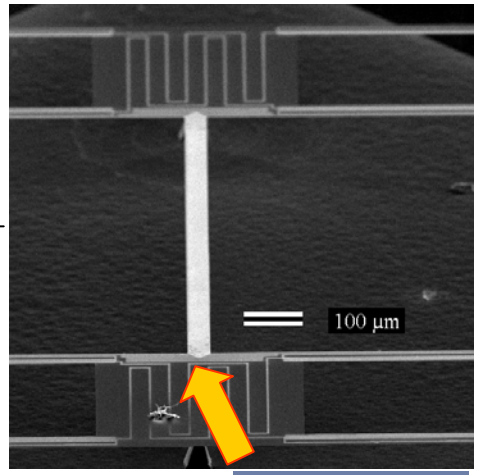
Optimize spin wave device

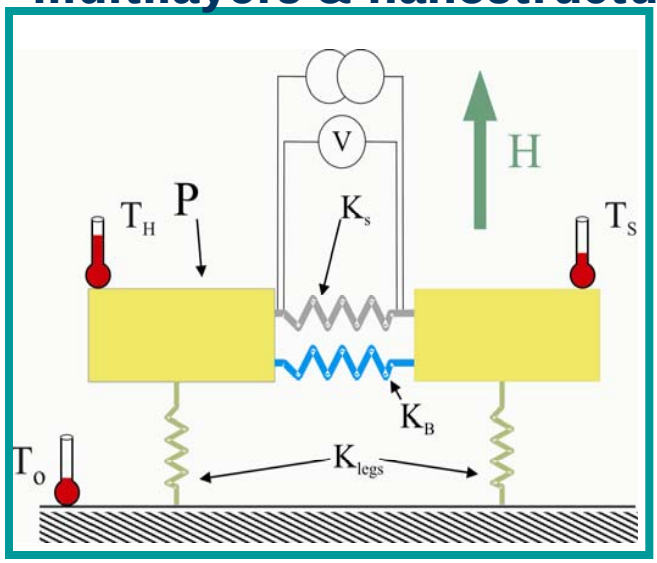
Measuring thermal spin currents and torques

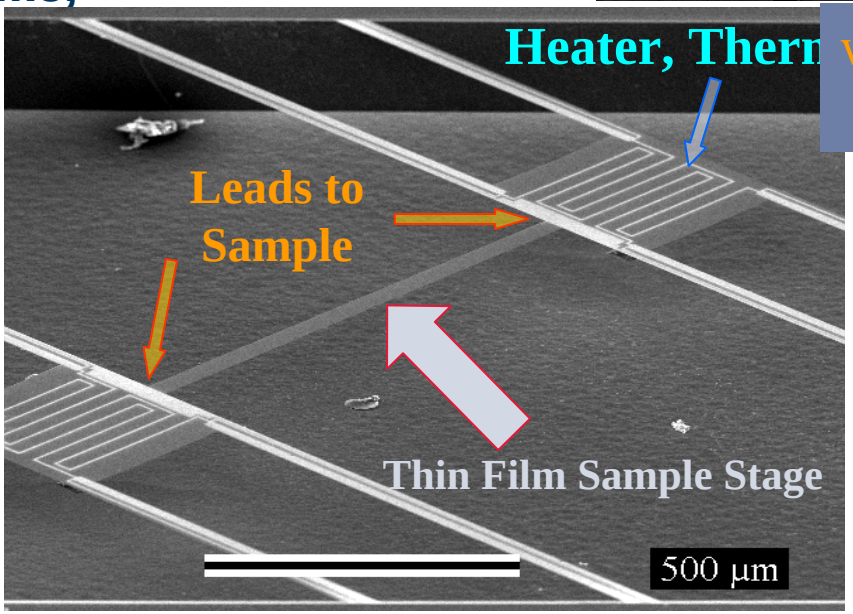
A. Avery, R. Sultan, D. Bassett, B. L. Zink, U. of Denver; M. R. Pufall, NIST

- **Motivation: Thermal gradients predicted to drive spin-polarized currents and torques in magnetoelectronic nanostructures**
- **Goal: Use novel measurement techniques to quantify the thermal, thermoelectric, and magnetothermal properties of magnetic thin films, multilayers & nanostructures**









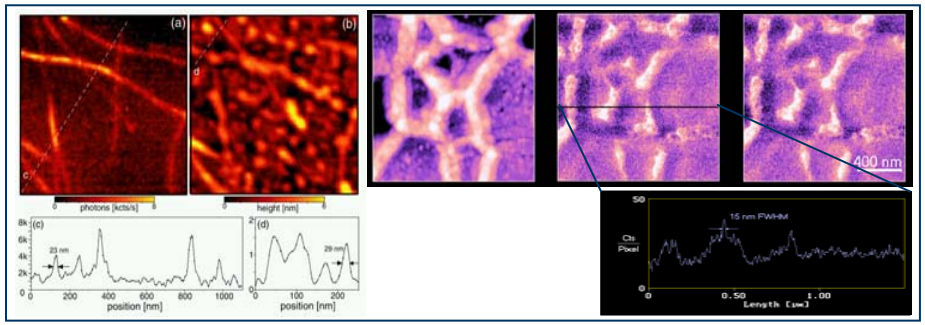
Development of a Tip-Enhanced Near-Field Scanning Magneto-Optical Kerr Microscope

E.J. Sanchez, Portland State

ONAMI WIN Western Institute of Nanoelectronics

Background

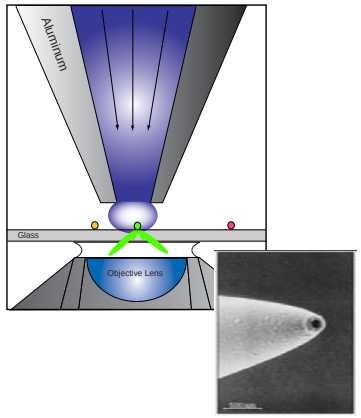
- Due to diffraction, traditional optical microscopy is limited to a resolution of roughly half the wavelength of the incident light.
- Near-field scanning optical microscopy (NSOM) is able to overcome this diffraction limit.
- Tip-enhanced near-field optical microscopy (TENOM), has produced higher resolution images ~10's of nm's.



Left: Simultaneous near-field Raman image (a) and topographic image (b) of SWNT grown by CVD on glass.

Right: 15 nm resolution of photosynthetic membranes (*Spinacea Olerecia*) on glass.

NSOM:



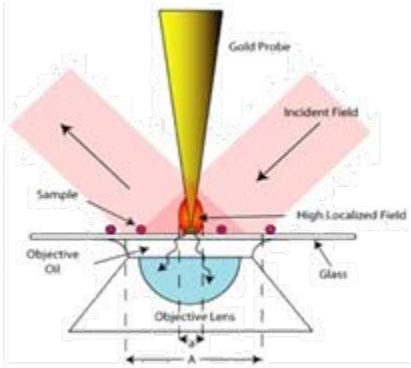
Light propagates thru pulled optical fiber onto surface

Optical signal collected thru fiber

Resolution limited by diam. of aperture (~>50 nm)

Simultaneous illumination/ collection allows for study of non-transmissive samples

TENOM:



Light focused on sharp gold tip 2-5 nm from surface

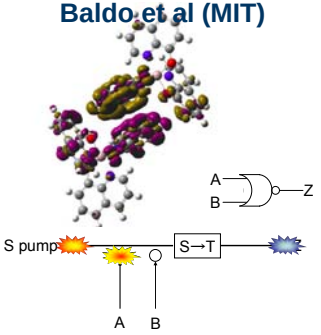
Sample excited by localized field enhancement

Raman/fluorescence imaging

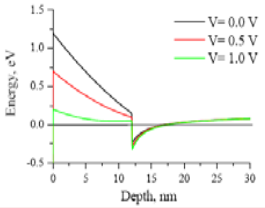
Resolution limited by sharpness of tip (<20 nm)

Better resolution, higher topography

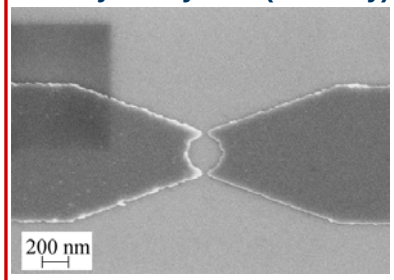
Molecular Excitons Spintronics
Baldo et al (MIT)



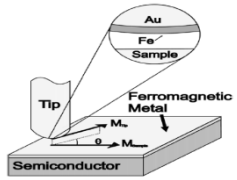
Quantum Dot Modeling
Shur et al (RPI)



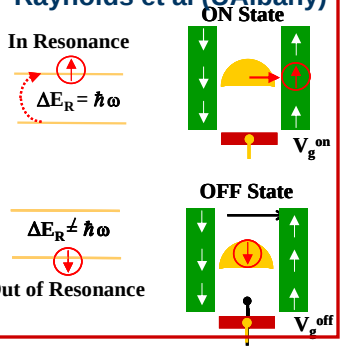
Quantum Dot Devices
Oktyabrsky et al (UAlbany)



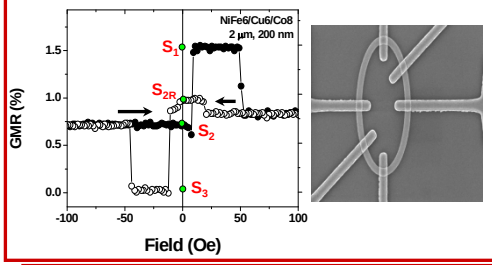
Ballistic Spin Devices
Labella et al (UAlbany)



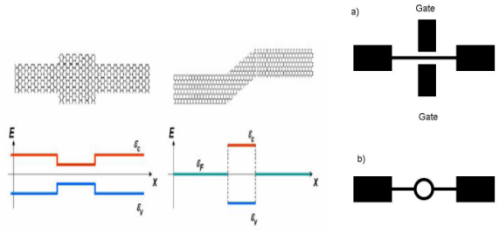
Single Electron Spin Devices
Raynolds et al (UAlbany)



Magnetoelectronic Devices
Multi bits logic Ross et al (MIT)

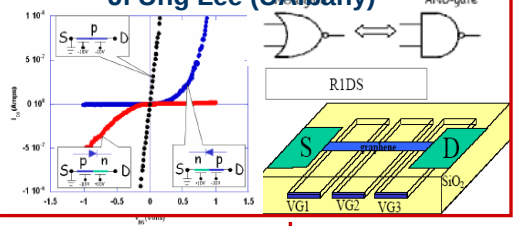


Graphene Nanowire Switches
Murali and DeHeer (GT)

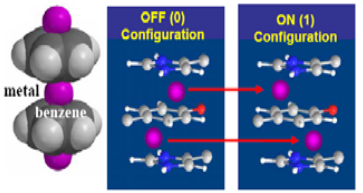


Post CMOS Switches

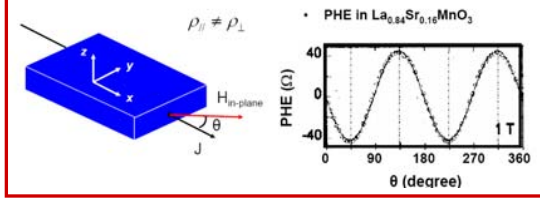
Reconfigurable One-Dimensional (1D) Switch (R1DS)
Ji Ung Lee (UAlbany)



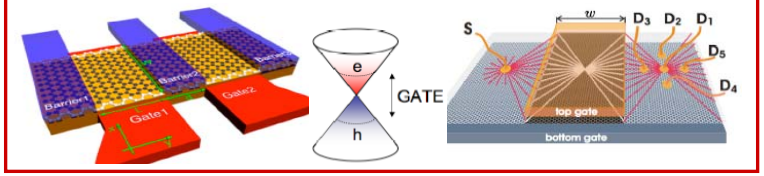
Molecular Nanowire Switches
Kaloyeros et al (UAlbany)



Logic Switches based on Complex Oxides
Ahn et al (Yale)

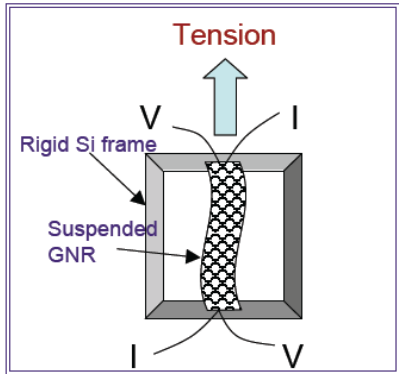


Graphene based Quantum Devices
Charles Marcus (Harvard)

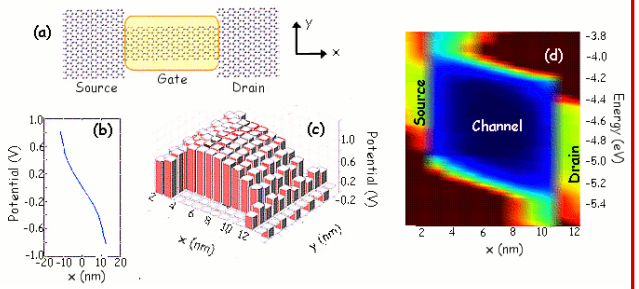


New Project 2008

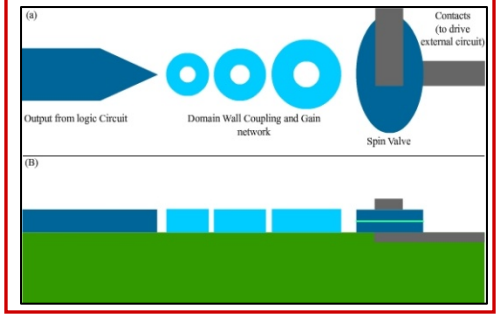
In-situ graphene characterization
Greer (CalTech)



Graphene Circuit Modeling
Stan (UVA)



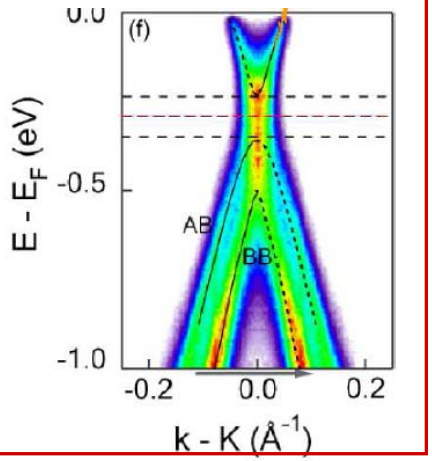
Magnetic Tunnel Junctions in Nanowires
Misra et al (NCSU)



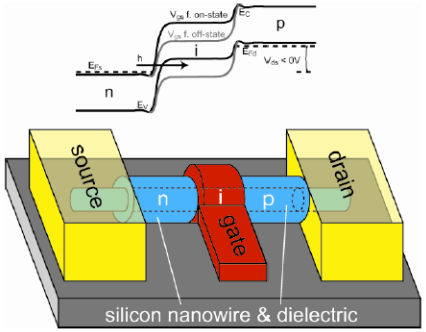
INDEX
INSTITUTE FOR NANOELECTRONICS DISCOVERY AND EXPLORATION

Post CMOS Switches and Metrology

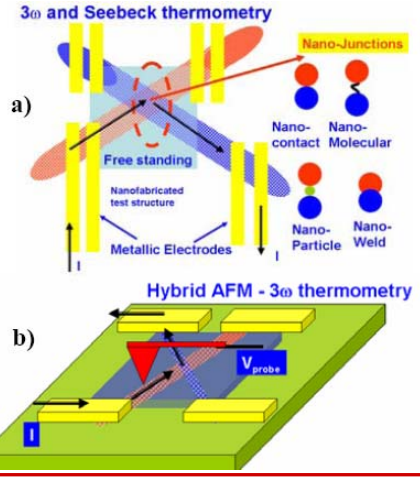
Graphene Metrology
First (GIT)



Non-equilibrium FET
Appenzeller (Purdue)

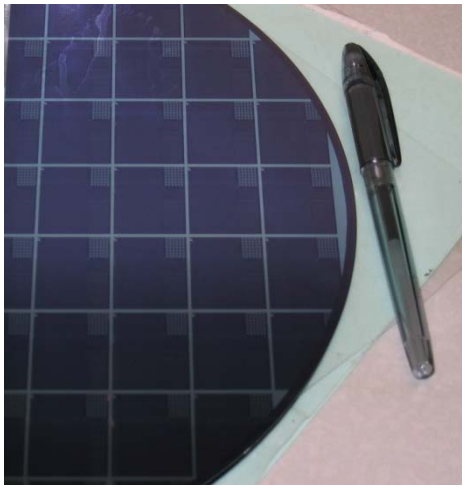


Heat Management
Ramanath et. al. (RPI)

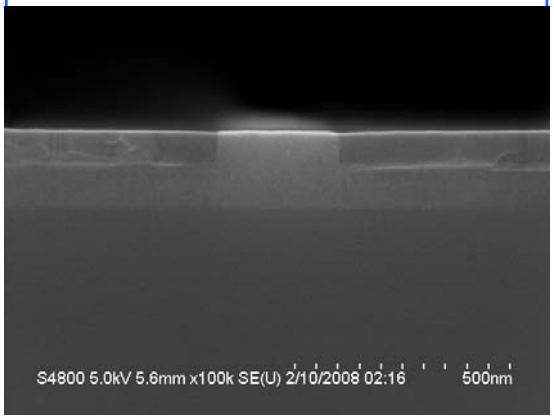


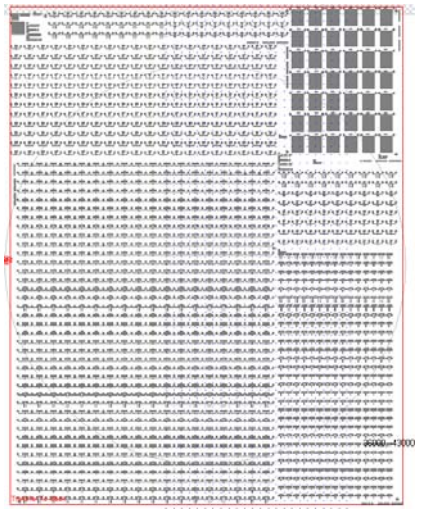
Test Site Design and Fabrication

(0.1+0.1 wafer starts per day from IBM and UAlbany)



- >1000 devices/die
- Advanced processes





Novel Device Integration Capability: Developed test structures and process capabilities for carbon nanotube and graphene post-CMOS devices using advanced 300mm wafer line.

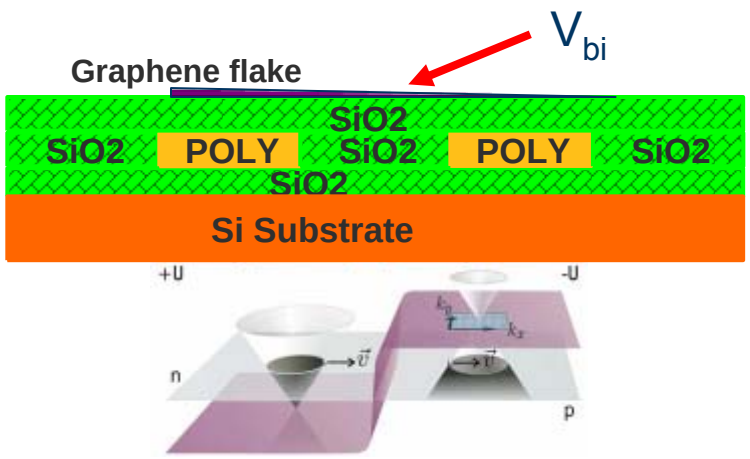
- **First run completed for measuring exciton transport in CNTs**

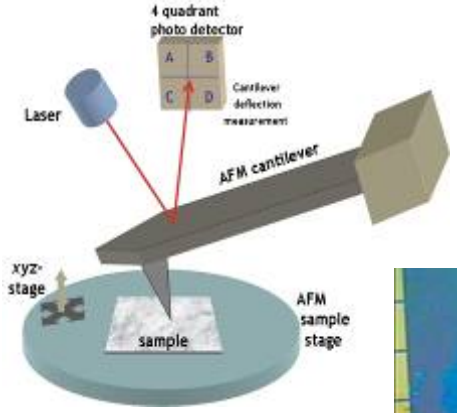
NRI Objective: Develop massively parallel scheme for sampling large device and materials parameters.

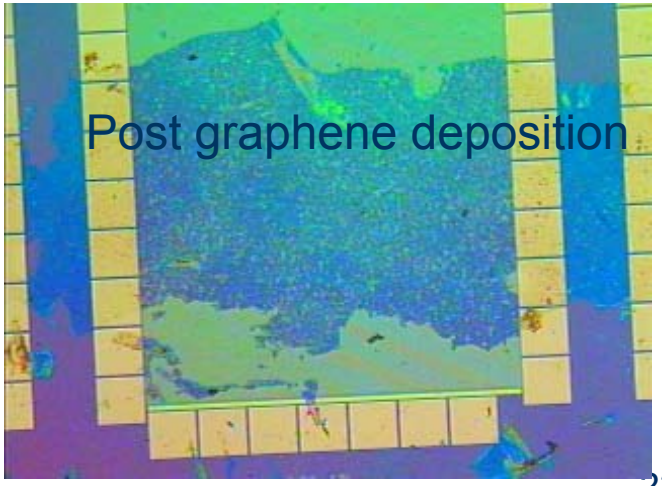
Nanoscale Electrical and Scanning Probe Microscopy of Graphene Devices

Robert Geer-UAlbany, Joe Kopanski – NIST

- *Kelvin probe microscopy: Electric-force imaging to extract surface potential*
- *Enables measurement of V_{bi} in conventional semiconductor p-n junctions*
- *Adapt to electrostatically-doped graphene structures (macro-electrodes)*





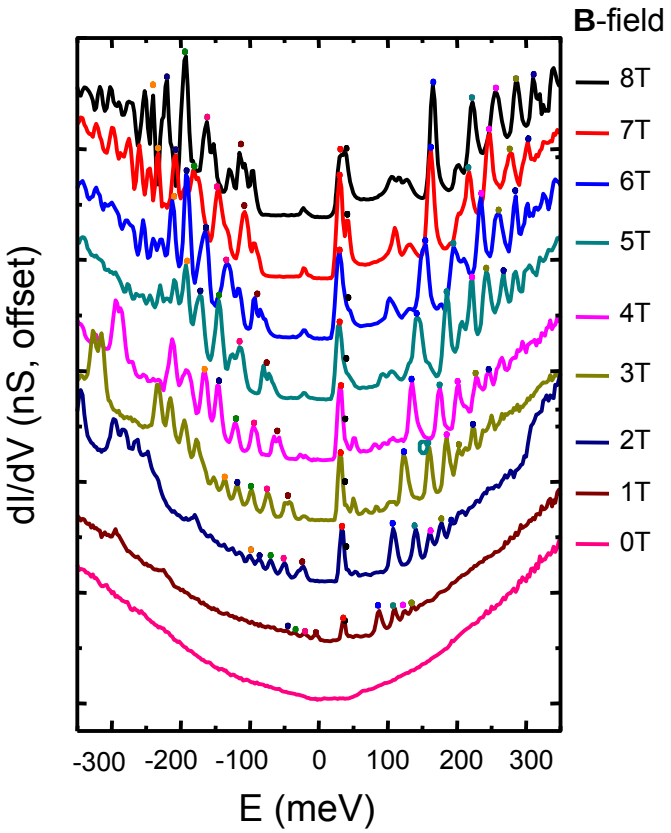


Effect of Magnetic Field: Epi-Graphene on SiC(000-1)

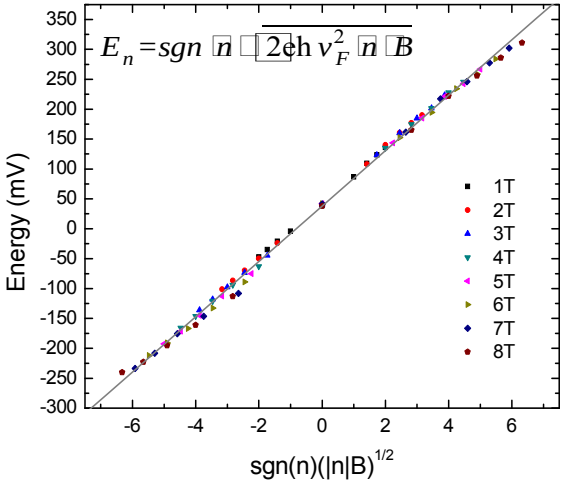
P.N. First (GIT), J.A. Stroscio (NIST)
Material: ***W. A. de Heer,*** *GIT*

Rotationally-stacked Multilayer with **Single Layer** Behavior

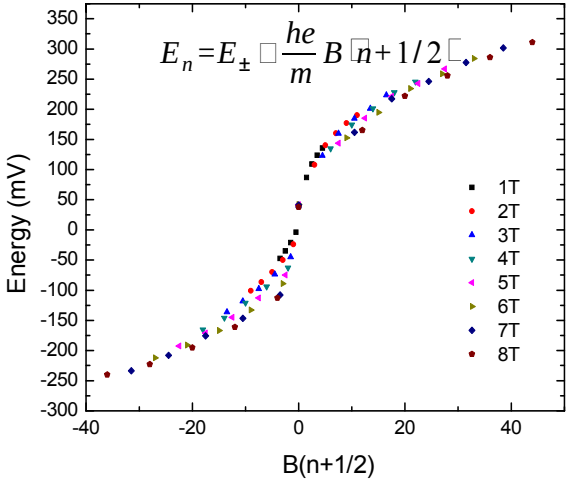
Tunneling spectroscopy of Landau levels (quantized cyclotron orbits) shows graphene indexing, **not** graphite.



Graphene Indexing

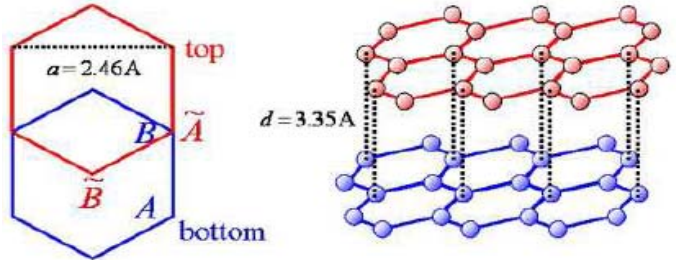


Graphite Indexing

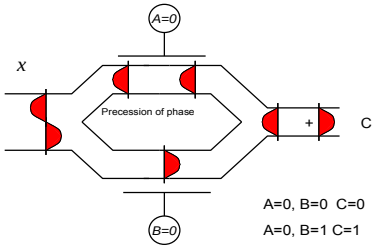


South West Academy of Nanoelectronics

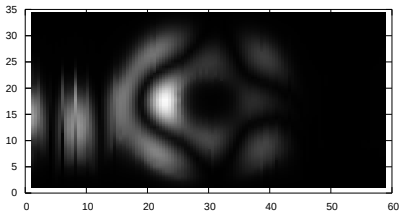
Task 1: Logic Devices with Alternate State Variables



Pseudospintronics on Graphene: UT, UTD, Maryland

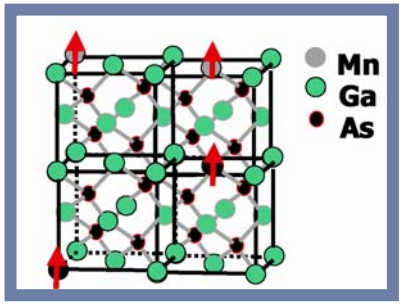


Phasetronics: UT

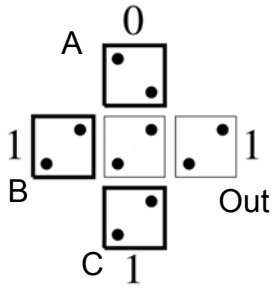


Path Integral Monte Carlo: ASU

Task 2:Novel Materials and Structures

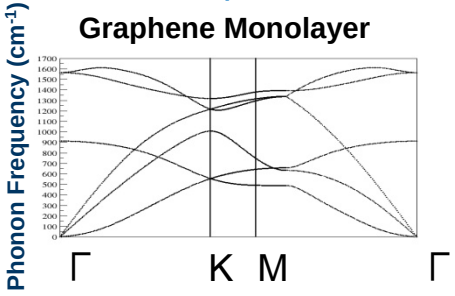


DMS: A&M, Maryland, UT

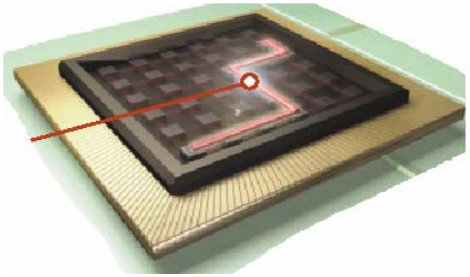


MQCA:ND

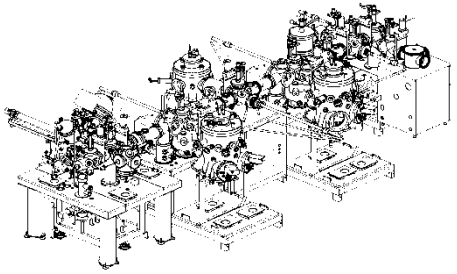
Task 3: Nanoscale Thermal Management
UIUC, NCSU



Task 4: Nano plasmonic interconnects
Rice



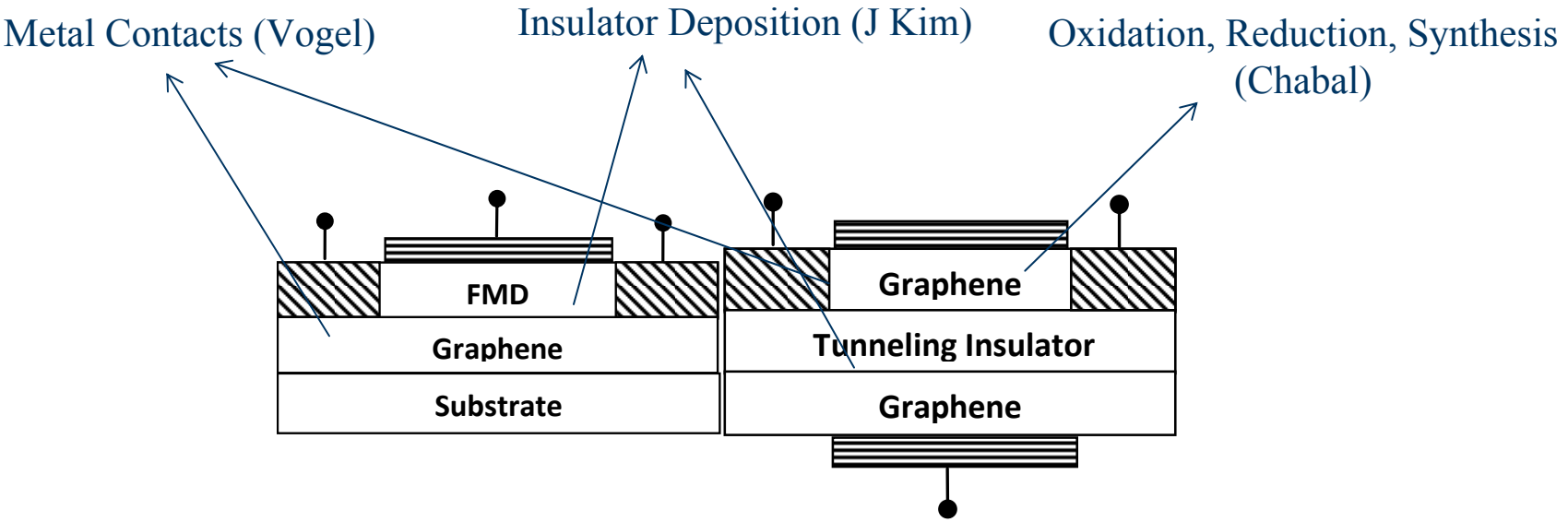
Task 5: Nanoscale Characterization
UTD



Graphene Device Fabrication

Goal of UTD SWAN-Graphene Program:

To develop the materials science, processes, characterization techniques and associated understanding necessary to implement beyond-CMOS graphene-based devices.



Cross-cutting: Microscopy & Manipulation (M Kim), Surface Science (Wallace), Material Modeling (Cho)

How do real processes and interfaces affect the ideal properties of graphene (e.g. structure, bonding, D.O.S.)?

Hi-K on Graphene

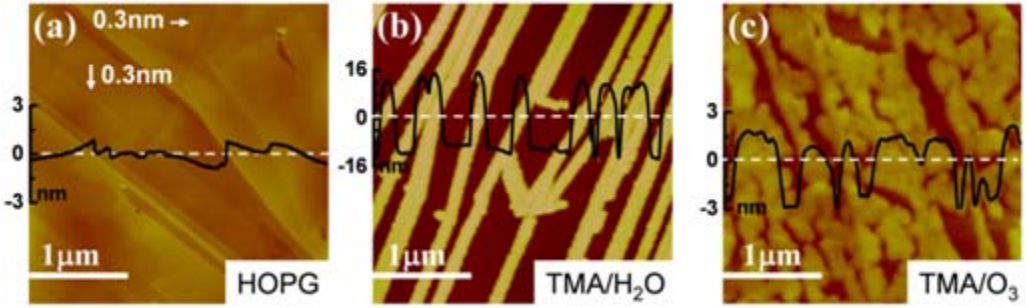
B. Lee, J. Kim

SWAN Southwest Academy of Nanoelectronics

NRI

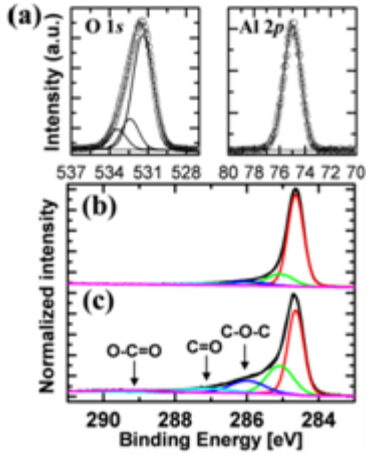
UT-Dallas demonstrated conformal Al_2O_3 ALD on HOPG

- **Characteristics of poor ALD-Al_2O_3 layer on the HOPG surface**



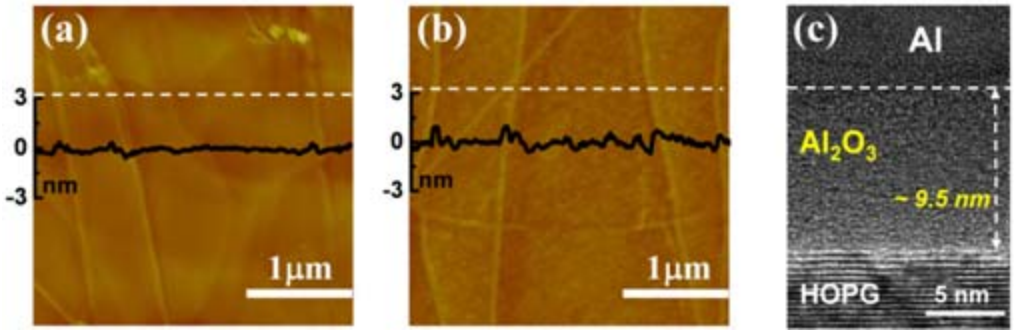
(a) AFM image of fresh HOPG surface (b) the sample with Al_2O_3 layer deposited from TMA/H2O 200 cycles process (c) with Al_2O_3 layer from TMA/O_3 process 50 cycles.

- **O_3 treatment functionalizes surface and enables conformal deposition**

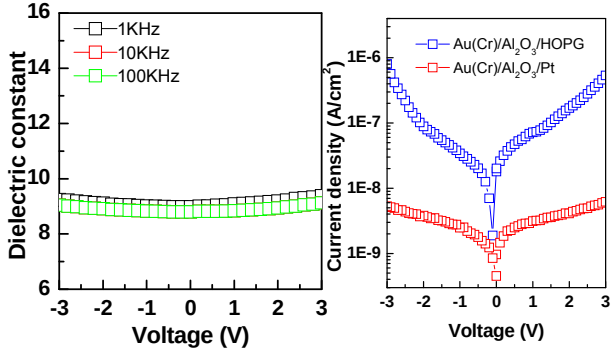


XPS spectra of the Al_2O_3 layer deposited in 50 cycles on top of HOPG treated by ozone (a) O 1*s* /Al 2*p* (c) C 1*s*. (b) XPS spectra of C 1*s* on the fresh HOPG

NRI Significance: Conformal deposition of the ALD-Al_2O_3 layer through functionalization of the HOPG surface using O_3



AFM images of (a) the HOPG surface treated by ozone pretreatment, (b) the ALD-Al_2O_3 dielectric (50 cycles) surface on the ozone-treated HOPG, and (c) the cross-sectional HR-TEM image of the Al metal/Al_2O_3 (100 cycles)/the ozone-treated HOPG.



Electrical properties of capacitors incorporating ALD Al_2O_3 films on HOPG demonstrating expected dielectric constant and the associated leakage properties

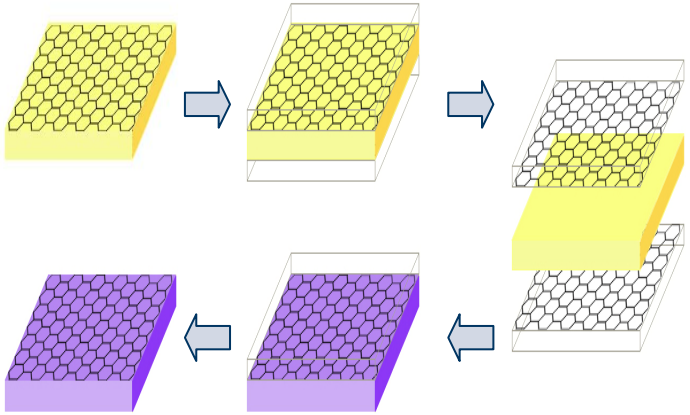
Graphene CVD Growth on Cu Foil

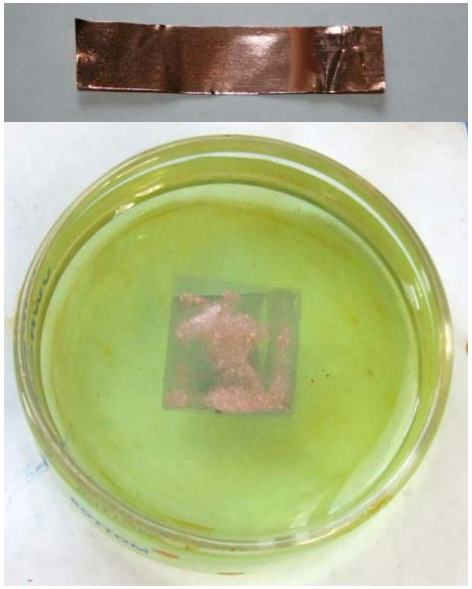
R. Ruoff, UT-Austin

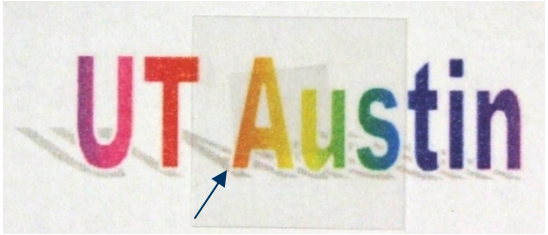
SWAN Southwest Academy of Nanoelectronics

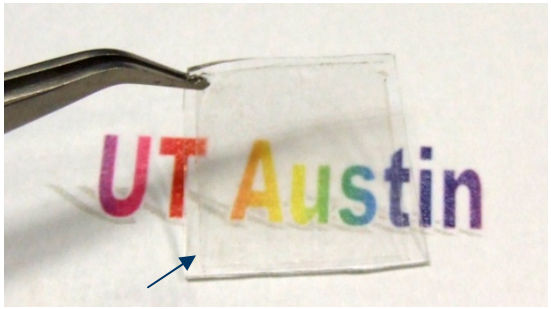
NRI

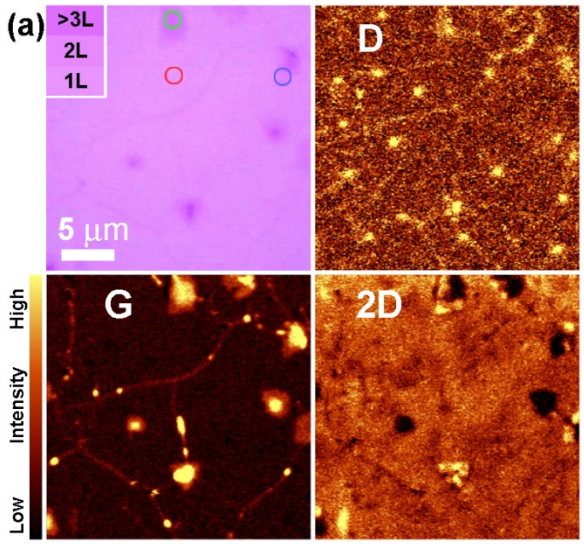
Transfer

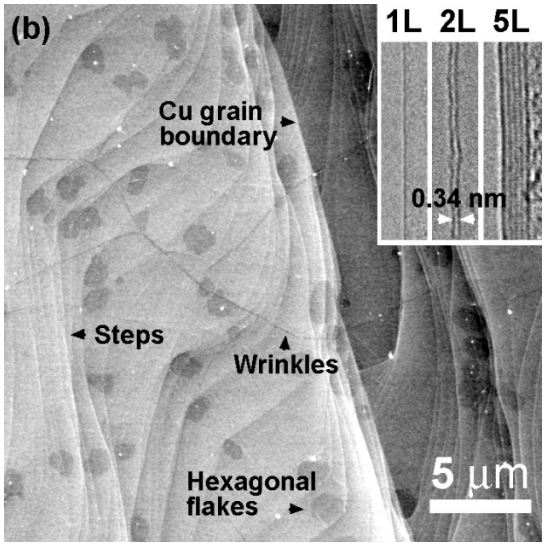


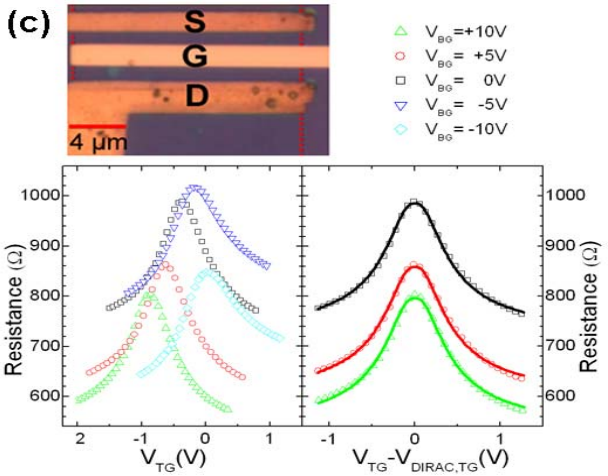








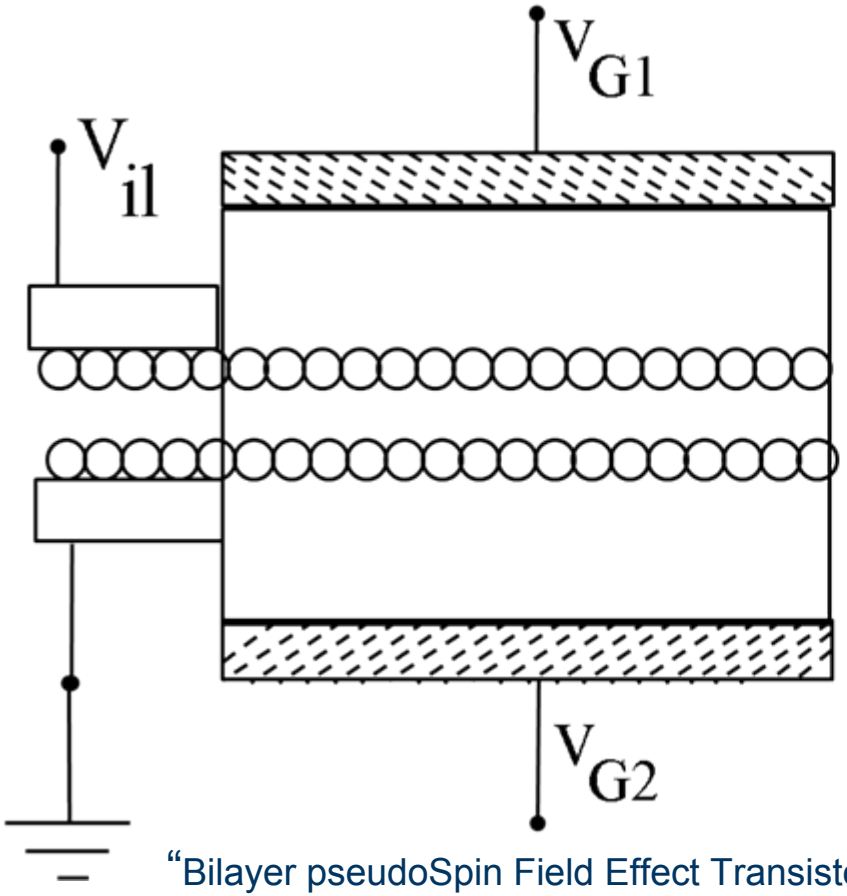


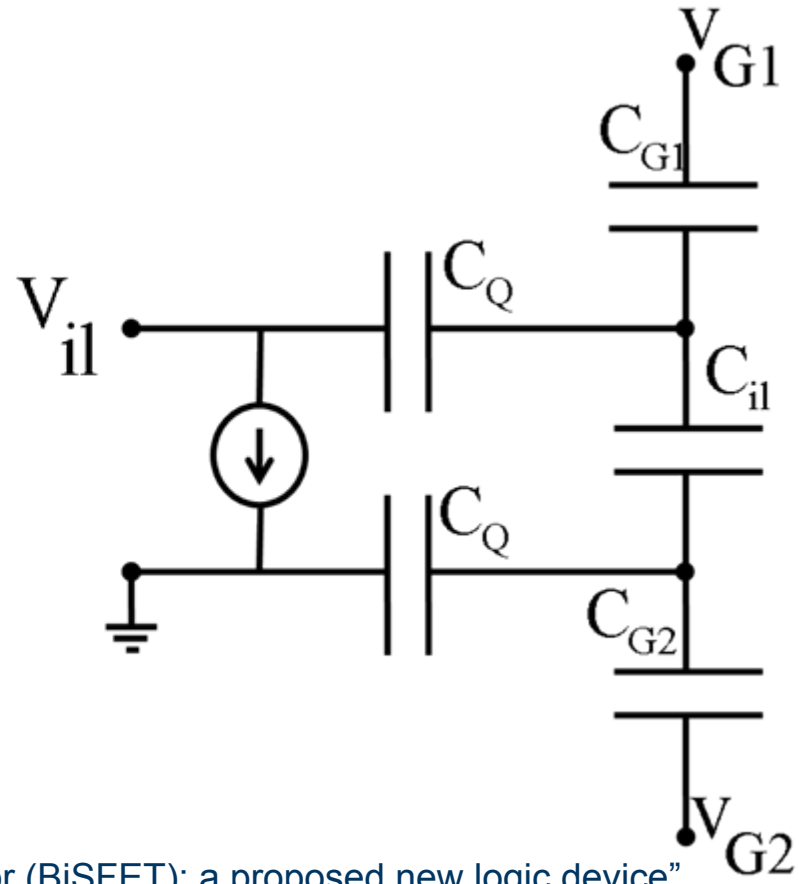


carrier mobility ~4050 $cm^2V^{-1}s^{-1}$, residual carrier concentration at the Dirac point $n_0=3.2\times10^{11}$ cm^{-2}

Bi-layer pseudoSpin Field Effect Transistor (BiSFET)

- Simulated devices and basic logic gates (SPICE)
  - Inverter with complementary BiSFET design simulated at 100 GHz with 25mV operation at just 2x Landauer limit

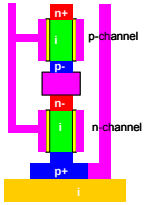




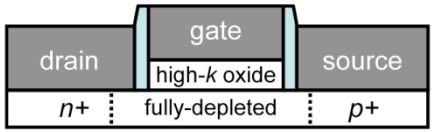
"Bilayer pseudoSpin Field Effect Transistor (BiSFET): a proposed new logic device"
S.K. Banerjee, L.F. Register, E.Tutuc, D.Reddy and A. Macdonald., EDL

Nanoelectronics — Energy-Efficient Devices

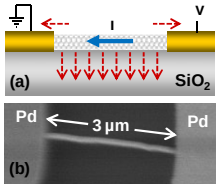
1-Dimensional nanowire interband tunnel transistors
Mayer et al. Penn State



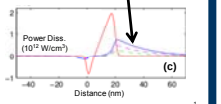
Lateral field-effect tunnel transistors
Fay et al. Notre Dame



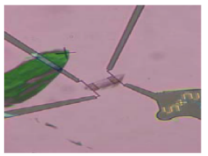
Energy Dissipation in Non-Equilibrium 1/2-D Systems
Pop et al. Illinois

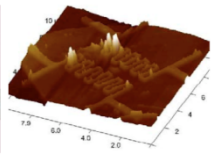


Monte Carlo modeling & design, CNT / graphene measurement



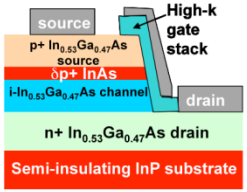
Thermal Transport and Thermal Logic Gates
Chen et al. Purdue and NML



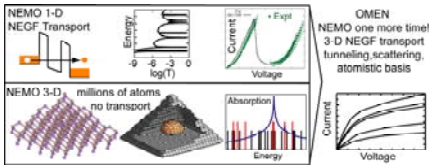


Patterned graphene nanostructures

Vertical heterostructure tunnel transistors
Datta et al. Penn State



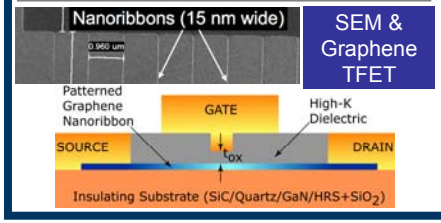
Full 3-D, 2-D, 1-D Quantum Transport Models
Klimeck et al. Purdue



Nanoelectronics • Architectures

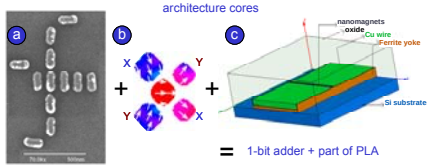
MIDWEST INSTITUTE FOR NANOELECTRONICS DISCOVERY

Gated graphene resonant tunneling transistors
Jena et al. Notre Dame



Architectures for nanoscale magnetic logic devices
Niemier et al. Notre Dame

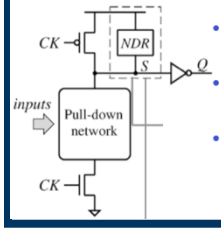
Leverage (a) experimental progress, (b) physical-level simulations of new circuit structures, and (c) drive circuitry designs + experiments to fabricate two architecture cores



Architectures for emerging NRI devices
Porod et al. Notre Dame

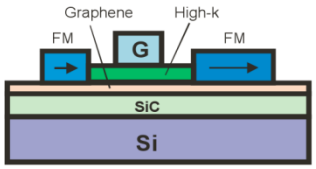
Provide performance comparison of NRI emerging device technologies for benchmarking and for comparison to CMOS technology

Circuit design for emerging NRI technologies
Mazumder, Univ. Michigan

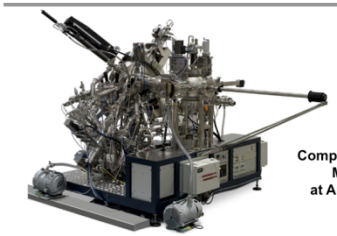


- Design tunnel transistor circuits
- Enhance noise margins
- Explore multivalued and adiabatic circuits

Graphene SpinFETs on Silicon
Ye et al. Purdue and UTD



National Lab Collaborations
NIST – Argonne – NML



Complex oxide MBE at Argonne

Architectures — Energy-Efficient Systems

Magnetic Quantum Cellular Automata (MQCA)

M. Niemier, Notre Dame

Nanoelectronics • Architectures

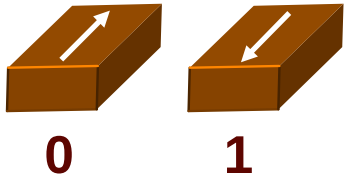
MIND

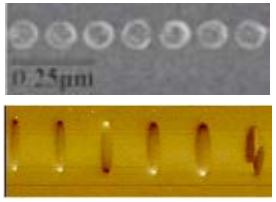
MIDWEST INSTITUTE FOR NANOELECTRONICS DISCOVERY

Schematic

Experimental

Device

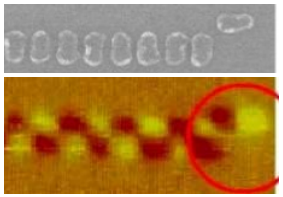




R. Cowburn, M. Welland, *"Room temperature magnetic quantum cellular automata,"* Science **287**, 1466, 2000

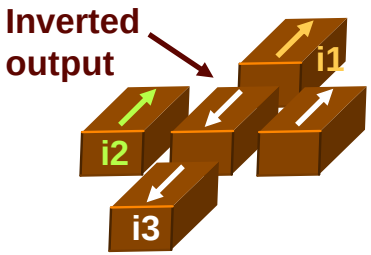
A. Imre, "Experimental Study of Nanomagnets for Magnetic QCA Logic Applications," U. of Notre Dame, Ph.D. Dissertation.

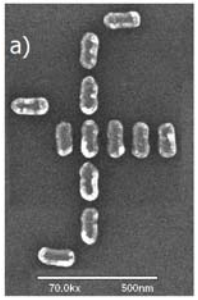
Wire

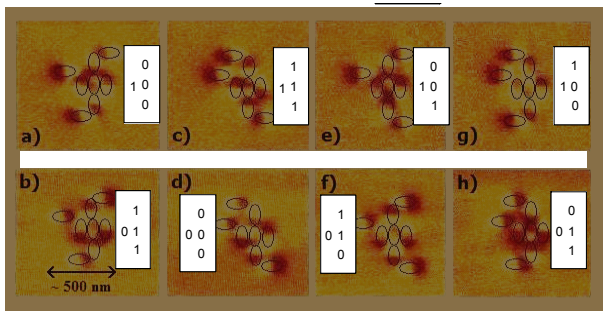


A. Imre, et. al., "Majority logic gate for Magnetic Quantum-Dot Cellular Automata," Science, vol. 311, No. 5758, pp. 205–208, January13, 2006.

Gate



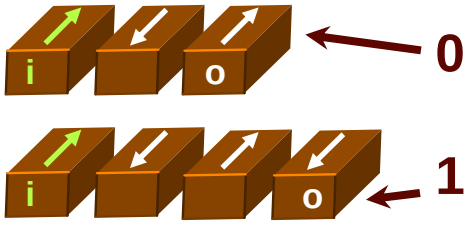




A. Imre, et. al. "Magnetic Logic Devices Based on Field-Coupled Nanomagnets," NanoGiga 2007.

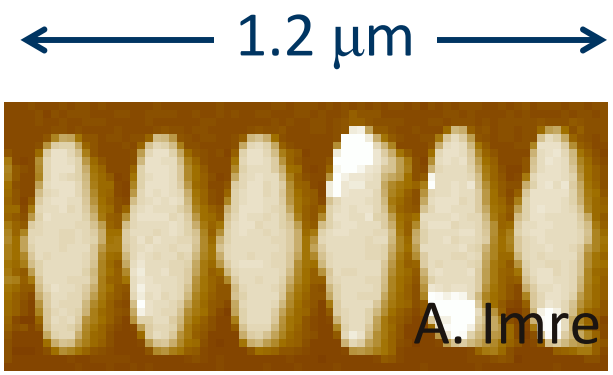
A. Imre, et. al., "Majority logic gate for Magnetic Quantum-Dot Cellular Automata," Science, vol. 311, No. 5758, pp. 205–208, January13, 2006.

Inverter

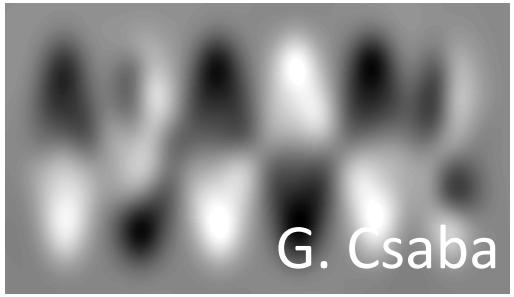


Nanomagnet logic – modeling and characterization

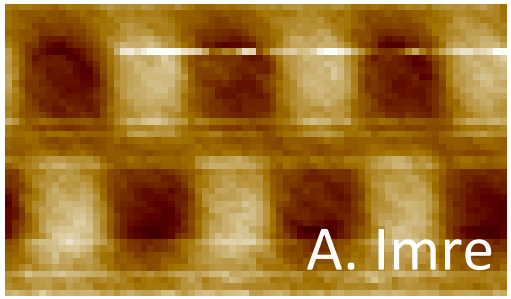
Nanoelectronics • Architectures
MIND
MIDWEST INSTITUTE FOR NANOELECTRONICS DISCOVERY
NRI



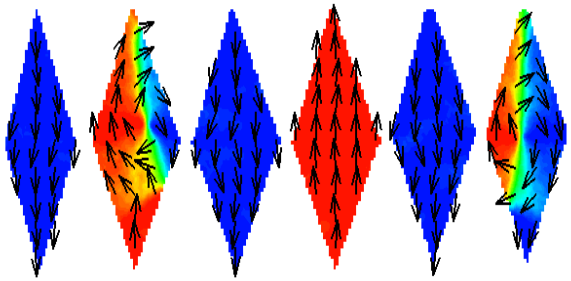
AFM topographic picture



Simulated MFM



Measured MFM



OOMMF simulation

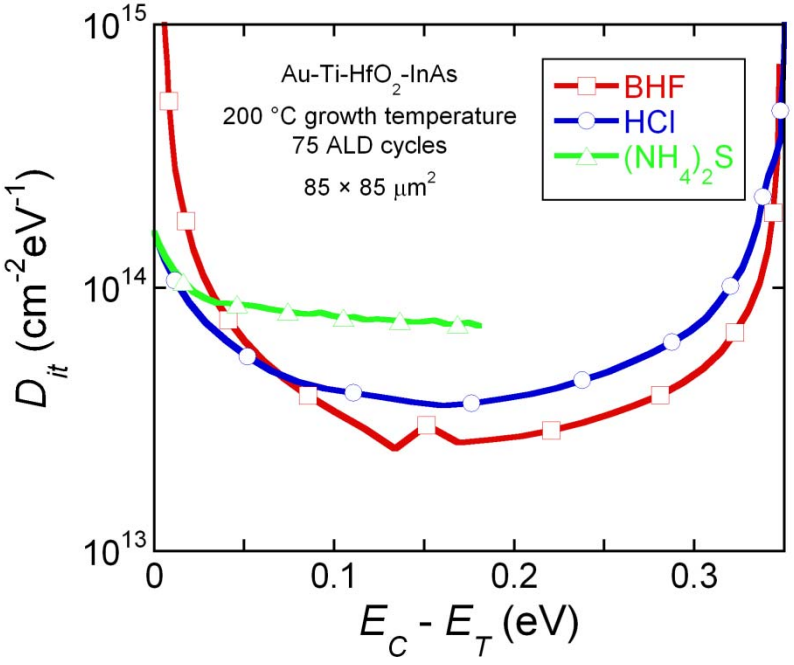
- Magnetization is routinely mapped using magnetic force microscopy (MFM)
- Quantitative field maps are inferred by comparison with simulation
- Direct nanoscale B/H field measurements are lacking at these scales (e.g. 20 x 40 x 60 nm dots)

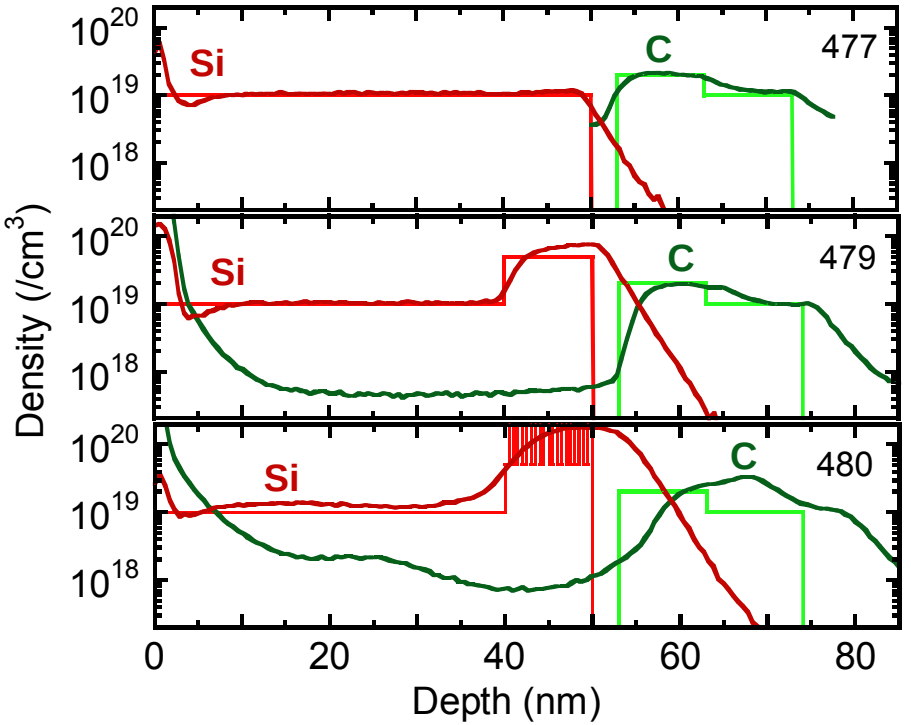
OOMMF – object oriented micromagnetic framework

M. Niemier, S. Hu, W. Porod, G. Bernstein
Notre Dame

Interface properties and dopant profiles

Field-control of tunneling, spin injection, polarization, … remain key challenges for post CMOS technologies





- SIMS characterization of InGaAs tunnel junctions: measured vs. target
- Need for electrical profiles with sub-10-nm/decade resolution

Things to Consider Going Forward

- Specific areas of focus for 2009:
  - Room temperature demonstrations of all phenomena
    - Plan to show RT results or a simulation “roadmap” on how to reach RT
  - Accelerate work to demonstrate theory, on simplified structures
    - Theorists provide insight on how to verify effects in “realistic” environments
  - Increase focus on the logic gate / computational system potential
    - How to connect the devices, how to do logic, how to scale functional density
- Increase work on metrology to explicitly link theory to experiment to assess potential devices
  - Experimentalists: “What modeling is needed to understand and extrapolate the device potential of current materials/structure/phenomena results?”
  - Theorists: “What experiments are needed to constitute a proof-of-concept of your theory or analysis? For example, what experimental work is needed to verify key parameters/assumptions in your model?”
  - Metrologists: “How can we measure the critical parameters to bridge between the experimental and simulation results?”

Take-aways

- Power will continue as the principal scaling issue for all IC applications
  - CMOS will continue to scale over at least the next decade, with emphasis on utilizing increasing transistor density over increasing frequency
- Any new technology must overcome the power / performance limits of a charge-based FET to continue the scaling trend of increased function / dollar
  - Does it offer the prospect of lower energy operation / storage?
  - Does it offer the prospect of non-equilibrium (e.g. ballistic) operation?
  - Does it offer the prospect of energy recovery?
- Advancing metrology and characterization techniques is key to the effort to develop any new device
  - “If we can’t measure it, we can’t make it.”

Questions? More Information?

Jeff Welser, Director
jeff.welser@src.org

Allison Hilbert, Executive Assistant
allison.hilbert@src.org