Design of test structure for 3D-stacked integrated circuits (3D-SICs) metrology

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Background

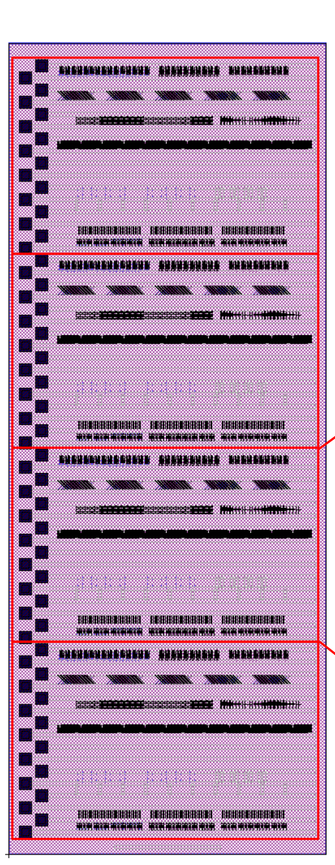
- 3D Stacked Integrated Circuits (3D-SICs) draw tremendous research. [1]
- However, it faces some challenges such as Through Silicon Vias (TSVs) and Back-end of line (BEOL) issues. [2-4]
- Scanning Probe Microscopy (SPM) technologies have mature surface metrology capability but is short in subsurface imaging, which is important for 3D-SICs.
- Recently, some SPM techniques show their capability of subsurface characterization on different semiconductor devices. [5, 6]

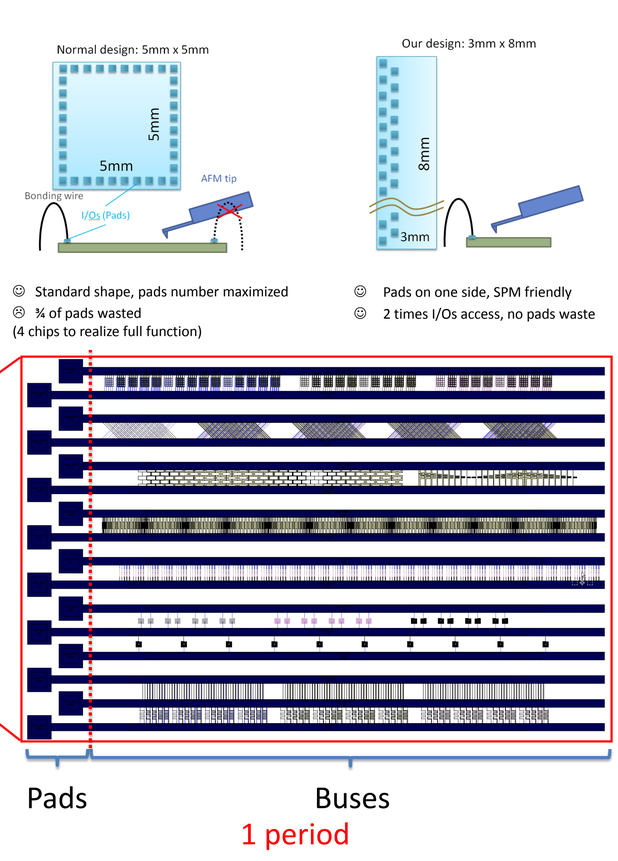
Objectives

- A multi-level chip to simulate 3D circuit issues
- Must be SPM friendly (SMM, KFM, SCM, etc.)
- Provide multi-level subsurface structures
- Can be externally biased and extract physical parameters (φ, E, B, C, ε, etc…)

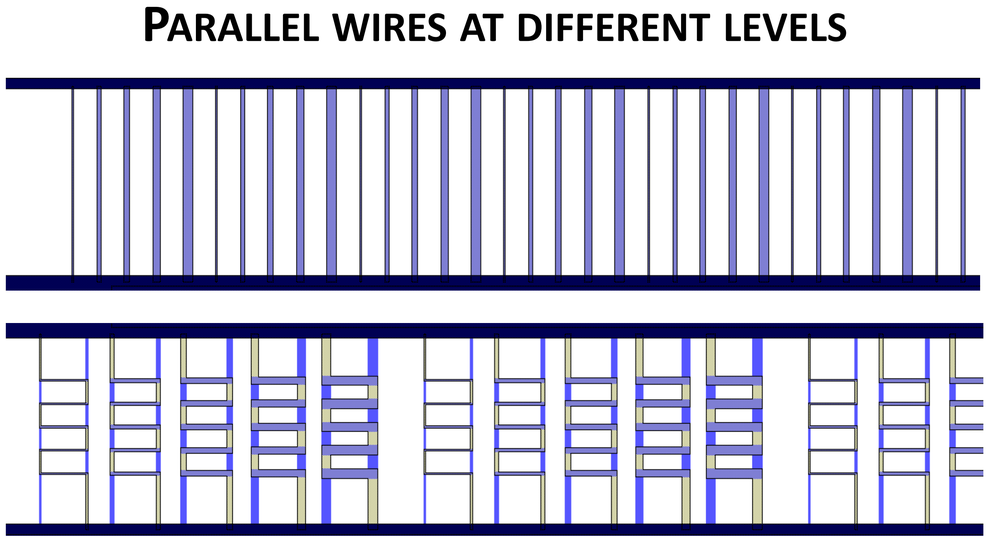
Test chip design concept

Overall view



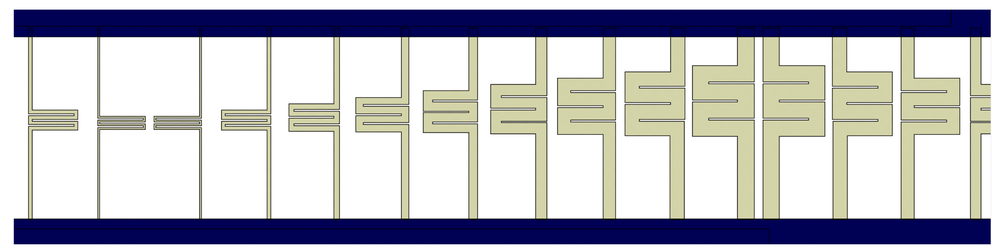


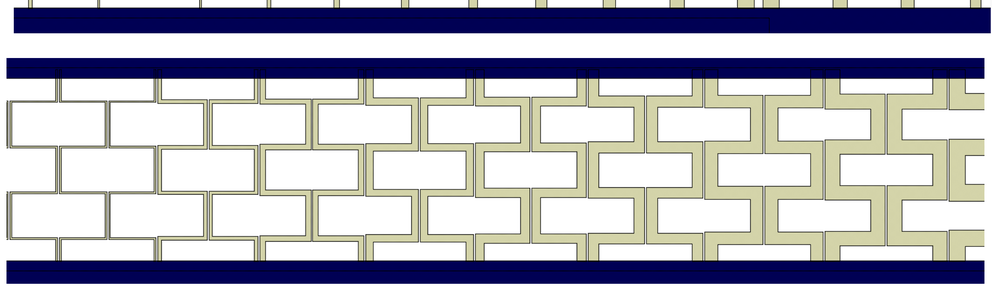
Parallel wires at different levels



This part simulates that the parallel metal lines buried at different level. The upper layout simulates that the two lines have the same direction of current flow. (The wires at different levels are overlapped) The lower layout simulates the current flows in reverse condition. As all the lines have the same current direction (top to bottom or reverse), the overlapped horizontal parts of the wire has the reversed current flow inside.

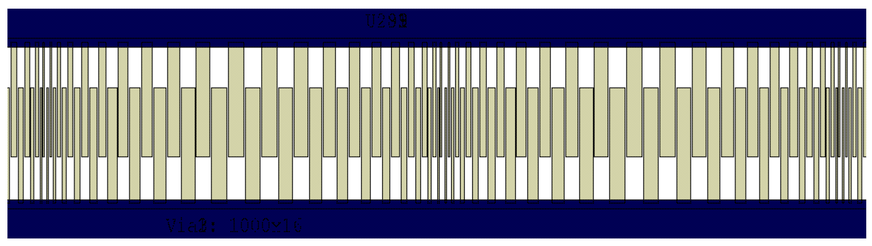
Parallel wires at the same level





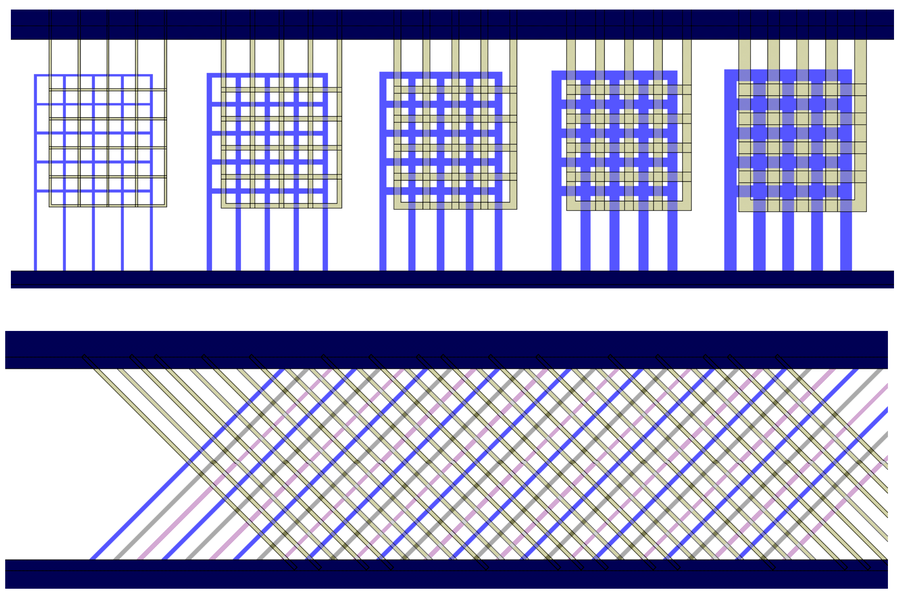
The upper layout simulates current flow in the reverse direction while the lower layout simulates current flow in the same direction. Due to electromagnetic effect, the neighbor wires are expecting different electrical properties. The line length are identical in these two cases.

Cross finger feature



The potential influences from close neighbor wires can be simulated. The upper and lower wires biases can be tuned differently to estimate such influences. Different clearance and finger thicknesses have been designed.

Perpendicular wires at different levels



Perpendicular lines at different levels are simulated.
In upper layout, the upper part of the wire can have potential differences with the lower part of wire. The surface potential information can be collected by Kelvin Force Microscopy (KFM) to observe the electrical field influence from the subsurface structures.
In the lower layout, the metal lines at different levels are rotated at 45° in contradict ways to create a 90° of cross-line. The cross talk of multi-level lines are simulated. In addition, some parts of lines (upper right and lower right) are not crossed and can be taken as reference

Reference

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