

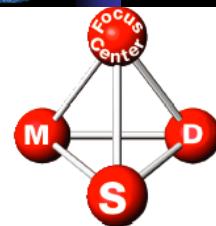
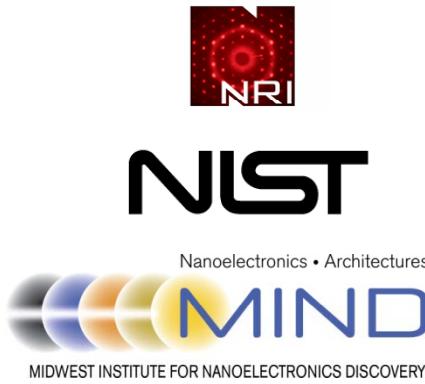
X-RAY PHOTOELECTRON SPECTROSCOPY OF NANOMATERIALS – GRAPHENE AND III-V INTERFACES

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SWAN



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Outline

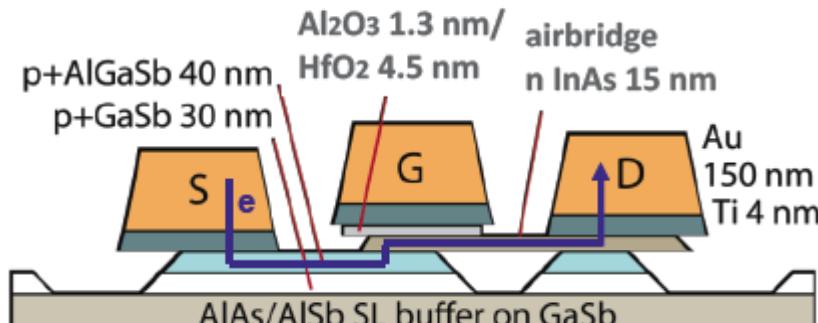
- Background and Motivation
- Experimental Methods
- Results
 - In-situ vs. Ex-situ methods
 - Arsenide Studies
 - Phosphide Studies
 - Antimonide Studies
 - Nitride Studies
 - Graphene
- Conclusions

Outline

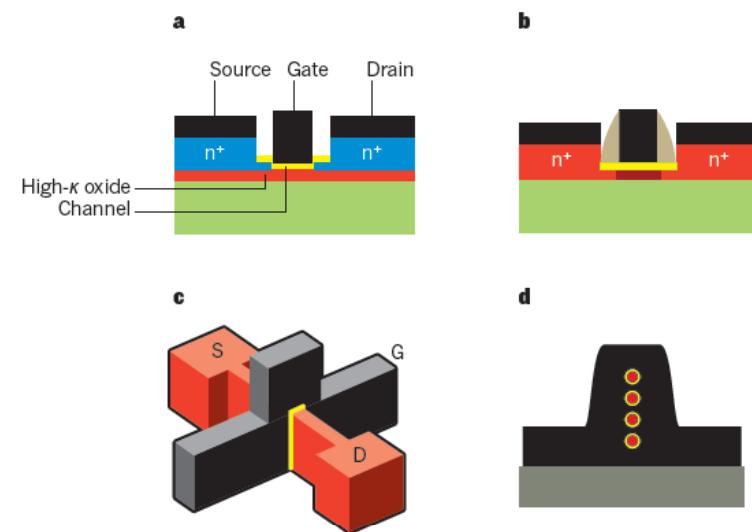
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Motivation

- CMOS performance requirements point toward alternative...
 - Materials (e.g., III-V)
 - Structures (planar → 3D Fin FET → Gate all around)
 - Devices (MOSFET → TFET)

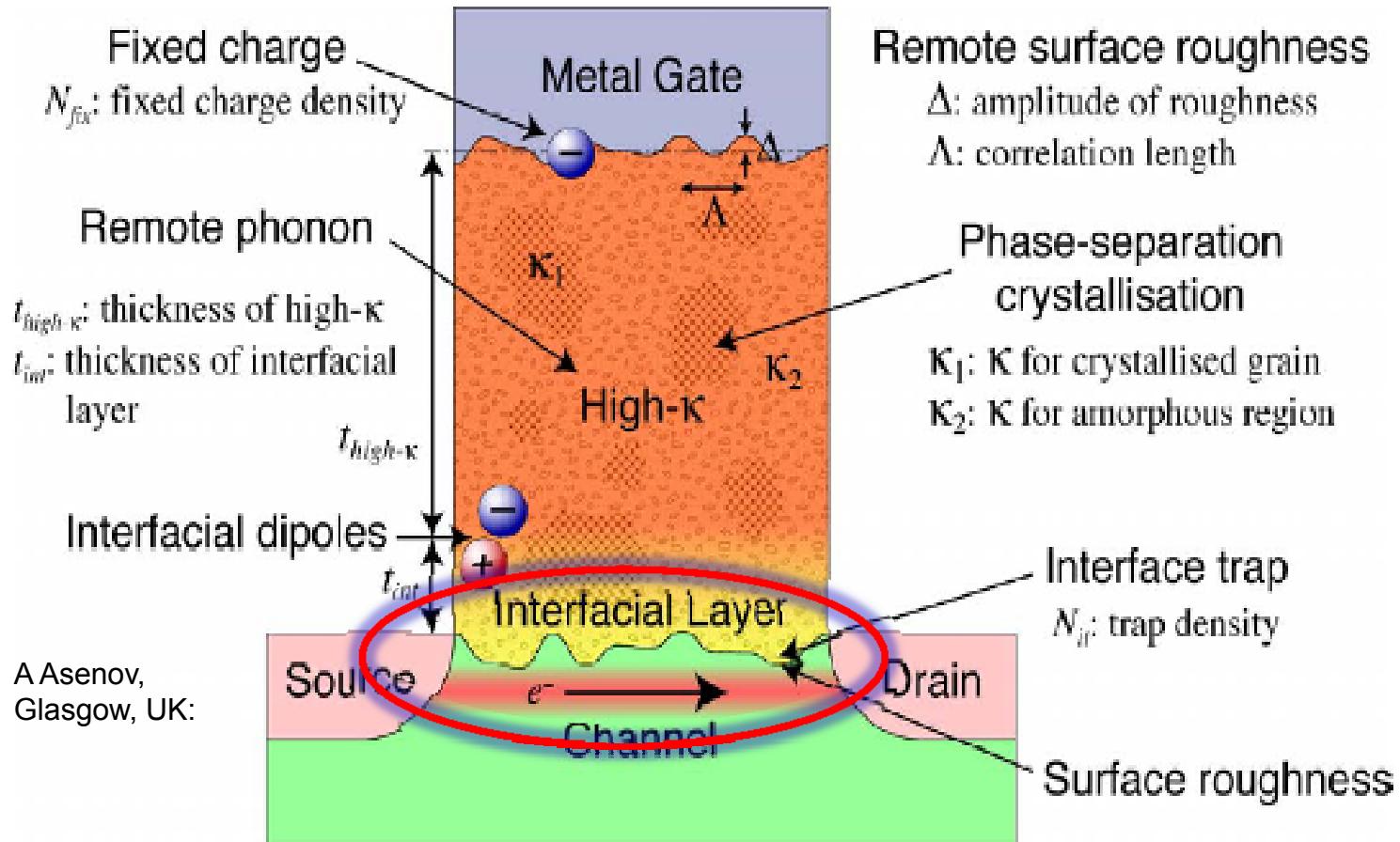


Seabaugh, et al.



Del Alamo Nature (2011)

Interfaces, interfaces....

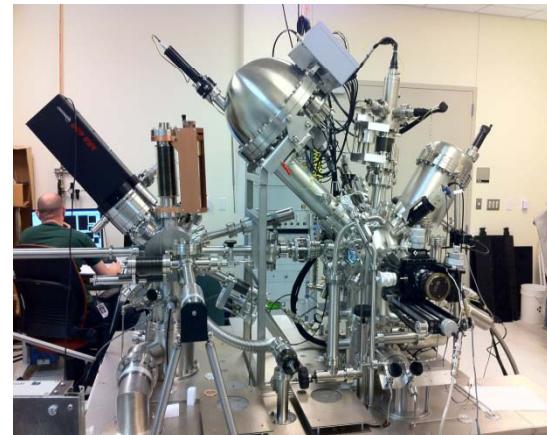
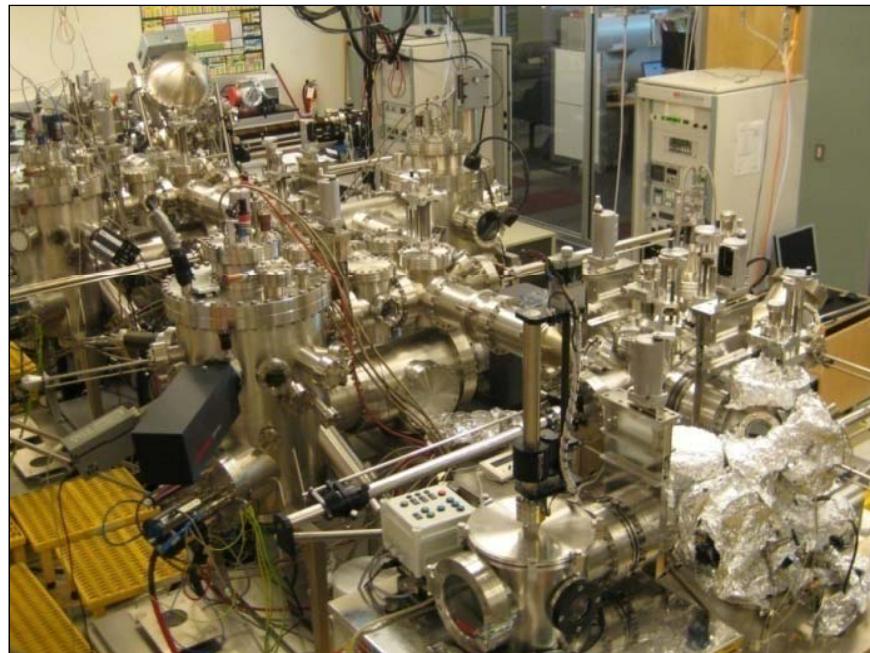


Outline: III-V

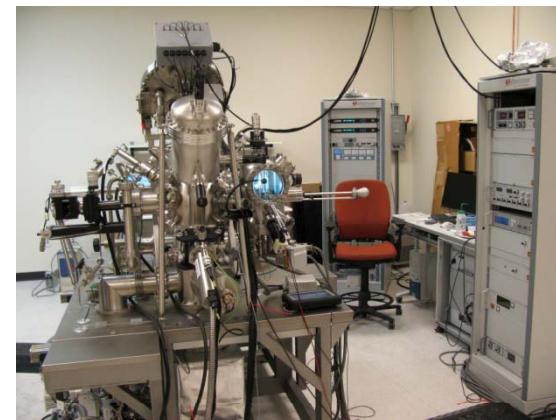
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Tools for *in-situ* studies of interfaces...

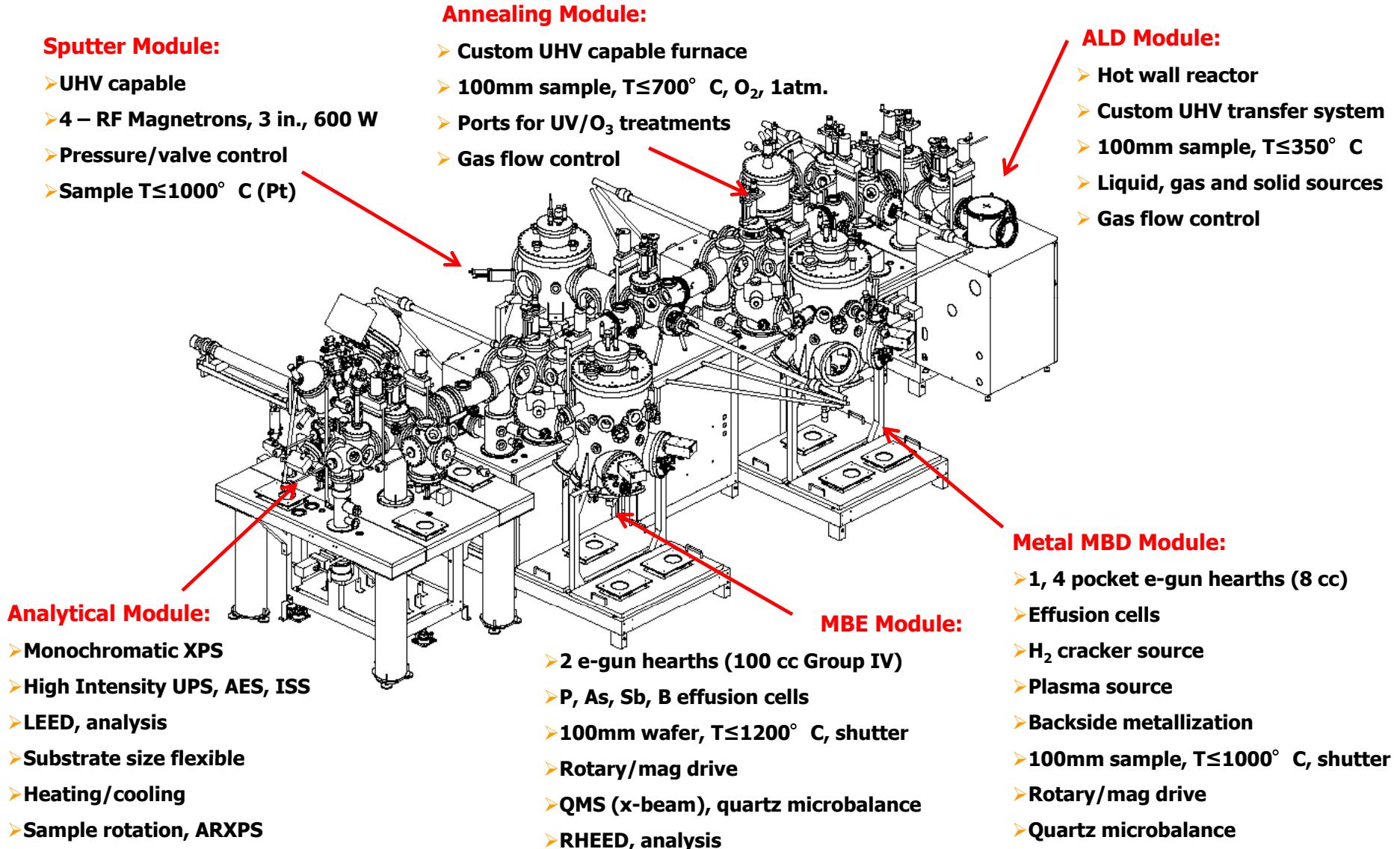
UHV Surface Science System



UHV Cluster System

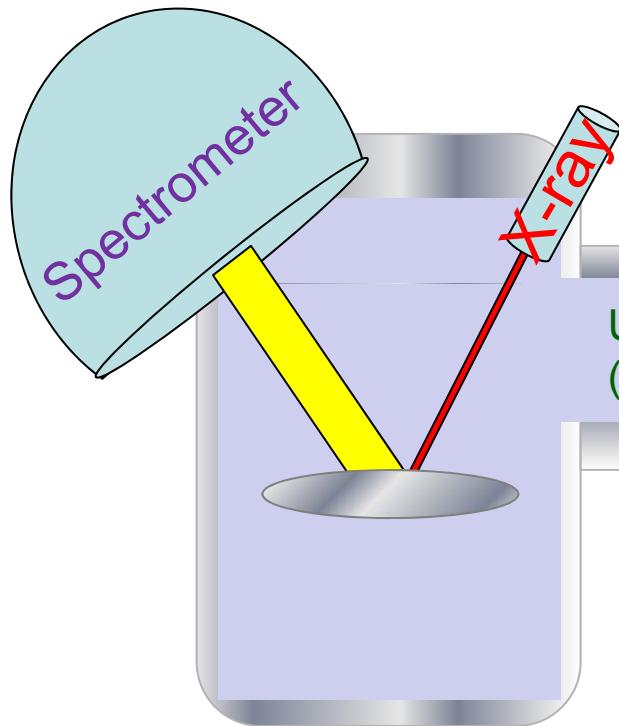


In-situ deposition and analysis system



In-situ half cycle ALD reactions study by XPS

High Resolution Monochromatic XPS



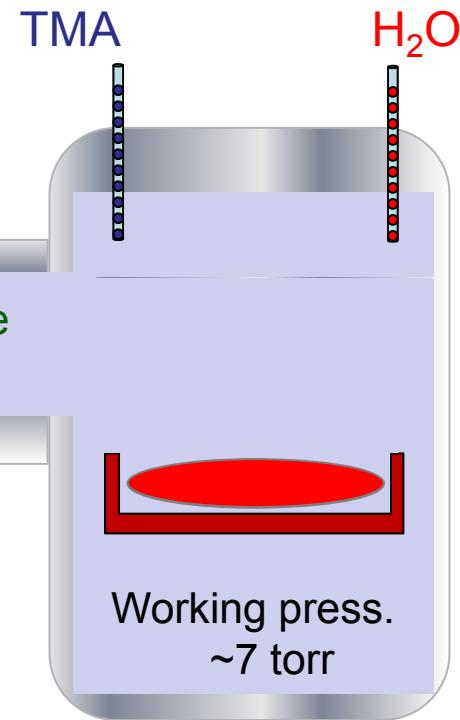
XPS Analysis

Pre-substrate Scan

Analysis after 1st Al pulse

Analysis after 1st H₂O pulse

Picosun ALD
Hot wall and Shower head type

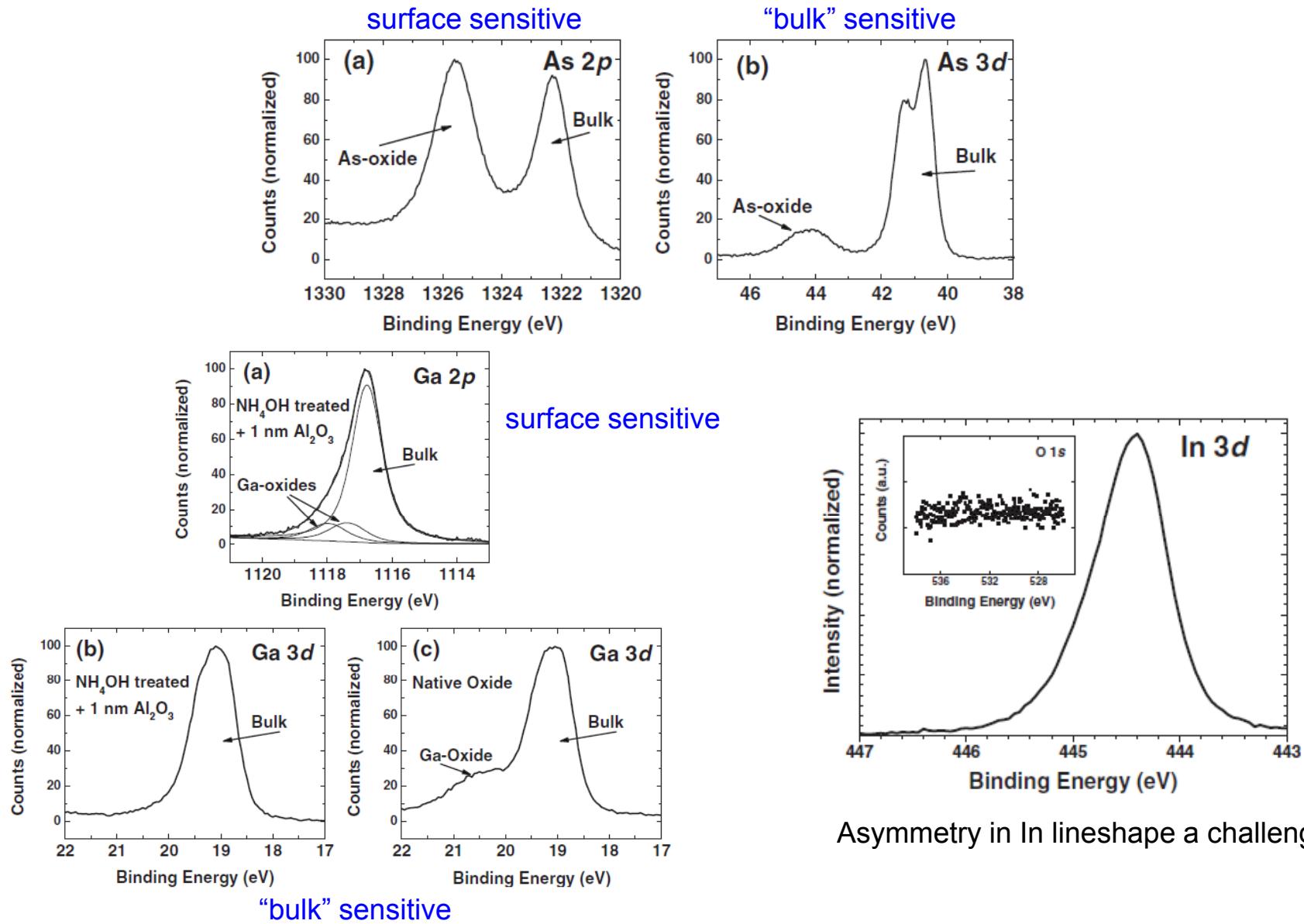


ALD (Al & H₂O)

Al pulse

H₂O pulse

XPS of Arsenides

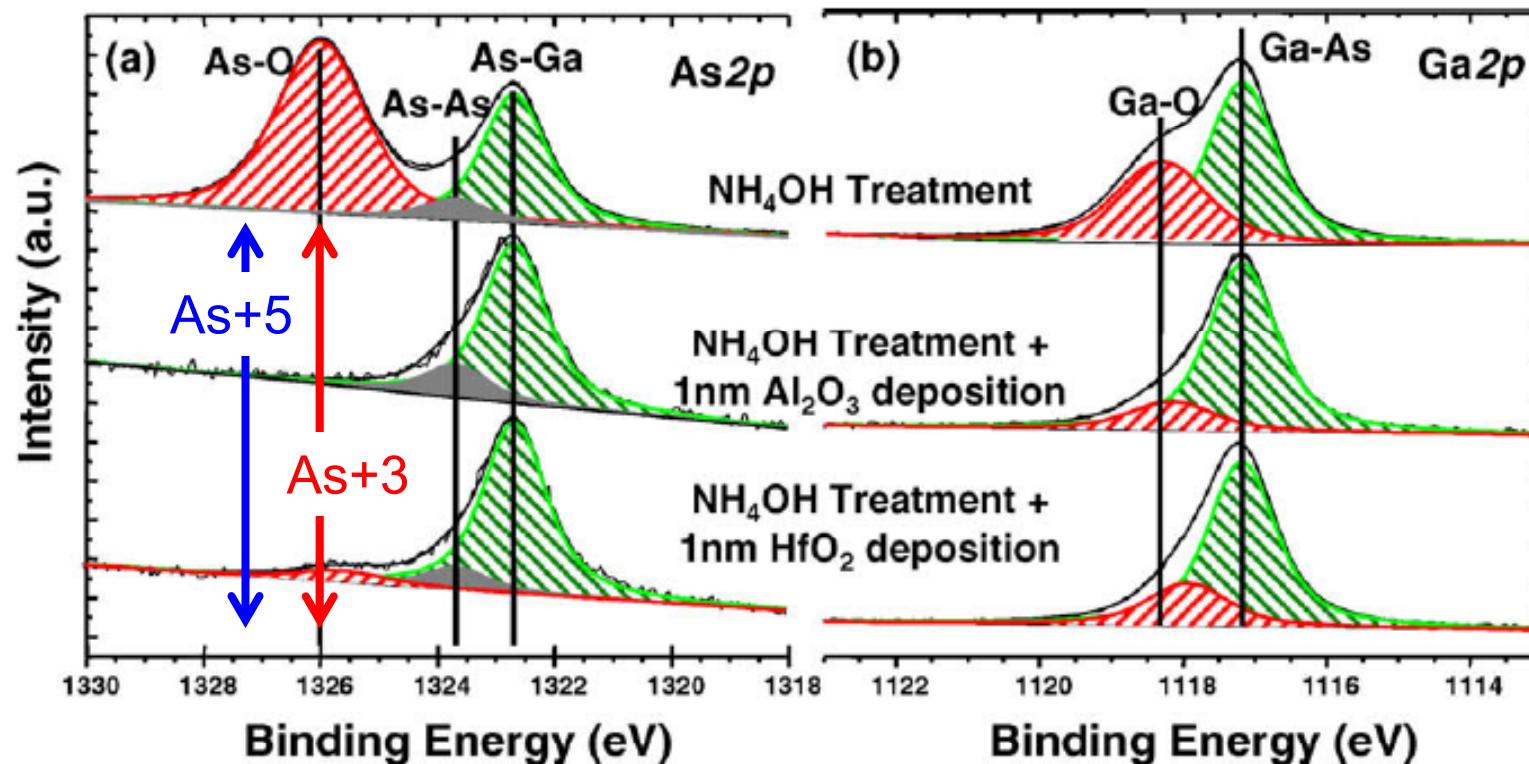


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The “Cleanup Effect”: ALD process and interfacial chemistry on GaAs

Oxide reduction of NH₄OH treated GaAs surface following ALD deposition

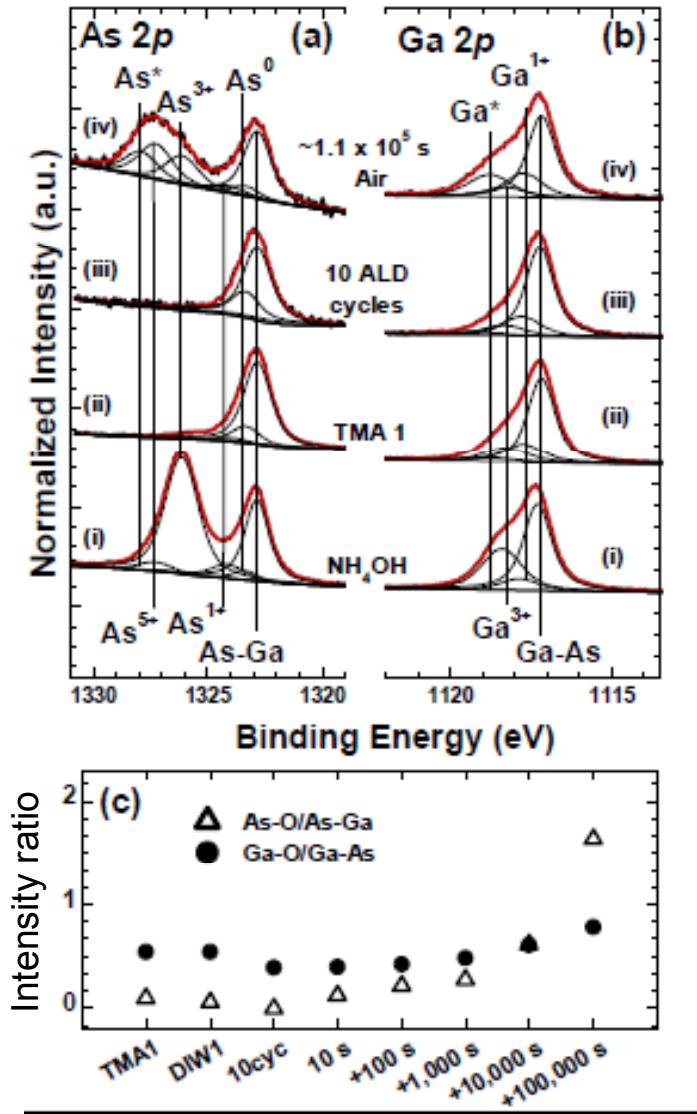


- ALD Process reduces As-oxides readily
- ALD process impacts Ga-oxides as well, but some Ga-oxide remains
- The ALD precursors remove *different* As oxidation states.
 - TMA removes the As³⁺ state while TEMAH removes the As⁵⁺ state.

Apparent contradictions in prior interface studies – some examples

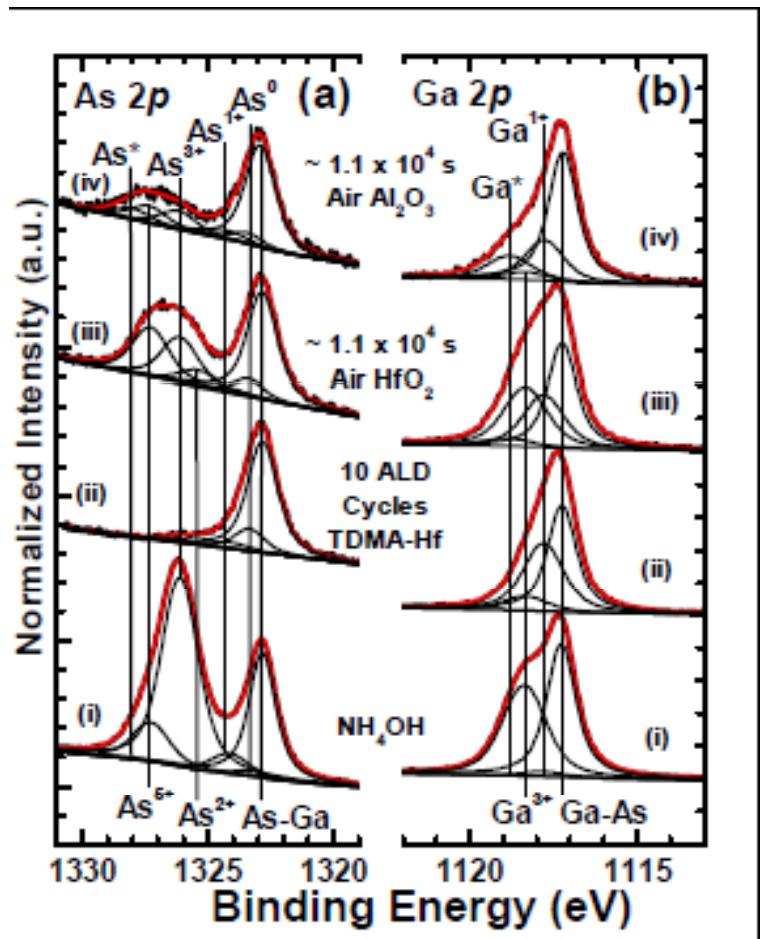
- Dalapati, et al. (IEEE TED 54 (2007) 1831)
 - concluded via ex situ XPS that both 1 nm Al_2O_3 and HfO_2 films had detectable arsenic oxides present at the oxide/semiconductor interface
- Suri, et al. (APL 96 (2010) 112905)
 - concluded via ex situ XPS no significant arsenic oxide reduction using TDMA-Hf at 200°C
- Hackley, et al. (APL 92 (2008) 162902)
 - Concluded that there is a thickness dependence to the oxide “clean-up” effect
- Shahrjerdi, et al. (APL 91 (2007) 193505)
 - Concluded via ex situ XPS no significant reduction of AsO_x upon deposition of HfO_2 on GaAs using TDMA-Hf

In-situ vs. Ex-situ Studies: TMA and GaAs



- NH₄OH-treated GaAs
- TMA exposure reduces oxides
- Exposure to air results in oxidation
 - GaAsO₄/hydroxide formation

In-situ vs. Ex-situ Studies: TDMA-Hf and GaAs



- NH₄OH-treated GaAs
- TDMA-Hf exposure reduces oxides
- Exposure to air results in oxidation
 - GaAsO₄/hydroxide formation
- Al₂O₃ interface oxidation less than that detected for HfO₂
- Suggests that caution is needed in concluding mechanisms from ex-situ studies of thin (<5nm) films

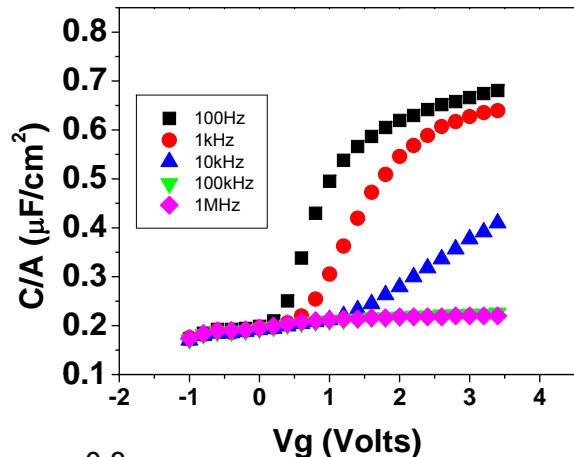
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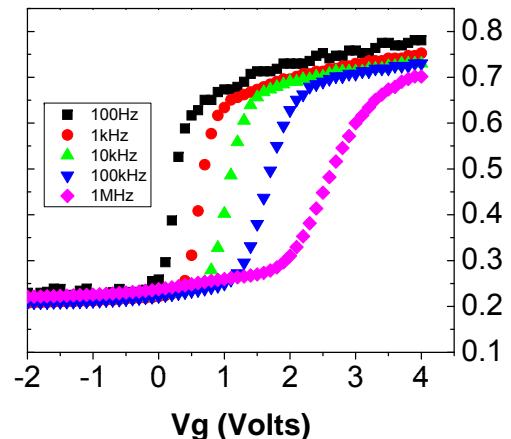
CV and high-k III-Arsenides

Data

NH₄OH Clean/ Si interlayer/1.1 nm Si/10nm Al₂O₃
(oxide at interface)

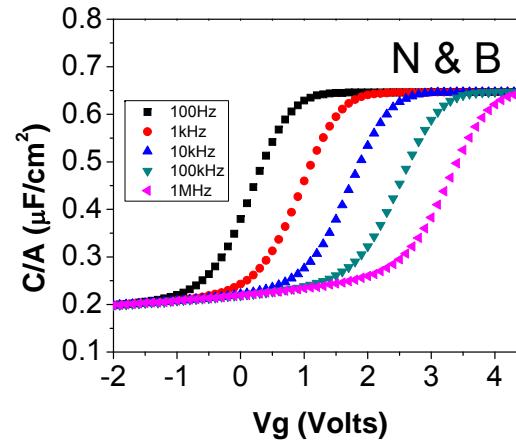
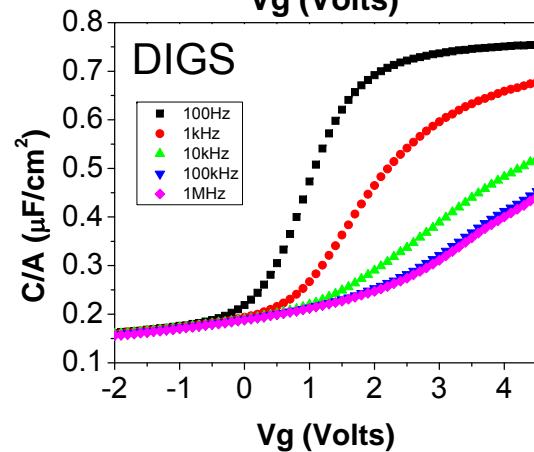


Atomic Hydrogen/ Si interlayer/1.1 nm Si/10nm Al₂O₃
(No oxide at interface)



Models

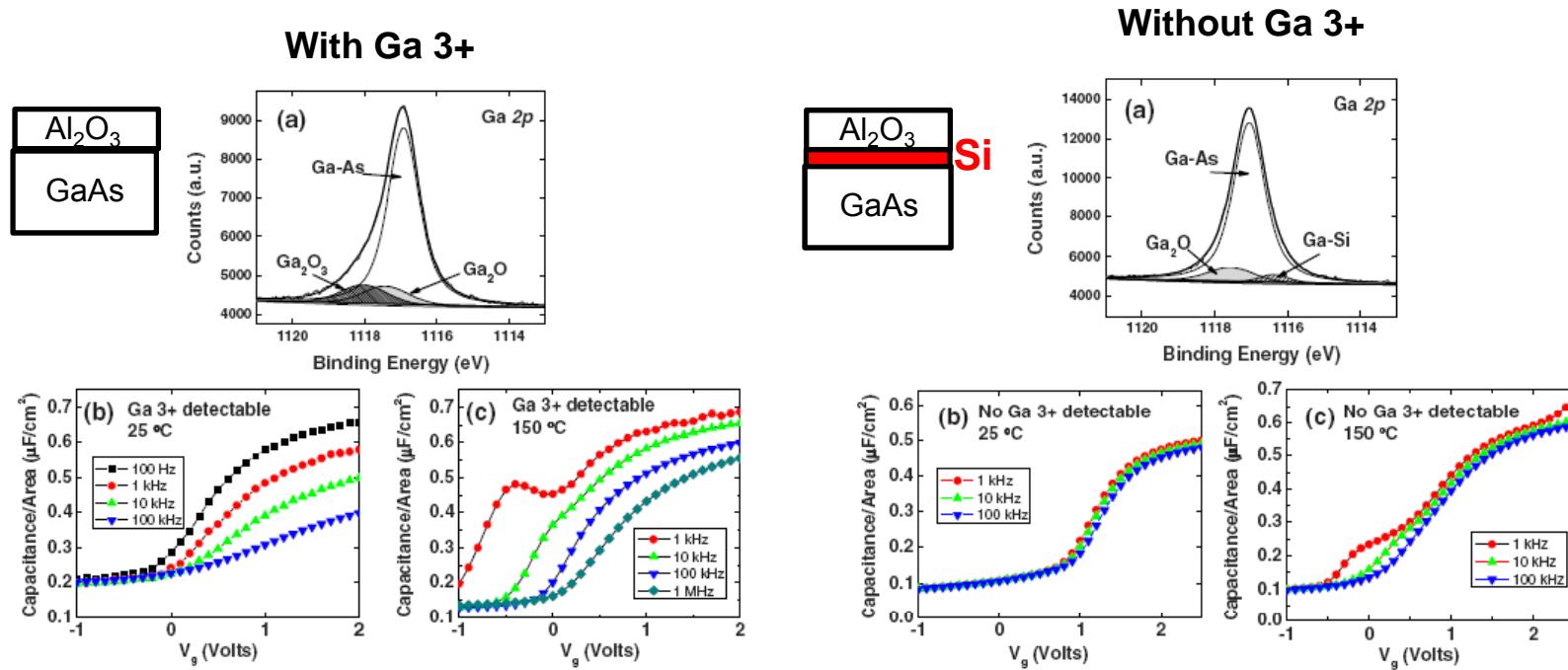
$$D_{it} = 5 \times 10^{13} \text{ cm}^{-2} \text{ eV}^{-1}$$



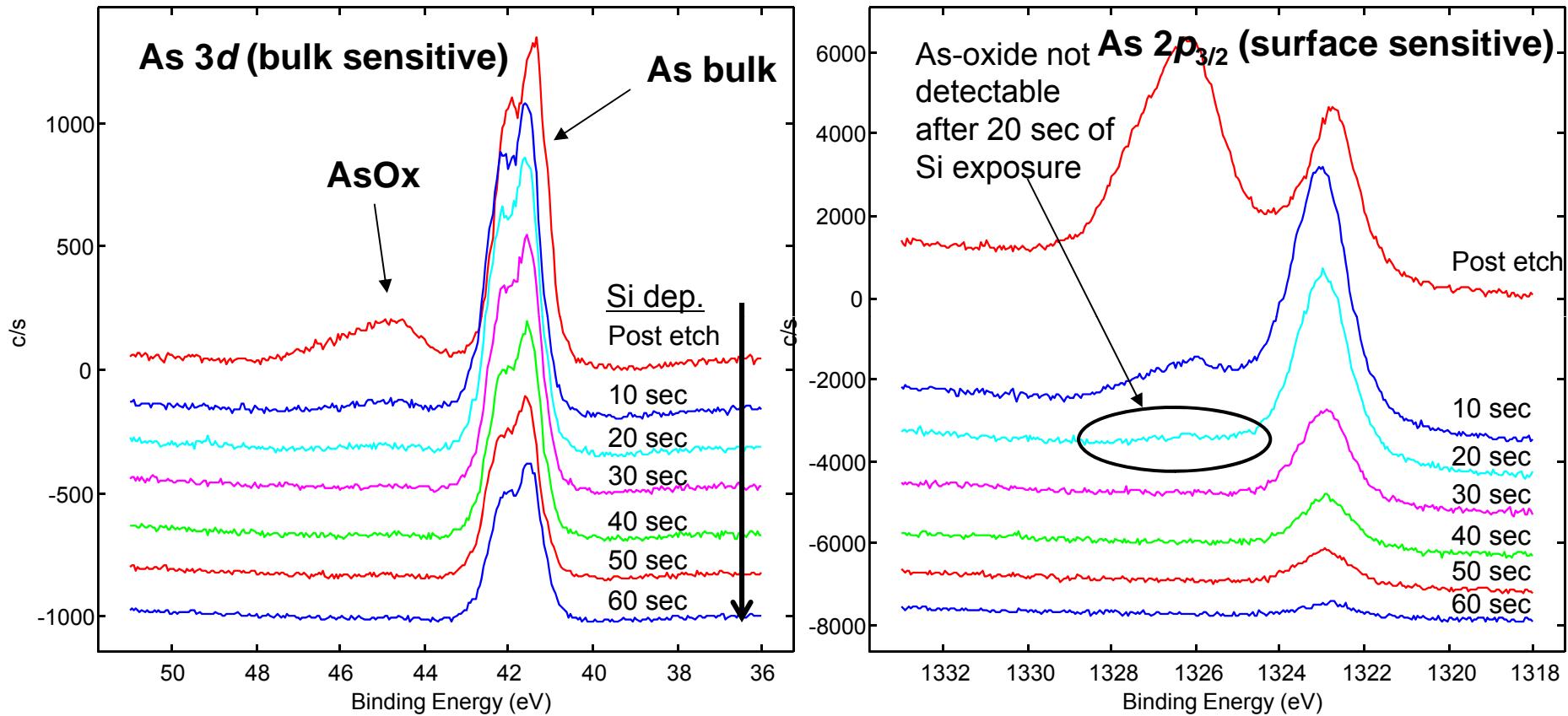
- Marked reduction in accumulation capacitance frequency dispersion.
- The starting surface with its lack of oxygen from atomic H cleaning appears to be the key.
- The primary difference between the N&B interface state model and the H&S model is a low bandgap interlayer (assumed to be disordered) permitting tunneling of carriers to defects.

Effect of Si-IPL on device performance

- Prior work on high-k/III-Arsenides
 - $\text{Al}_2\text{O}_3/\text{GaAs}$
 - $\text{Al}_2\text{O}_3/\text{In}_x\text{Ga}_{1-x}\text{As}$
 - $\text{Al}_2\text{O}_3/\text{InAs}$
- Defect formation and oxidation
- Correlated capacitor and transistor performance with interfacial properties

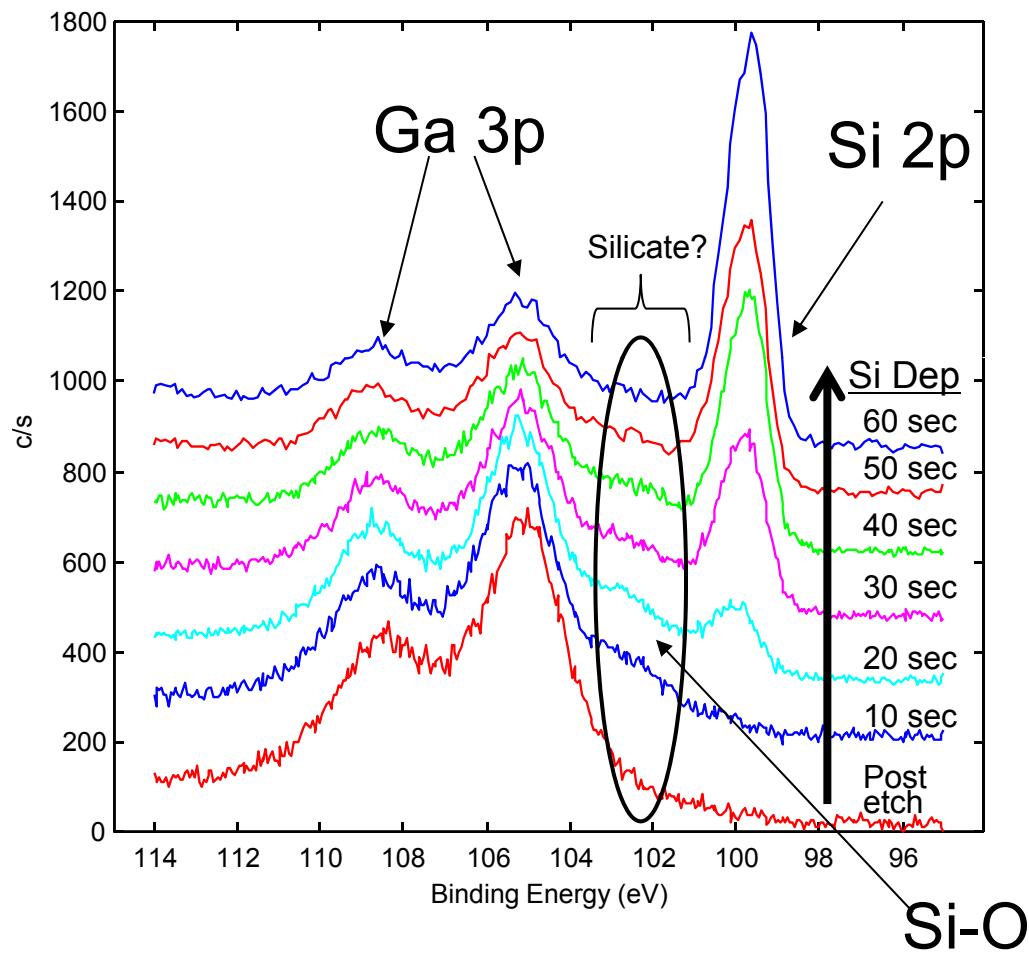


Removal of As-Oxides: NH_4OH etch + anneals+ Si interlayer



- As-O bonding can be removed easily through a variety of techniques including ALD ligand exchange, a-Si deposition, and chemical and thermal treatments.

Surface oxide evolution with processing: NH_4OH etch + anneals+ Si interlayer

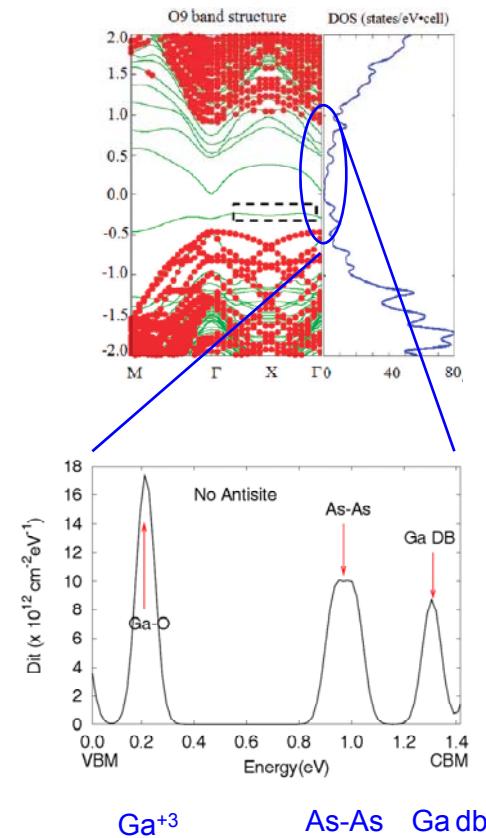
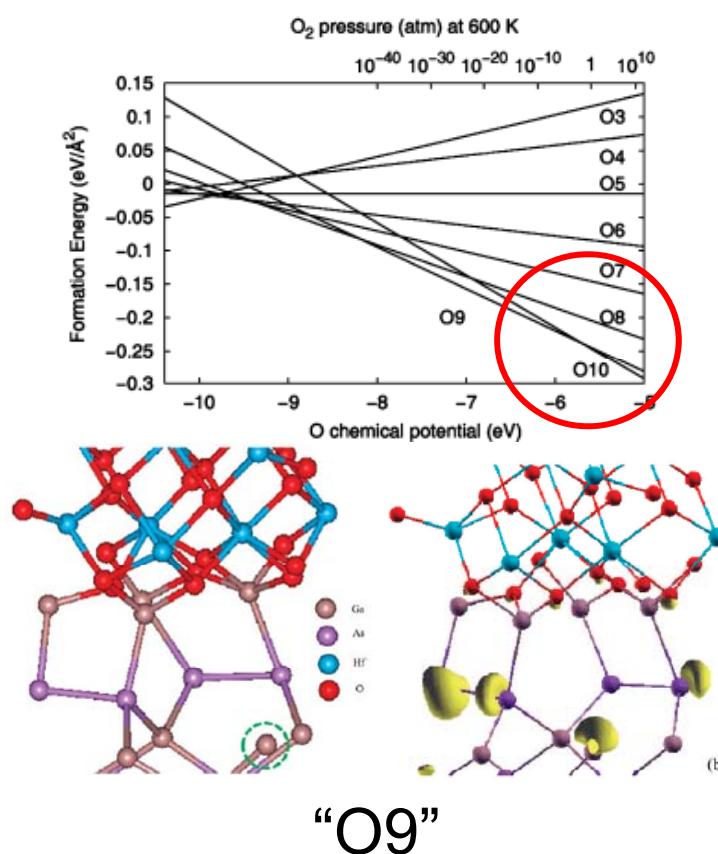


- Silicon is initially detected as Si-O (~10 s of Si flux exposure)
- The detection of Si-Si bonds after 20s coincides with the reduction of As-O below detection limits.
- This implies an initial bond conversion from As-O to Si-O from *in-situ* process
- Subsequent ALD likely to result in a thin silicate high-k layer with elemental Si fully consumed.
- Compare to *ex-situ* XPS results where As-O and As-Si-O formation is reported.*

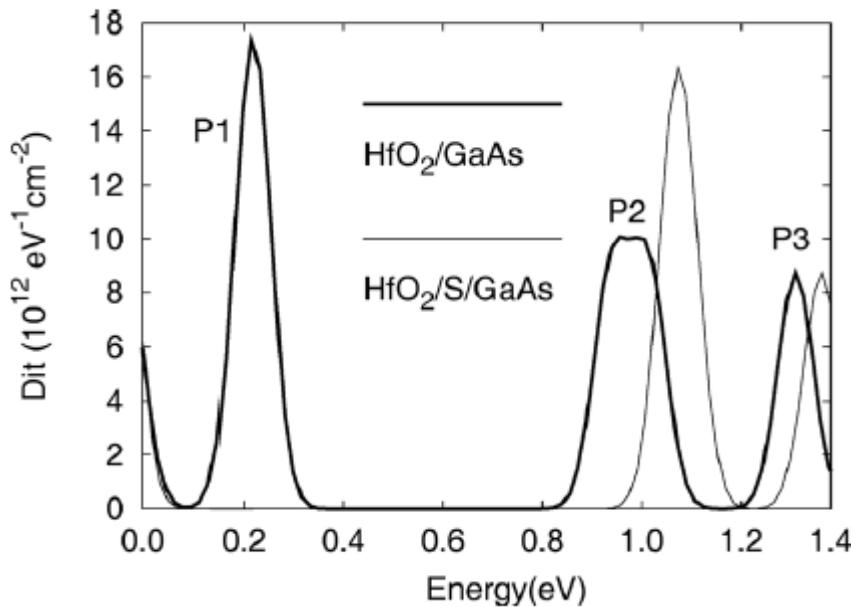
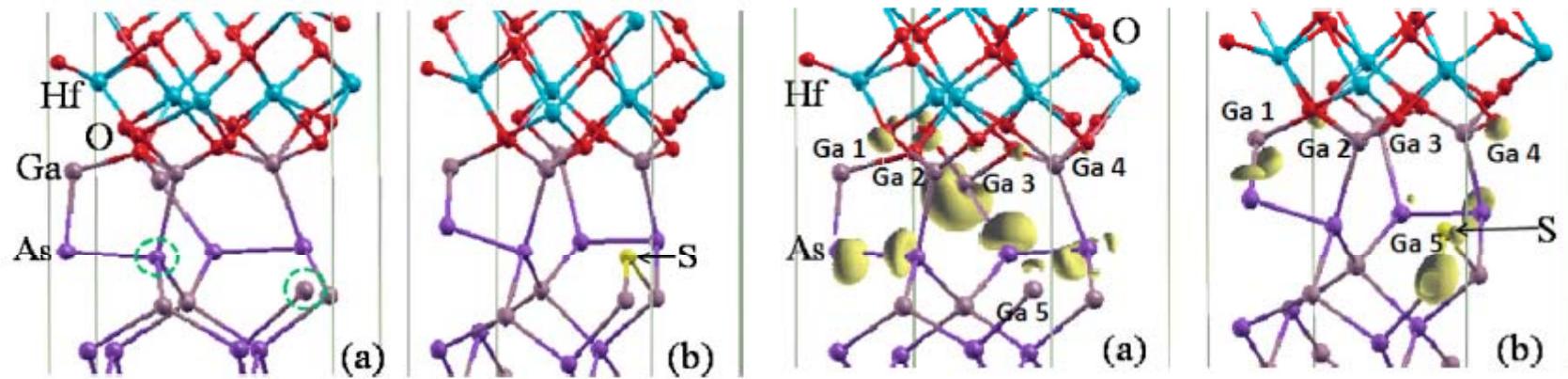
- See: Zhang, et al., J. Appl. Phys. 101 (2007) 034103 and Oktyabrsky, et al., Mat. Sci. Eng. B 135 (2006) 272
- Hasegawa, et al. JJAP 27 (1988) L2265; JVST B 7 (1989) 870; Mat.Sci.Eng. B 165 (2009) 122; JVST B 27 (2009) 2028;

Al_2O_3 /III-Arsenide Interfaces

- DFT Modeling of Effect of Oxidation: strain free HfO_2/GaAs
- O-rich is most stable
- Major defects in gap from oxidation: As-As dimer, Ga db, Ga+3



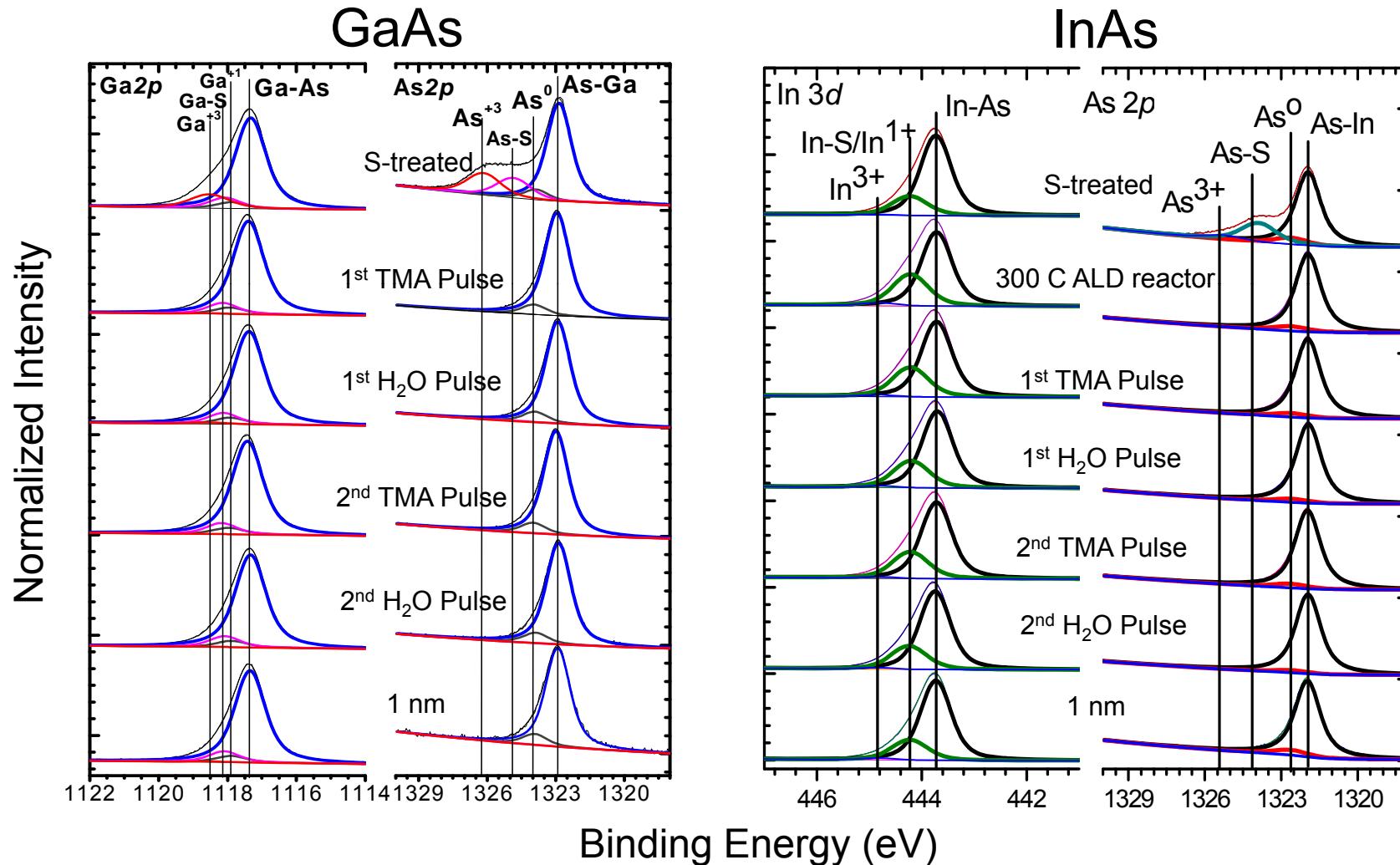
Interface passivation: Sulfur



- S passivation helps mitigate defects from oxidation (Ga+3, As-As, Ga db)
- Defect states move toward the CB edge

S-passivated III-As Interfaces

- Oxidation minimized, but not eliminated by wet chemical treatment
- As^0 (As-As) bonding persistent, though less for In-rich surface



Optimization of S-Passivation: $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$

Table 2
 $(\text{NH}_4)_2\text{S}$ processing parameters for InGaAs samples.

#	Time (min)	Temperature ($^{\circ}\text{C}$)	Concentration (% $(\text{NH}_4)_2\text{S}$)	Pretreatment
(a)	0	RT	0	
(b)	20	RT	22	
(c)	10	RT	22	
(d)	20	RT	22	HCl
(e)	10	RT	22	HCl
(f)	20	40	22	
(g)	20	60	22	
(h)	20	RT	10	
(i)	20	40	10	
(j)	20	60	10	
(k)	20	RT	5	
(l)	20	40	5	
(m)	20	60	5	

Table 4
RMS roughness from AFM measurements of samples after $(\text{NH}_4)_2\text{S}$ and subsequent annealing.

Sample	Treatment	RMS roughness (nm)	
		$1 \mu\text{m} \times 1 \mu\text{m}$	$5 \mu\text{m} \times 5 \mu\text{m}$
(a)		0.29	0.60
(b)	22% RT 20 min	0.29	0.50
(c)	22% RT 10 min	0.24	0.52
(d)	22% RT 20 min HCl	0.27	0.50
(e)	22% RT 10 min HCl	0.40	0.73
(f)	22% 40 $^{\circ}\text{C}$ 20 min	0.38	0.70
(g)	22% 60 $^{\circ}\text{C}$ 20 min	0.45	0.50
(h)	10% RT 20 min	0.20	0.61
(i)	10% 40 $^{\circ}\text{C}$ 20 min	0.33	0.47
(j)	10% 60 $^{\circ}\text{C}$ 20 min	0.33	0.67
(k)	5% RT 20 min	0.31	1.16
(l)	5% 40 $^{\circ}\text{C}$ 20 min	0.14	0.33
(m)	5% 60 $^{\circ}\text{C}$ 20 min	0.21	0.47

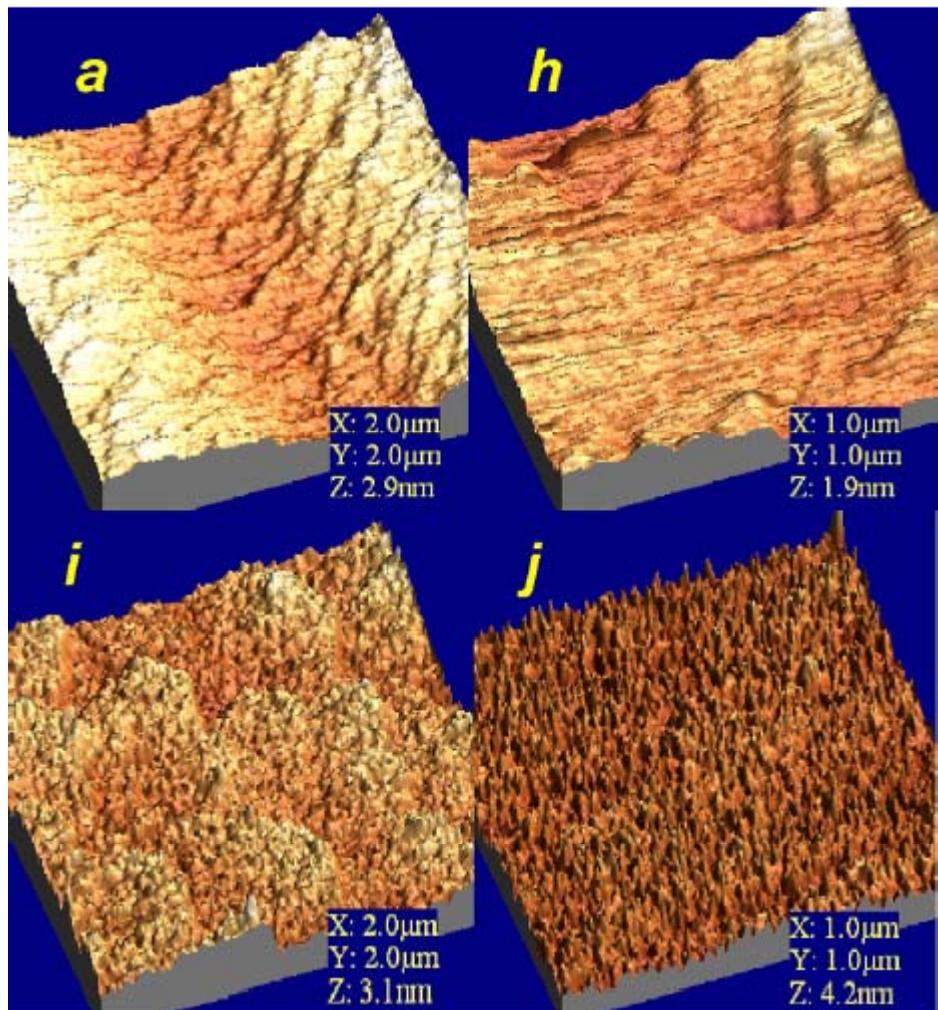
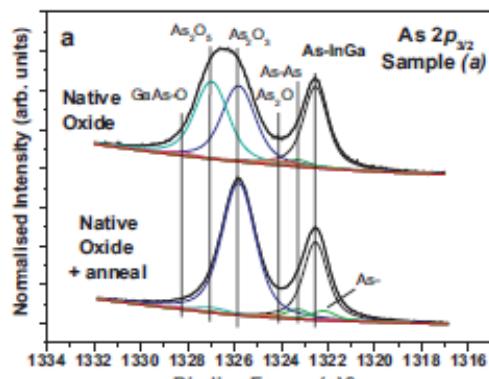


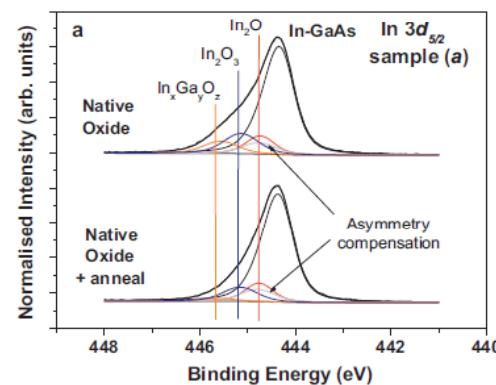
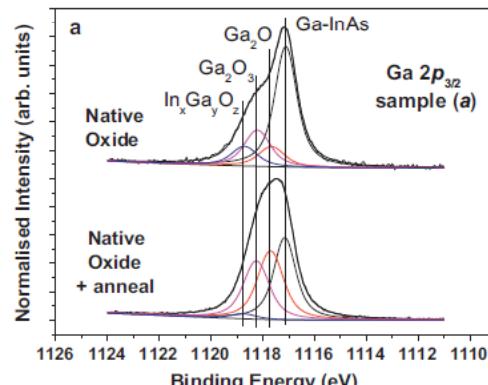
Fig. 8. AFM images from samples (a) and (h–j) with $1 \mu\text{m} \times 1 \mu\text{m}$ and $2 \mu\text{m} \times 2 \mu\text{m}$ scan areas after $(\text{NH}_4)_2\text{S}$ treatment and subsequent annealing at 300 $^{\circ}\text{C}$.

Optimization of S-Passivation: $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$

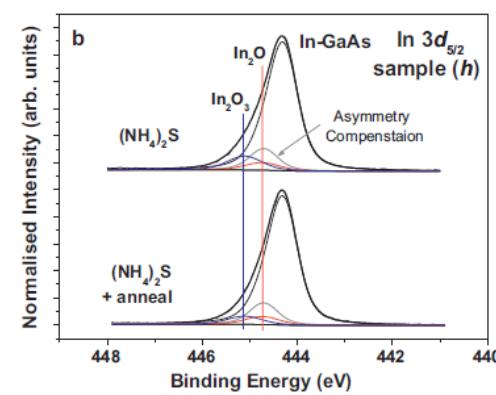
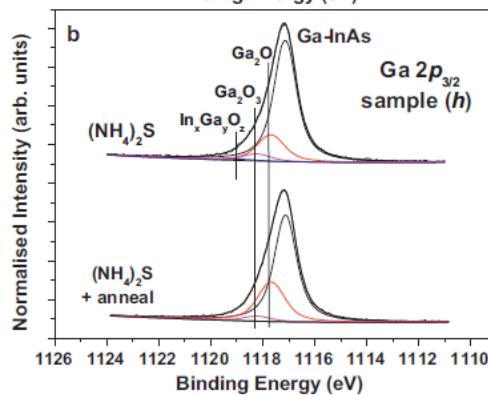
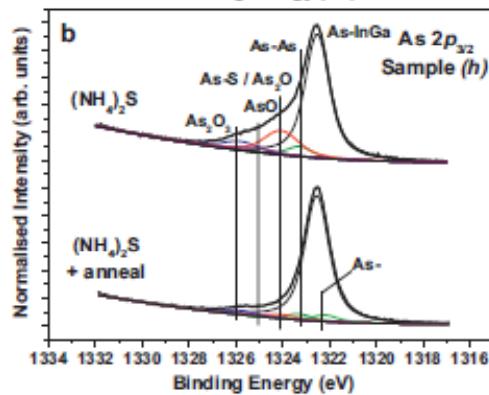
Native oxide



Anneal: 300°C in vacuum (ALD reactor)



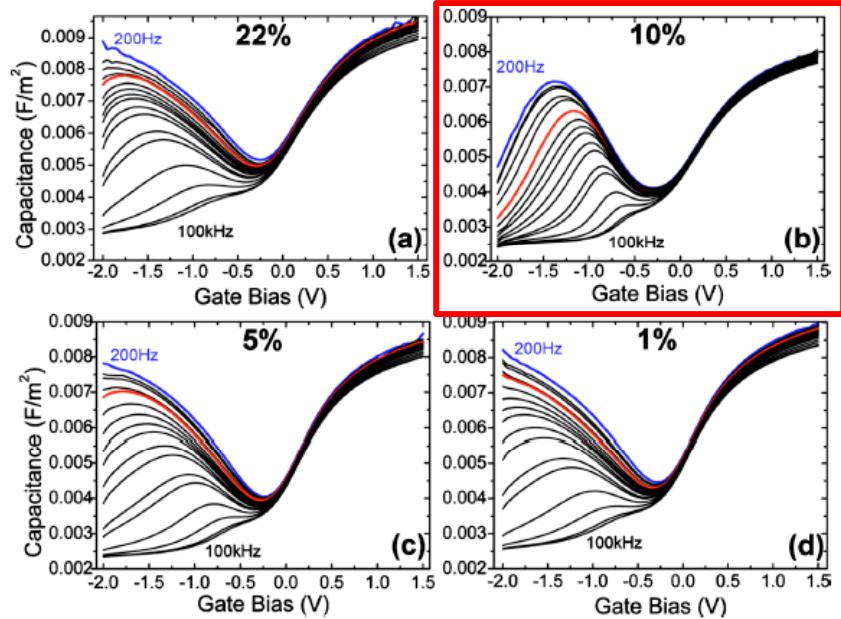
Optimized



- Optimized wet S-passivation: 10% $(\text{NH}_4)_2\text{S}$, Room Temp., 20 min + DIW rinse
- Native oxides reduced and reoxidation inhibited
- Anneal results in further oxide reduction and minimized As-As formation
- Interfacial roughness minimized

Optimization of S-Passivation: $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$

n-In_{0.53}Ga_{0.47}As



p-In_{0.53}Ga_{0.47}As

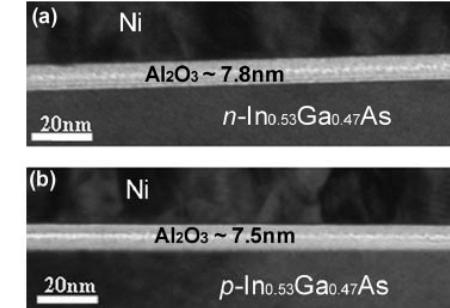
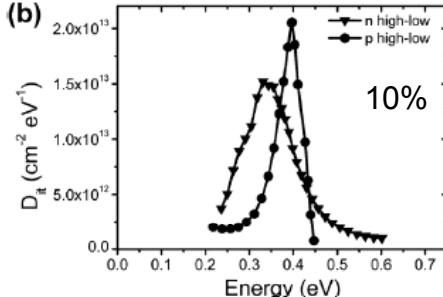
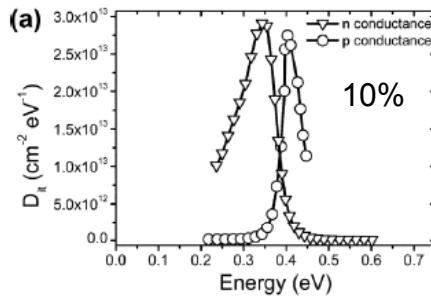
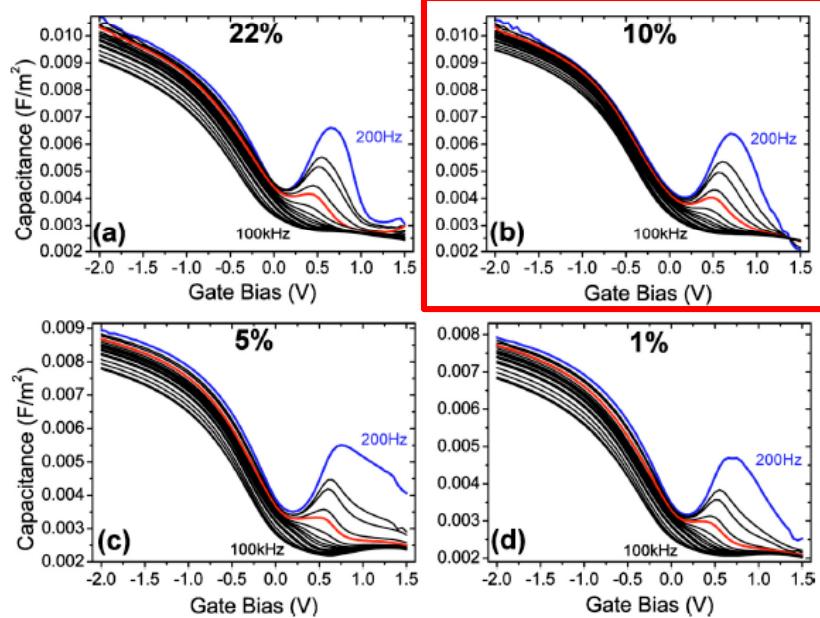


FIG. 1. Cross-sectional TEM micrographs of (a) 10%(NH_4S) treated, $\text{Au}/\text{Ni}/7.8\text{ nm Al}_2\text{O}_3/\text{n-In}_{0.53}\text{Ga}_{0.47}\text{As}/\text{InP}$, and (b) 10%(NH_4S) treated, $\text{Au}/\text{Ni}/7.5\text{ nm Al}_2\text{O}_3/\text{p-In}_{0.53}\text{Ga}_{0.47}\text{As}/\text{InP}$ device structures.

- Frequency dispersion minimized for 10% (NH_4S) treatment
- Hysteresis also minimized
- Important to keep post-etch surface exposure to atmosphere minimized as well (<7 min)
- Mid-gap D_{it} remains significant, likely As-As related

Summary: III-V

- Conclusions from ex-situ surface analysis of interfaces must be drawn very carefully
 - In-situ studies can serve as a baseline for interfacial chemistry
 - Enables sorting out extrinsic effects
- High-k on III-arsenides
 - Oxidation leads to defect states (As-As, Ga db) which can be *partially* mitigated
 - Si IPL effective in reducing defect states in interfacial region (e.g., silicate formation)
 - S passivation effective at minimizing reoxidation, and can remain through deposition process
 - In-rich arsenides preferred from defect perspective
- Interfacial region CAN be engineered with clusterable process

[To Gr](#)

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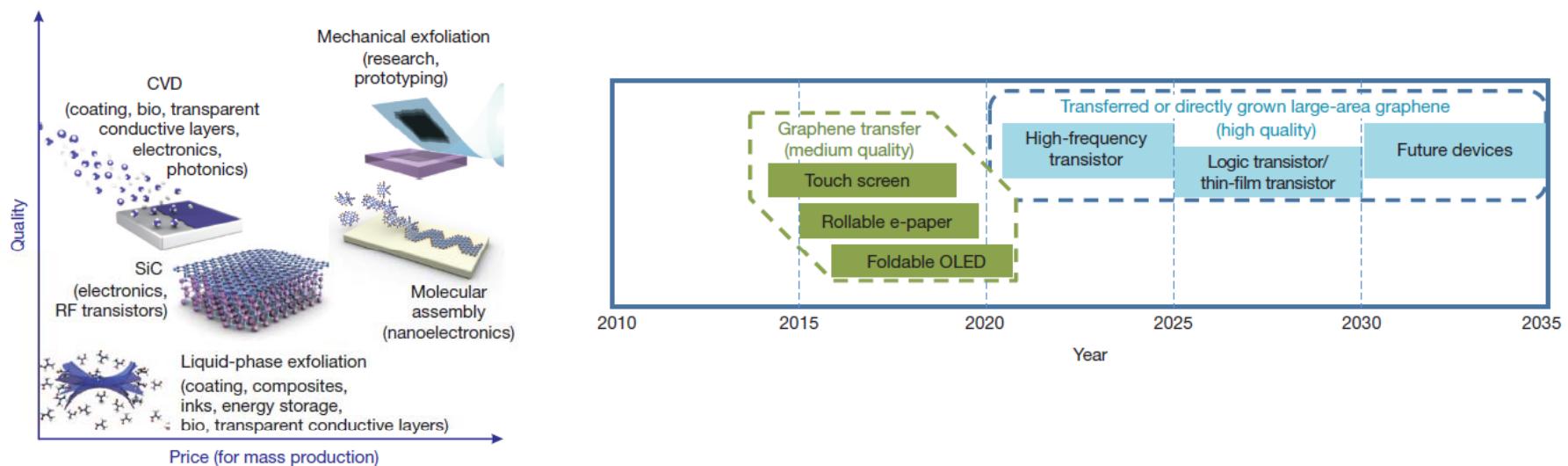
Graphene at a Crossroads

- Transitioning from science to technology
 - Exploiting interesting phenomenon
 - Routes toward integration into useful products
 - Mass production challenges
 - Establishing cost/performance space



Graphene-based Electronics

- Large area synthesis of device quality graphene
- Low cost, reliable CVD (+ transfer) process
- Interaction of contacts
- Interaction of dielectrics
- Packaging (atmospheric exposure/sensitivity)

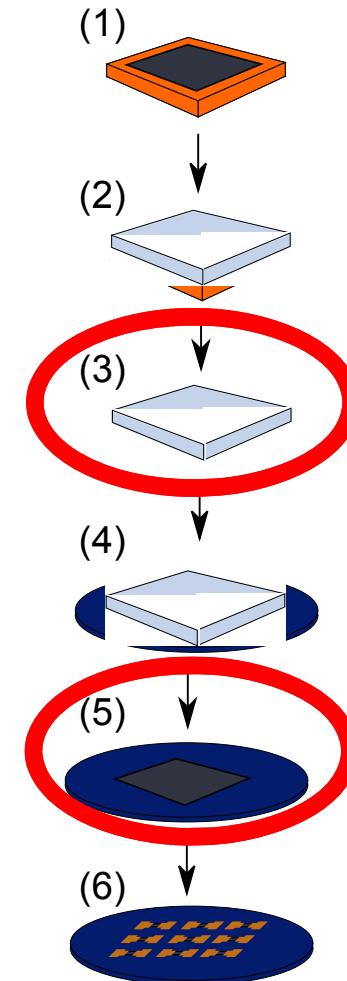


Graphene Transfer Process Flow

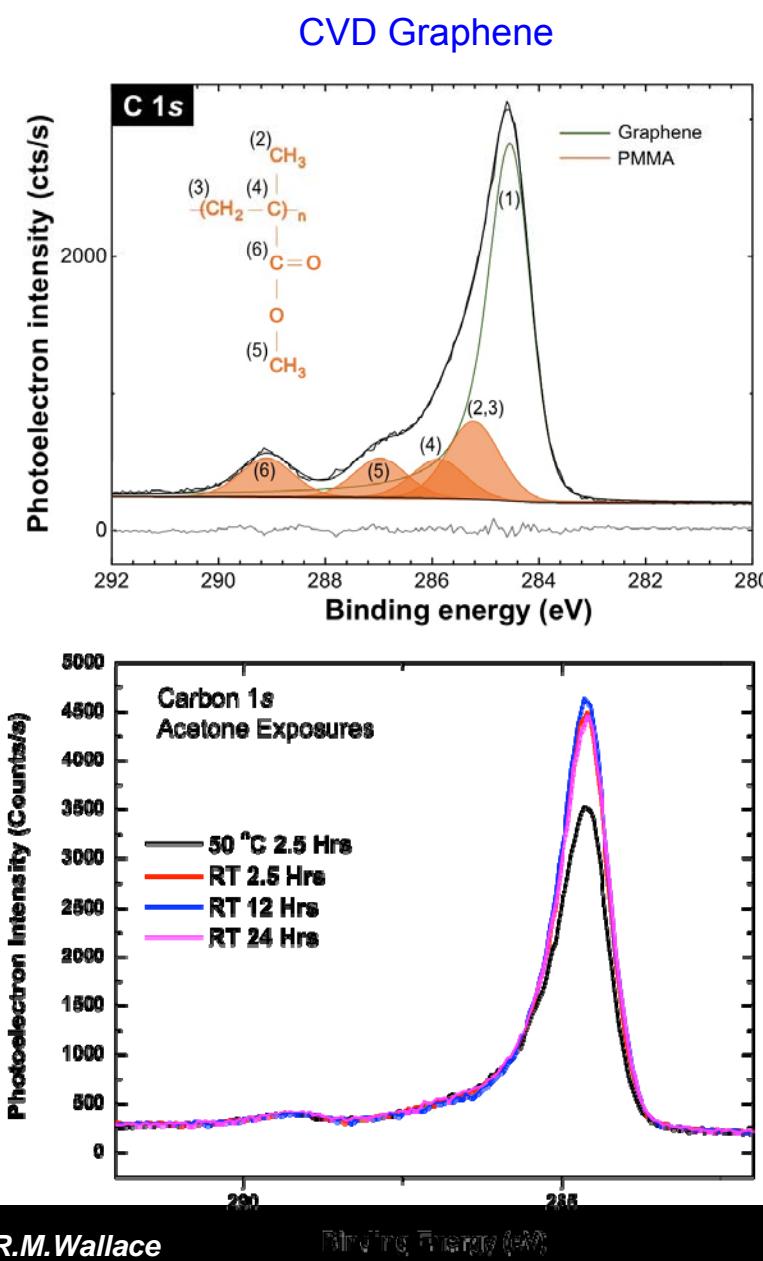
Pioneered By Ruoff's group*

1. Graphene growth on Cu substrate
2. Spin on PMMA dissolved in chlorobenzene.
3. Etch Cu substrate in 3:1 DIW:HNO₃ for 1 min followed by 3 hrs + 15 hrs in fresh ammonium persulfate baths
4. Draw PMMA/graphene membrane onto a SiO₂/Si wafer
5. Remove PMMA “handle” layer in acetone
6. Three-terminal graphene FET fabrication using photolithography

- Steps 3 (the removal of copper) and step 5 (the removal of PMMA) are key points in the transfer process optimization
- Result in reduced chemical residues and increase device performance.



Step 5: PMMA Residue from Transfer Process

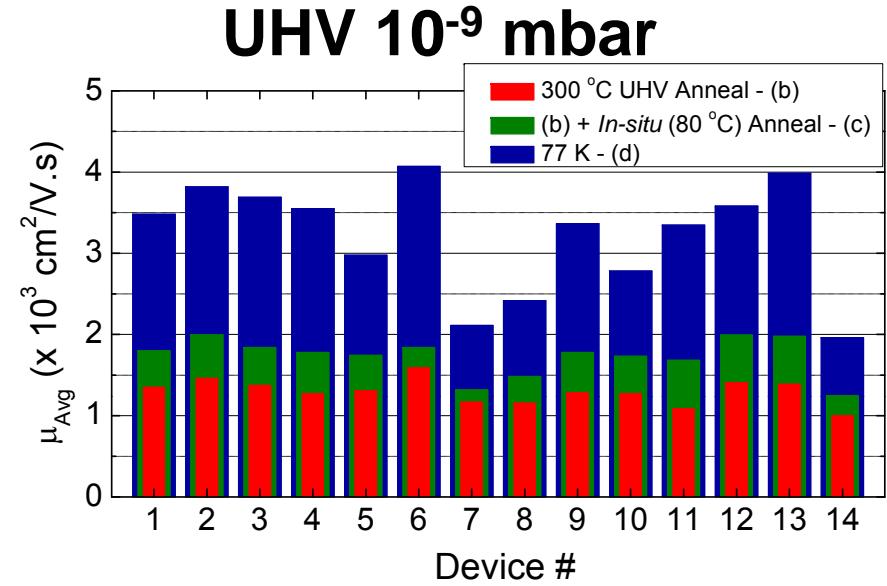
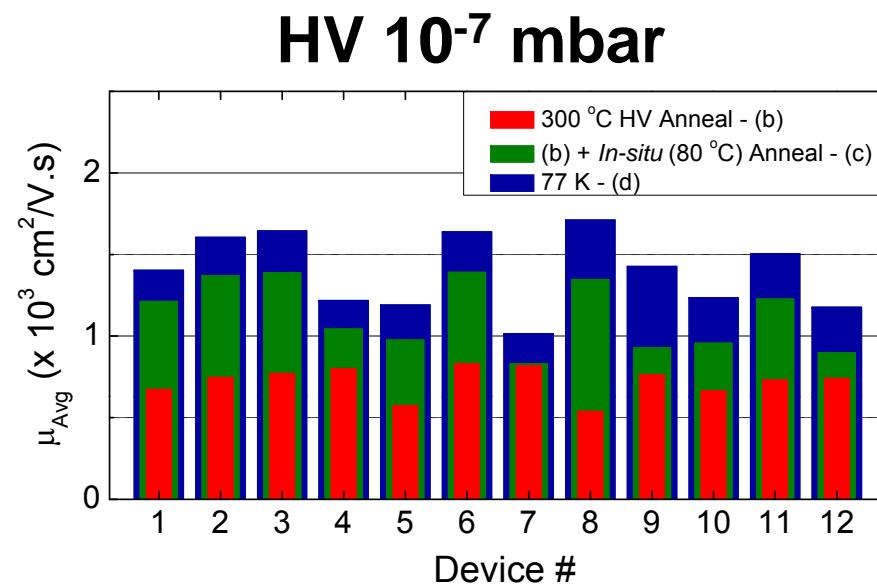


- PMMA ‘handle’ is typically removed with an acetone rinse*
- XPS shows that some PMMA residue is left**
- Longer acetone rinses in hot (~50 °C) acetone have also been reported***
- Longer acetone rinses including hot acetone are shown here to be ineffective at providing an increased reduction to the remnant C=O and C-O bonds concentrations.

References:

- * B. Fallahazad *et al.* Phys Rev B **85** 201408(R) (2012)
- ** A. Pirkle *et al.* Appl. Phys. Lett. **99**(12) 122108 (2011)
- *** Z. Luo *et al.* Chem Mater. **23** 1441 (2011)

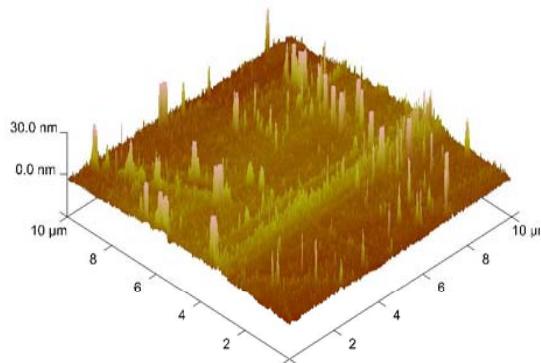
Residue Removal by Vacuum Annealing: UHV vs HV



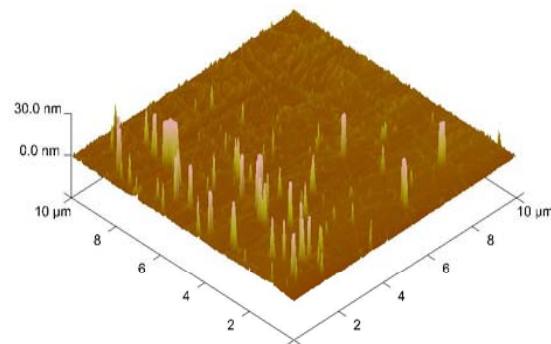
- The UHV anneal result in a factor of 2 increase in the mobility with respect to the HV anneal
- UHV is required for annealing to yield significant mobility increase

High temperature Annealing

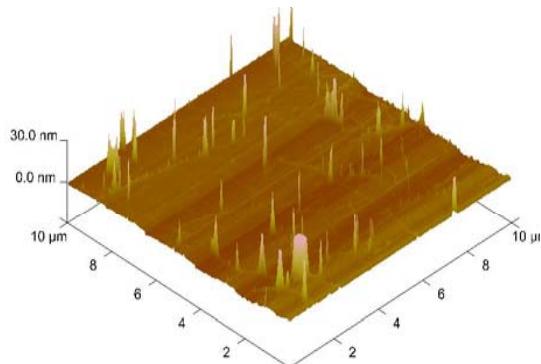
As transferred



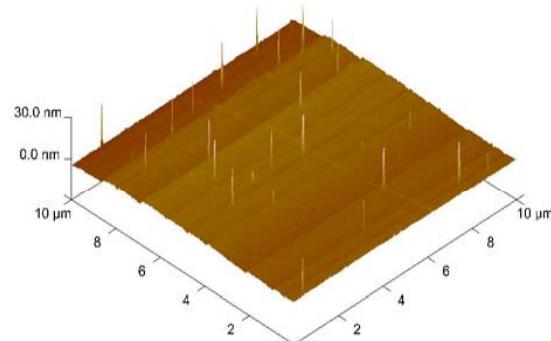
300 °C Anneal



300 °C + Atomic H

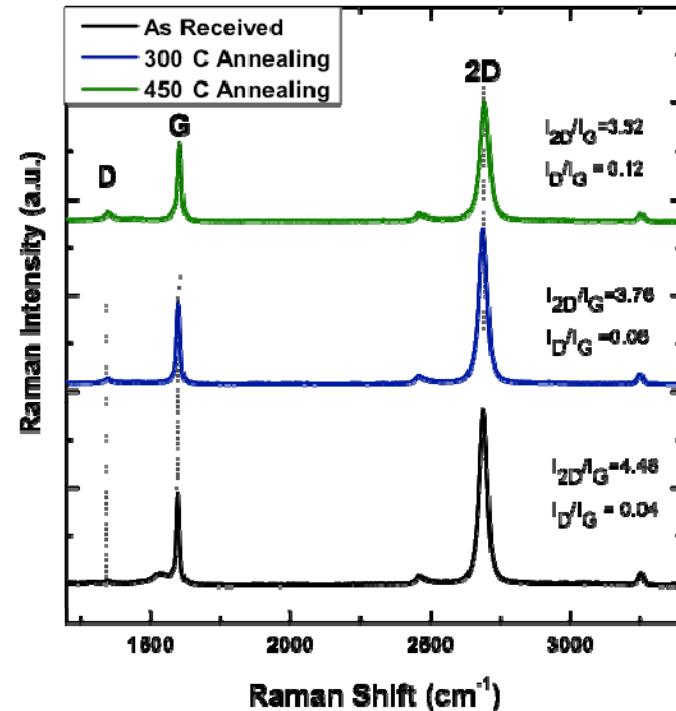
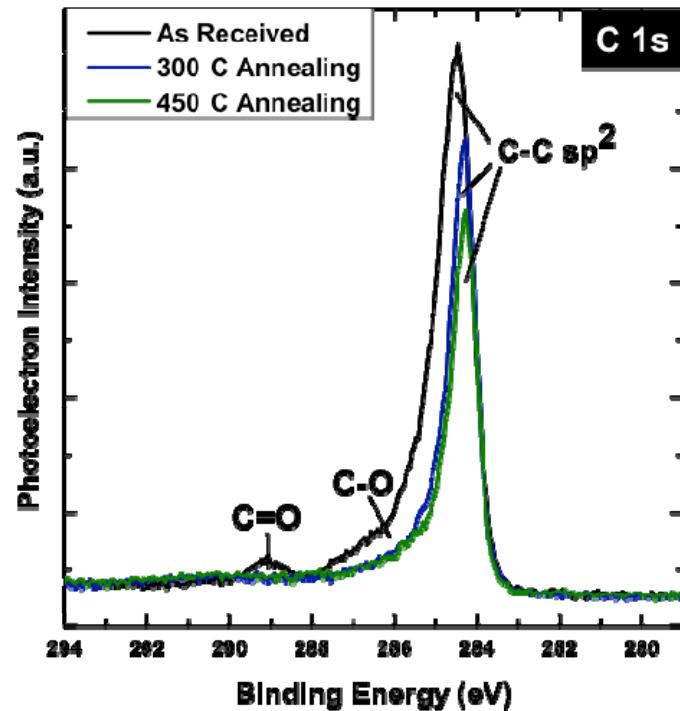


450 °C anneal



- AFM shows the reduction in surface roughness with UHV anneals
- 300 °C Atomic hydrogen shows a slight improvement over just 300 °C anneal
- 450 °C results in the smoothest surface

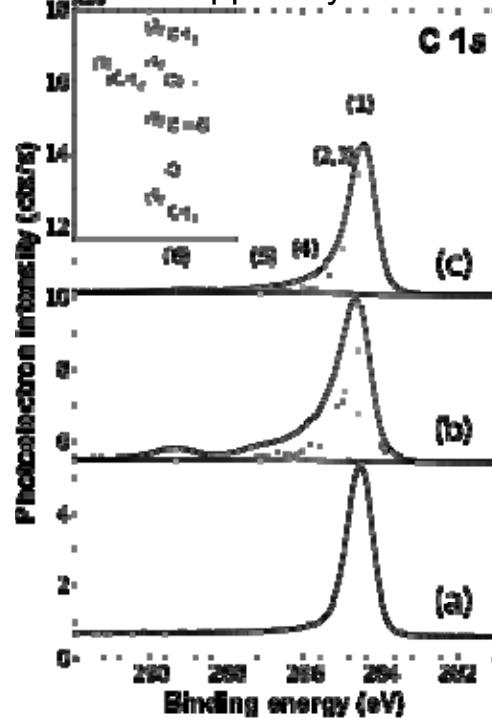
High temperature Annealing



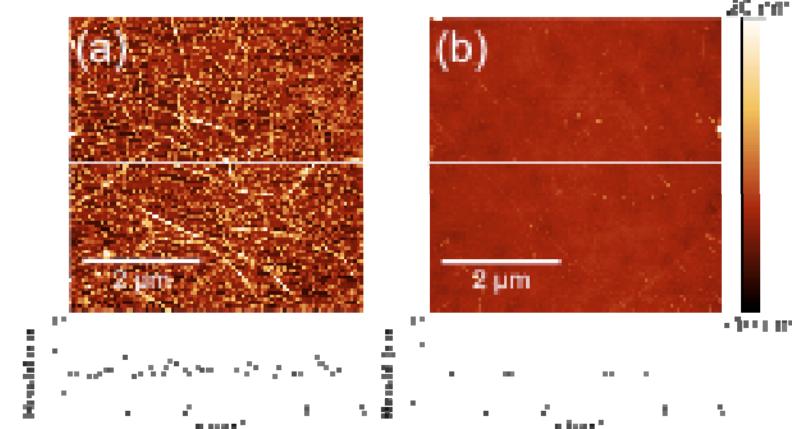
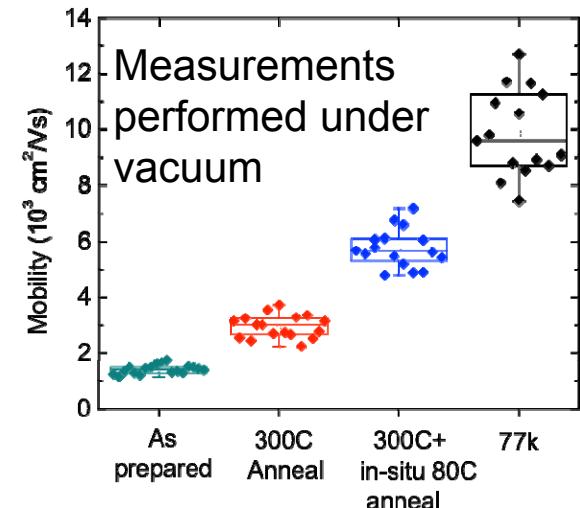
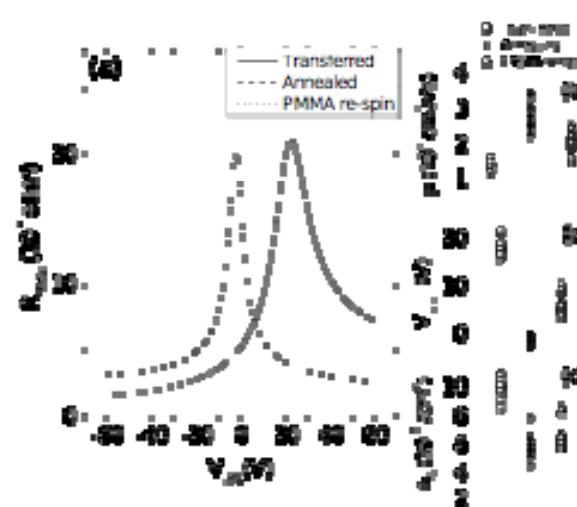
- Higher temperature anneals suggest increased PMMA residue reduction
- Increased $I_{2\text{D}}/I_{\text{G}}$ ratio is consistent with increased P-type doping due to reduced PMMA
- Increased D peak highlights that annealing may be causing damage to the graphene.
- This is consistent with recent reports suggesting that thermal decomposition of PMMA may produce radicals that could react with the graphene*

Optimizing the Transfer Process: Effect of Residues

* Pirkle, et al. Appl. Phys. Lett. 99(12) 122108 (2011)



** Chan, et al., ACS Nano 6(4) 3224 (2012)



- Transfer residues such as PMMA have been identified*
- 300°C UHV anneal results in a significant reduction*
- PMMA re-spin confirms that PMMA reduces graphene mobility*
- Mobilities as high as $12,700 \text{ cm}^2/\text{Vs}$ have been achieved on SiO_2 **

* Appl. Phys. Lett. 99(12) 122108 (2011)

** ACS Nano 6(4) 3224 (2012)

Summary: Transfer Optimization

- Four potential PMMA removal methods beyond acetone rinsing having been highlighted.
 - Extended (Hot Acetone), UHV anneals, reducing environment anneals and reactive metal sacrificial layers
- With the exception of extended and hot acetone anneals all show further reduced PMMA residue with little or no degradation of the graphene based on Raman analysis.
- UHV ambient required for effective PMMA removal
- High temperature UHV anneals can induce damage

To end

Summary: Graphene

- Ozone treatment can result in ALD nucleation without detectable damage
- Surface contamination likely responsible for high-k nucleation
- Residence time on surface important
- High-k seed layer approach has limited scalability

Conclusions

- In-situ studies enable the understanding of ...
 - Interfacial chemistry and resultant defects
 - Mechanisms of film nucleation and growth
 - The “baseline” to which ex-situ grown films/interfaces can be compared
 - Electrical device performance
- Future extensions are underway to...
 - Examine reactions at high pressures
 - Provide advance-studies prior to synchrotron work where beam time is a premium
 - Investigate processes in realistic environments

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