Starting Materials and Functional Layers for The 2005 International Technology Roadmap for Semiconductors: Challenges and Opportunities

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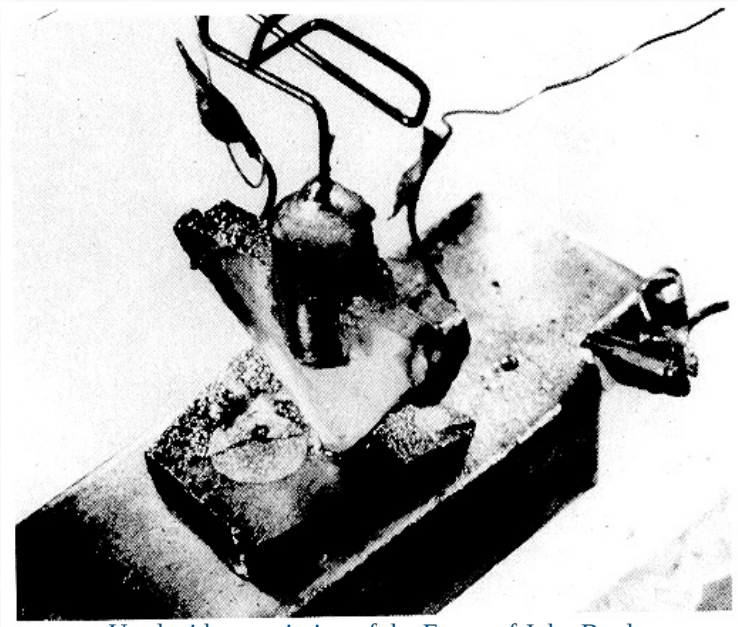
Agenda

- Introduction
- Challenges
  - Site Flatness and Nanotopography
  - Particle Size
  - Wafer Edge Exclusion / Roll-Off
  - 450 mm Diameter Wafers
- Opportunities
  - SOI
  - Strained Silicon (and Ge)
  - Hybrid Structures
- Actions

Transistors to Integrated Circuits



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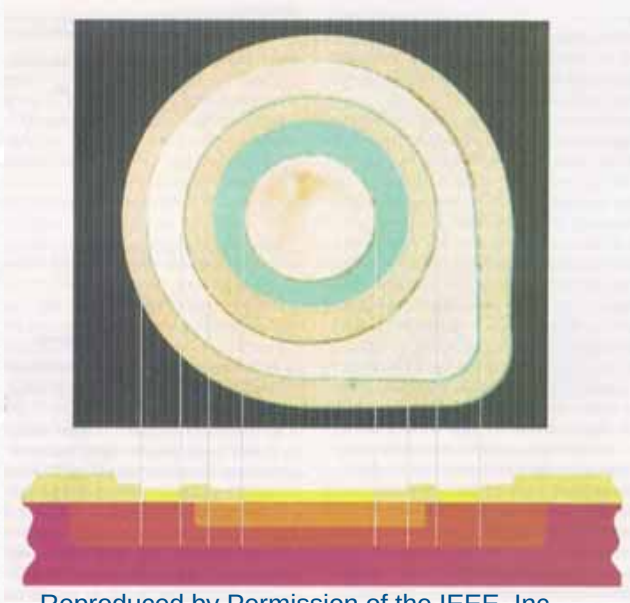

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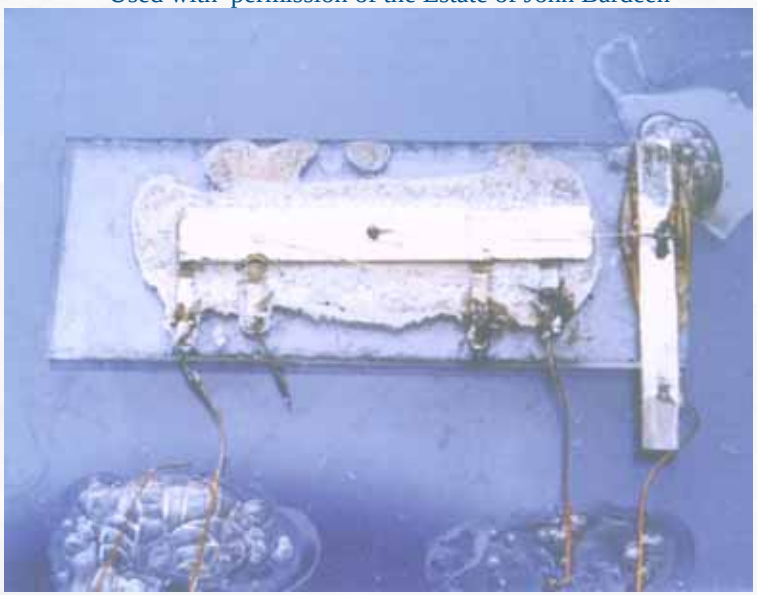
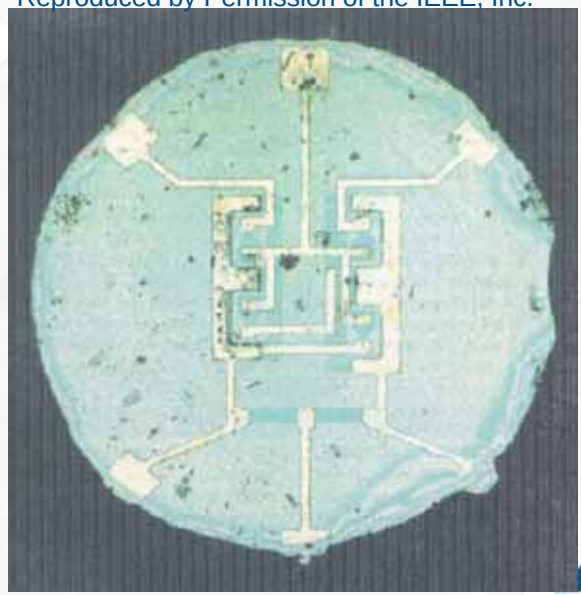


Courtesy of Texas Instruments, Inc.



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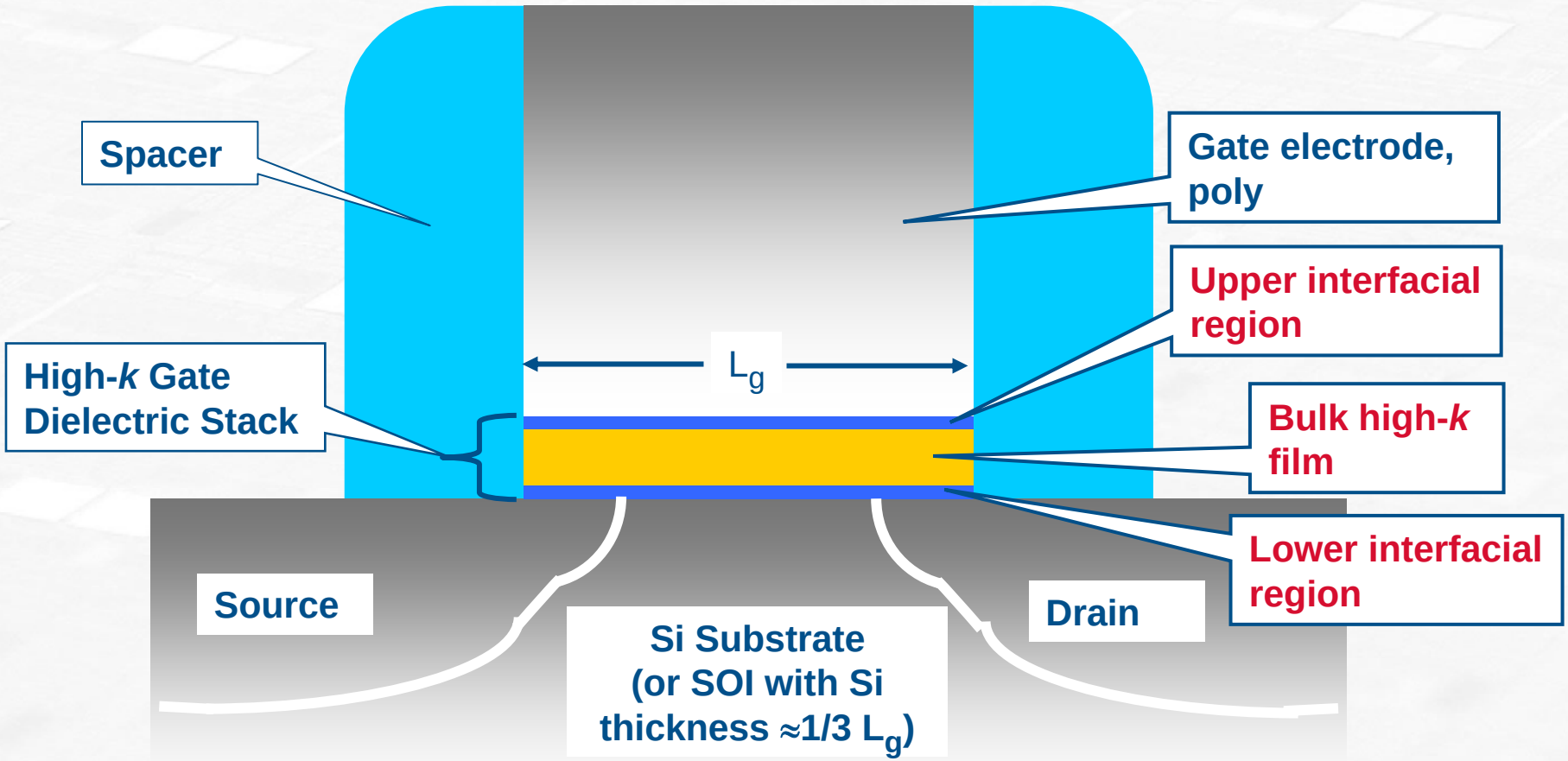
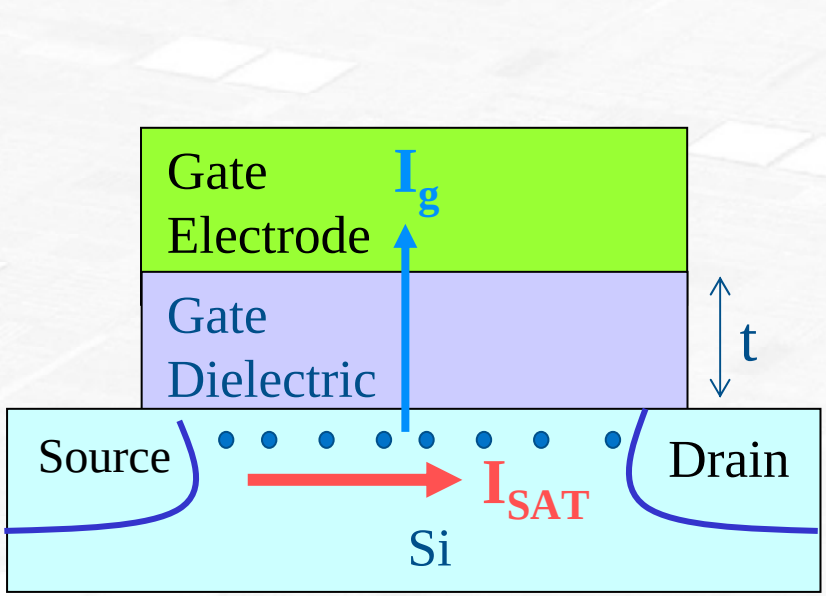
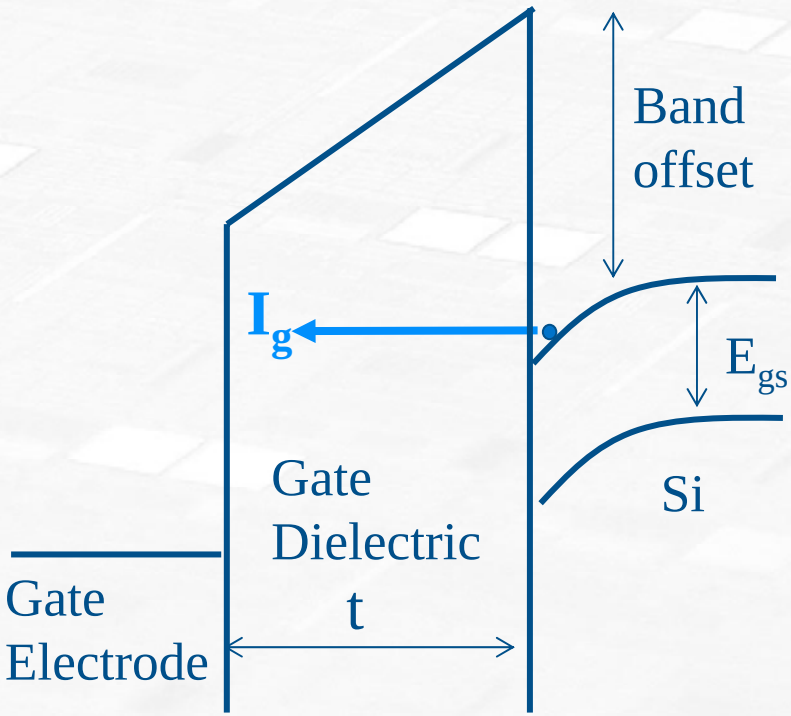
Simplified Cross-Section of MOSFET Transistor Structure



Modified From P.M. Zeitzoff, R.W. Murto and H.R. Huff, *Solid State Technology*, July 2002

Transistor Scaling





Requirement: Increase **Isat** $\propto \mu \cdot \varepsilon / t$ without increasing **Ig** $\propto \exp(-t\phi^n)$

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Site Flatness and Nanotopography

- Appears 25 mm x 25 mm site still relevant trend
  - SFSR still not standardized or widely accepted / used
- Bi-modal distribution of SFQR (survey result)
  - SFQR ≈ technology generation
  - SFQR significantly relaxed (≈ 40% larger than technology generation)
- Determination of nanotopography criticality
  - Dipole characteristic, IDMs either very interested or not interested at all

Critical Starting Materials: New Issues

- **Chuck – Wafer Flatness Interaction**
  - Nature of chuck-wafer interaction is a 3-D challenge, especially dependent on leveling mechanism of chuck and chuck design in edge region, the latter affecting ability to obtain zero defocus
  - Wide range of wafer chucks makes it virtually impossible for wafer suppliers to implement 100% chucked-wafer measurement
    - Wear of chucks in fabs exacerbates chuck flatness /chuck-wafer interaction
  - Recommend further discussion of relevant issues through SEMI
- **Emerging Materials Focus (in 2003 ITRS revision)**
  - Novel structures and processing methods to enhance silicon-based CMOS technology to achieve ITRS device metrics
  - Strained silicon and its embodiments (metrology)
    - Bulk strained Si (on uniform SiGe on compositionally graded SiGe)
    - Strained Si on uniform SiGe on Insulator (SGOI) – partially / fully depleted
    - Strained silicon on insulator (SSOI) or Ge – partially / fully depleted
  - Other areas under consideration include Ge MOSFET structures, high-resistivity silicon, isotopically pure silicon and integrated optoelectronics on silicon

Particle Size Reduction – Some User Input

- **"Folly to reduce particle size to ½ technology generation**
  - Absolute nonsense from many points of view, including necessity and metrology
  - Surface preparation should increase their size to one technology generation (or even larger)"
- **"Numerous process steps leading to pre-gate level exceptionally convoluted**
  - Incoming wafer may play only a limited role in performance
    - Beyond actual processing steps which offer ready particle sources, effect of in-line metrology cannot be discounted
  - Although same piece of silicon enters process, it clearly changes over time
  - From Starting Materials perspective, not obvious that two teams must publish equivalent trends in ITRS tables
    - Many existence proofs, based upon actual customer specifications, particles ≥ one technology generation ample to meet requirements"
- **Nevertheless, Surface Preparation claims IDMs indeed need / require particle size = ½ technology generation**

Defect Density Challenges

- **Assess viability of continued utilization of Maly equation to calculate defect density, kill ratio assumption as well as identification of appropriate kill ratio**
  - $Y = \exp [-D_P R A_{Active\ Chip}]$
- **Viability of utilizing square law relation**
  - $D_2 / D_1 = (\text{Tech. Gen.}_1 / \text{Tech. Gen.}_2)^2$
- **Should we list values of defects appropriate to variously configured SOI and other Emerging Material structural configurations?**
  - Some guidance and trends appear to be useful

Critical Starting Materials (Old Issue Re-Addressed)

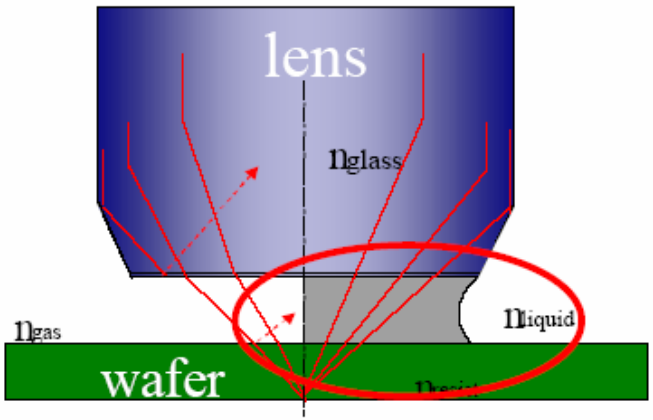
- **Surface Preparation sub-TWG has noted**
  - Starting Materials methodology of increasing particles and metals (by 2x the Maly derived value) enhances expectation that Surface Preparation can surely remove these increased levels
  - Wrong message may be sent to suppliers of cleans equipment who have to deal with in-line (pre-gate) requirements (i.e., Surface Preparation) and yet work with wafers that are “looser” in incoming metal and particle levels

Wafer Edge Exclusion

- **Edge exclusion (EE) needs to be consistent for Starting Materials, Yield Enhancement and Factory Integration(FI)**
  - **ITRS Governing Body decision:**
  - **Factory Integration decides EE - die/wafer**
  - ***Some types of SOI structures are currently incapable of achieving the 1mm EE mandated by FI***
- **ITRS denotes what perceived to be needed, even if tool is not yet available, per se**

Wafer Roll-Off – Possible Impact on NGL

Immersion Lithography Concept

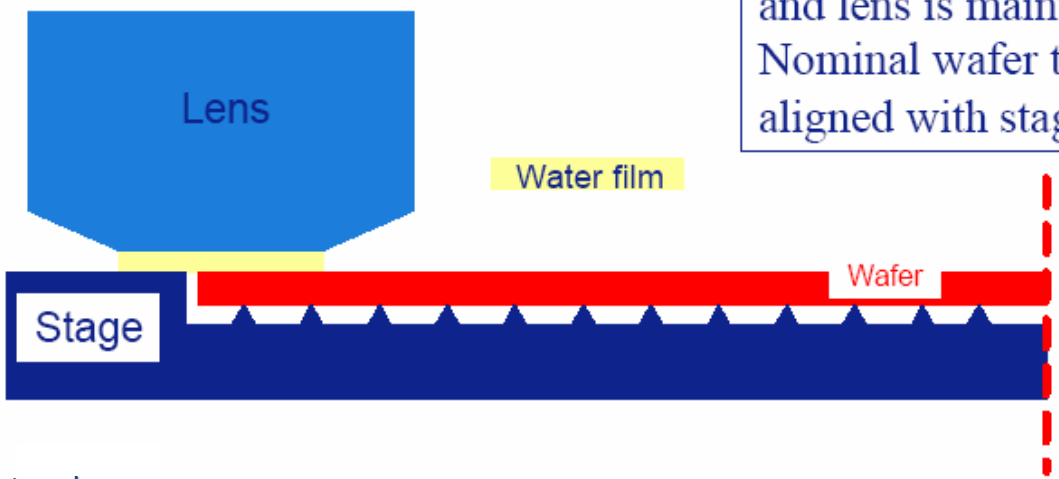


$n_{water} > n_{air}$

n bigger means

- NA bigger at constant sin(θ) → smaller CD
- sin(θ) smaller at constant NA → larger DoF

A thin water film between wafer and lens is maintained
Nominal wafer thickness is aligned with stage height



Courtesy M. Watanabe

Slide 1

ASML

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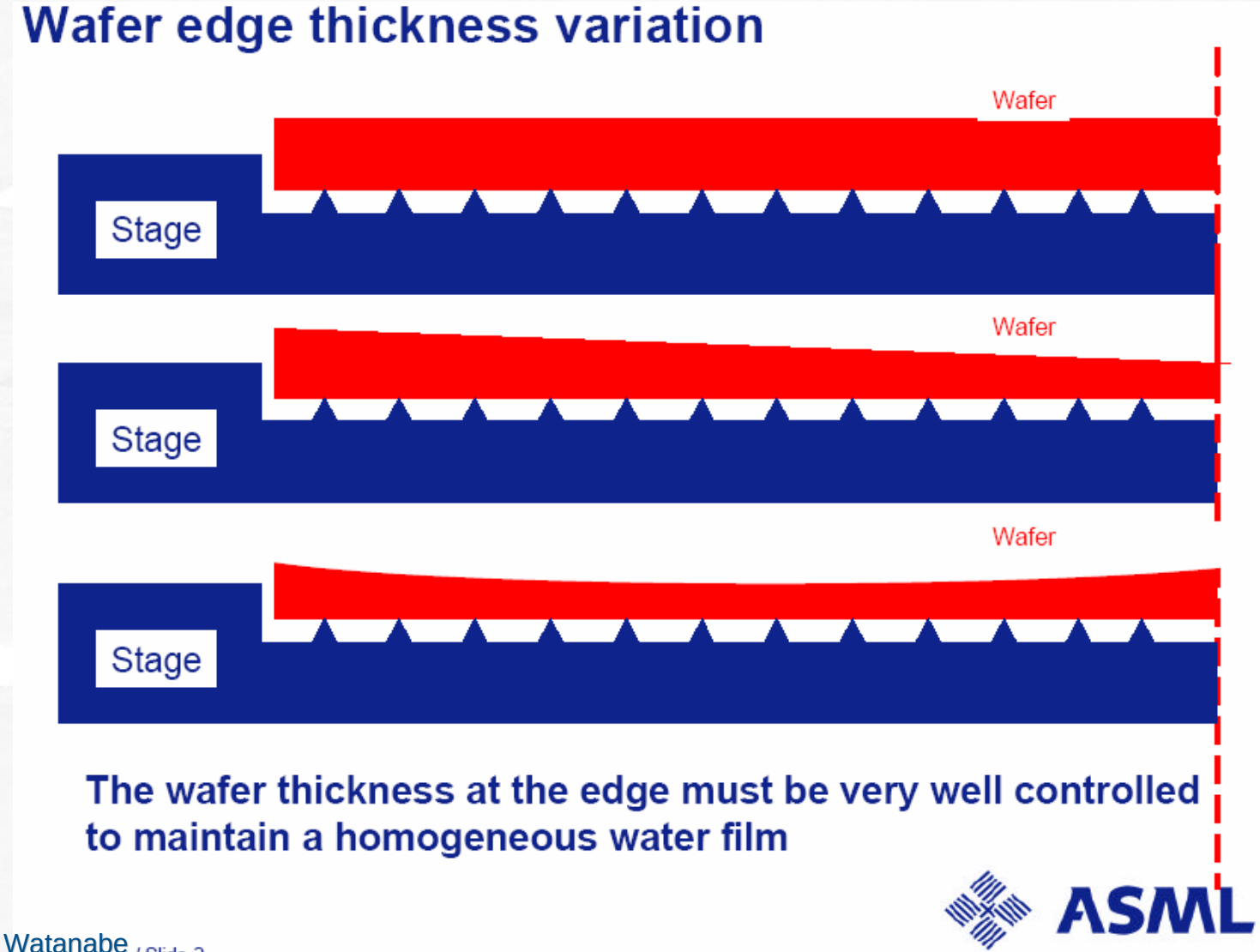
Wafer Roll-Off



Courtesy M. Watanabe / Slide 2

Wafer Roll-Off

Conclusions

- SEMI specifications for 300mm wafers:
  - Thickness, center point: 775 um +/- 20um
  - Total Thickness Variation (GBIR) max: 10um
- This yields a maximum edge height variation of +/- 30um

Question:

Can this edge height variation be reduced?

Courtesy M. Watanabe

450mm

- **Periodic wafer diameter increases key element in remaining on Moore's law**
  - **"When the wafer area increases by >2 times, but the cost of the new tool set *for the same number of wafer starts* increases by only 30-40% (which is typical), the cost per area decreases by 30-50% -- an annualized improvement of ~4% when wafer size changes occur about every 10 years."**

    R. Goodall, D. Fandel, A. Allan, P. Landler, and H. Huff,
    ***Semiconductor Silicon/2002*, ECS** PV 2002-2**, 125-143 (2002)**

D. Myers, Microelectronic Materials Strategy Symposium, SEMI, San Jose, CA, 9/24/02.

- ***However, it is also imperative to be cognizant of starting wafer cost as the expected timing of transition may intersect ITRS at a point where non-standard material types are predominant***

450mm

- **Very useful to maintain two year technology cycle**
  - **Migration to three year technology cycle may be likely**
- **Will nanotechnology-based manufacturing paradigm facilitate off-the-roadmap perspective and obviate 450mm diameter perceived need**
  - Extrapolation forward (business as usual) hoping world not change
- **Need further assessment of assumptions related to perceived wafer diameter change**
  - Nine year wafer diameter development cycle previously noted
  - Therefore, we may already be somewhat behind for 2011 450mm diameter wafer assessment at IDMs

450mm (cont.)

- **Assess potential alternatives to wafer diameter change**
- **Role / impact of emerging technologies requires consideration**
- **450mm anticipated to present severe financial crisis for silicon and equipment suppliers**
  - Changes in functionality of automated material handling system (AMHS) not fully comprehended
- **Although ITRS fundamental technology trend guide for industry, it does not directly address economic factors**
  - Consequence of strict adherence to historic trends without utmost due diligence represents clear issue to viability of IC industry

Connecting Economic & Technology Challenges

- **Industry strategy for next wafer size transition to include:**
  - Initial concepts for fab design, operations, and integration
  - Supply chain impact and key intercept points
  - Timing & cost of transition
- **ISMI View, based on Member Company feedback (July-04)**
  - Further modeling and analysis needed
  - Must leverage all TWGs addressing the issue
  - Too early for substantial resource commitments

ISMI

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450mm (cont.)

- **Is 2012 appropriate for 450mm / how funded?**
  - How and when will issue(s) and decision(s) be resolved
  - Need further discussion and more serious consideration for alternative solutions to productivity enhancement
- **Fundamental diameter issues addressed by ITRS Tables are for 300 mm but *MANY IDM's* have announced aggressive geometry production on 200mm (90 nm technology generations and potentially beyond)**
- **If SOI and 450mm both become necessary at about same time things could become very interesting**
  - May be unlikely, however, since SOI seems more poised for implementation than 450mm (and is indeed impacting available wafer substrate types in market-place)

Learnings From 300mm Experience?

- Establish earlier consensus on fab architecture & operations
  - One company driving strategy is suboptimal
  - Need to comprehend wafer size bridging in toolset
- Drive business models and architectural strategies
  - Leave supply chain pricing to the market
- Develop standards early to reduce costs
- Support multiple leading-edge operational modes
  - High-volume/low-mix, High-volume/high-mix, etc.
- Continuously evaluate and adjust, including:
  - Impact of technology on next wafer size transition timing
  - Tradeoffs and timing using modeling and simulation tools
- Industry coordination is crucial and valuable

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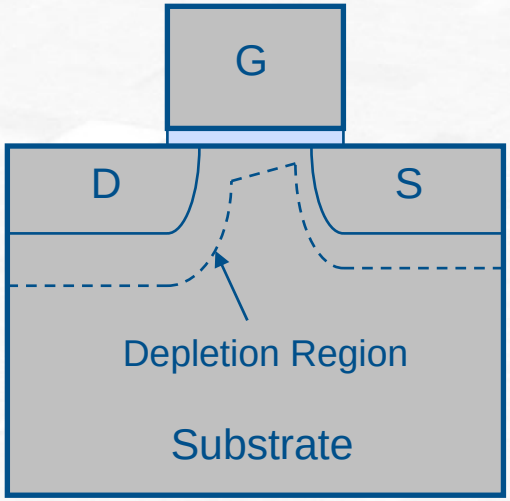
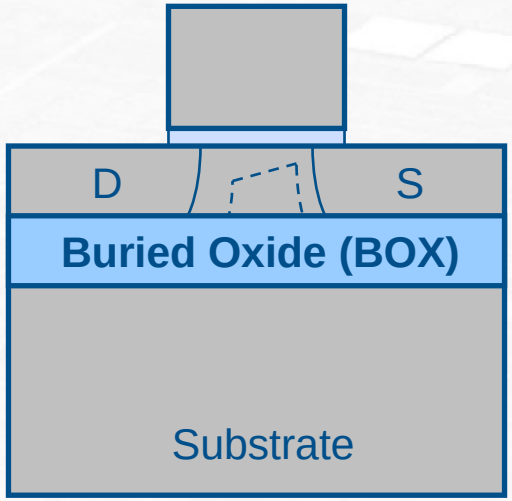
Transistor Structures

Planar Bulk



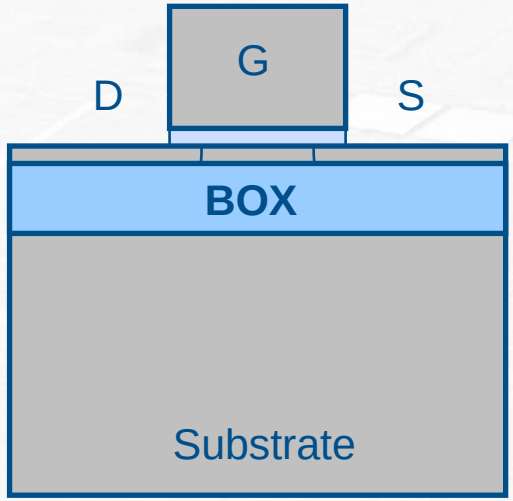
+ Wafer cost / availability
- SCE scaling difficult
- **High doping effects and statistical variation**
- **Parasitic junction capacitance**

Partially Depleted SOI



+ Lower junction cap
+ F.B. performance boost
- **F.B. history effect**
- SCE scaling difficult
- **Wafer cost/availability**

Fully Depleted SOI

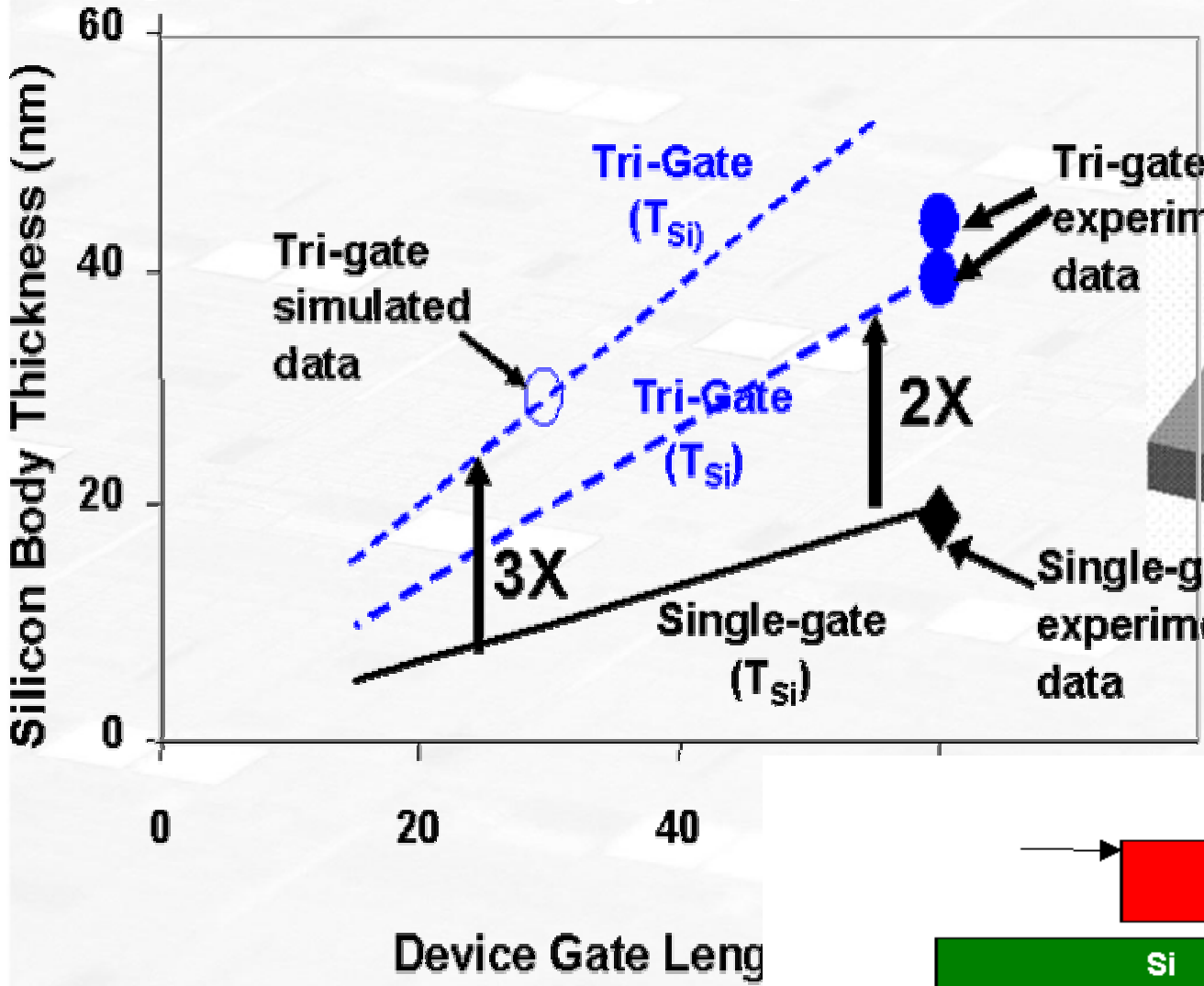


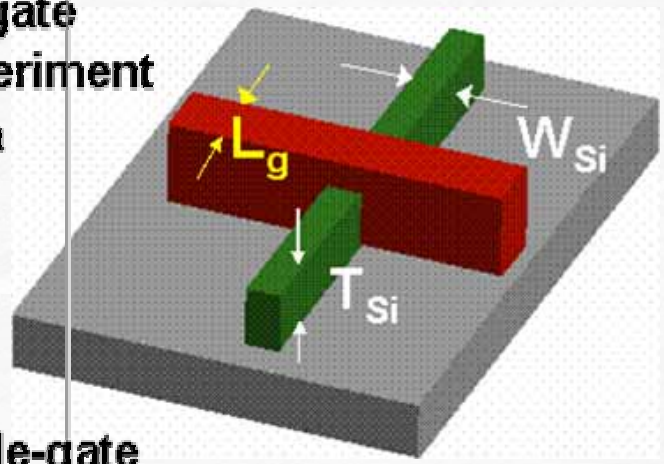
+ Lower junction cap
- SCE scaling difficult
- **High $R_{series,s/d} \Rightarrow$ raised S/D**
- **Sensitivity to Si thickness (very thin)**
- **Wafer cost/availability**

References:

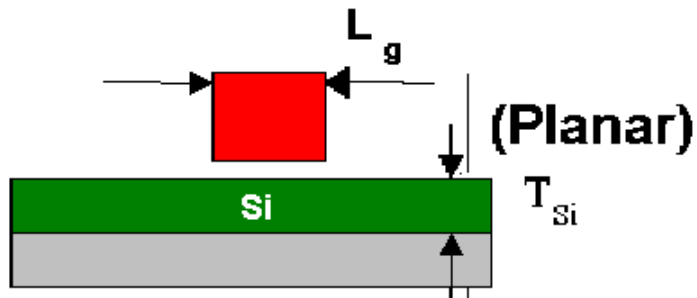
1. P. Zeitzoff, J. Hutchby and H. Huff, Internat. Jour. High Speed Electronics & Systems
2. Mark Bohr, ECS Meeting PV **2001-2**, Spring, 2001

Tri-gate Relaxes T_{Si} Requirement of Single-gate





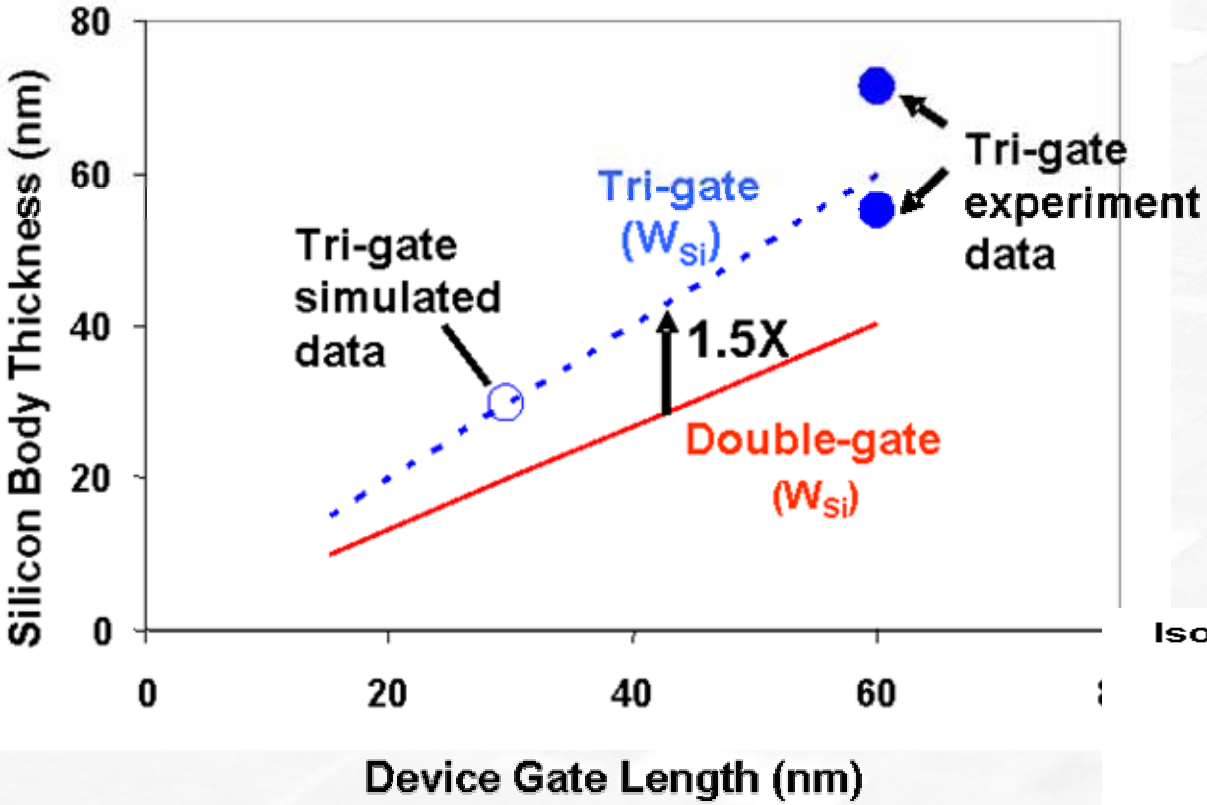
Tri-gate DST

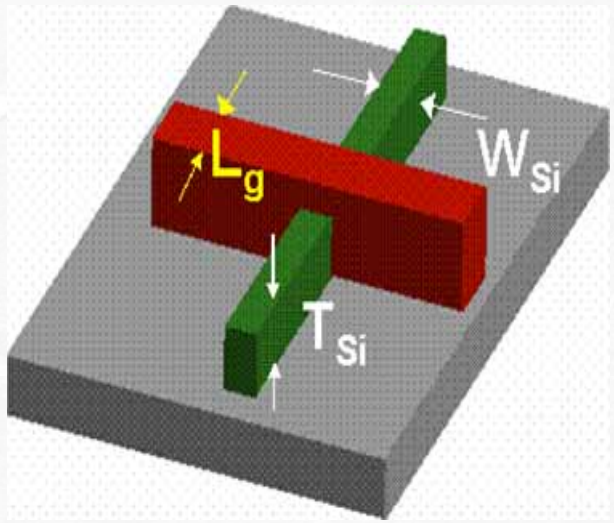


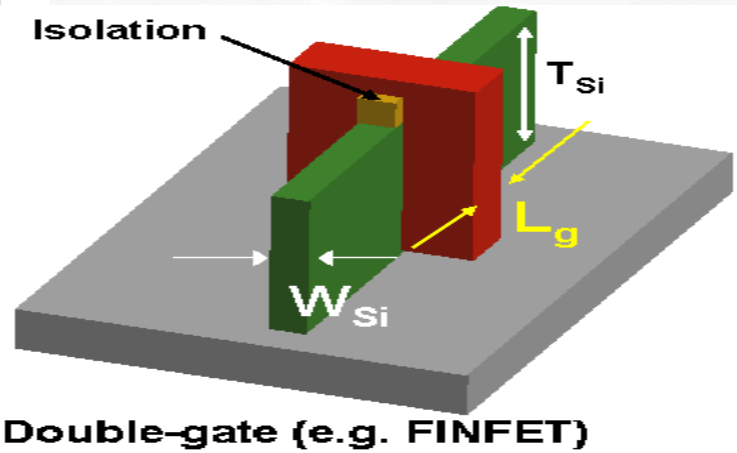
Single-gate DST = standard Fully-depleted SOI

Courtesy of Robert Chau et al., ISSDM, 2002

Tri-gate Relaxes W_{Si} Requirement of Double-gate



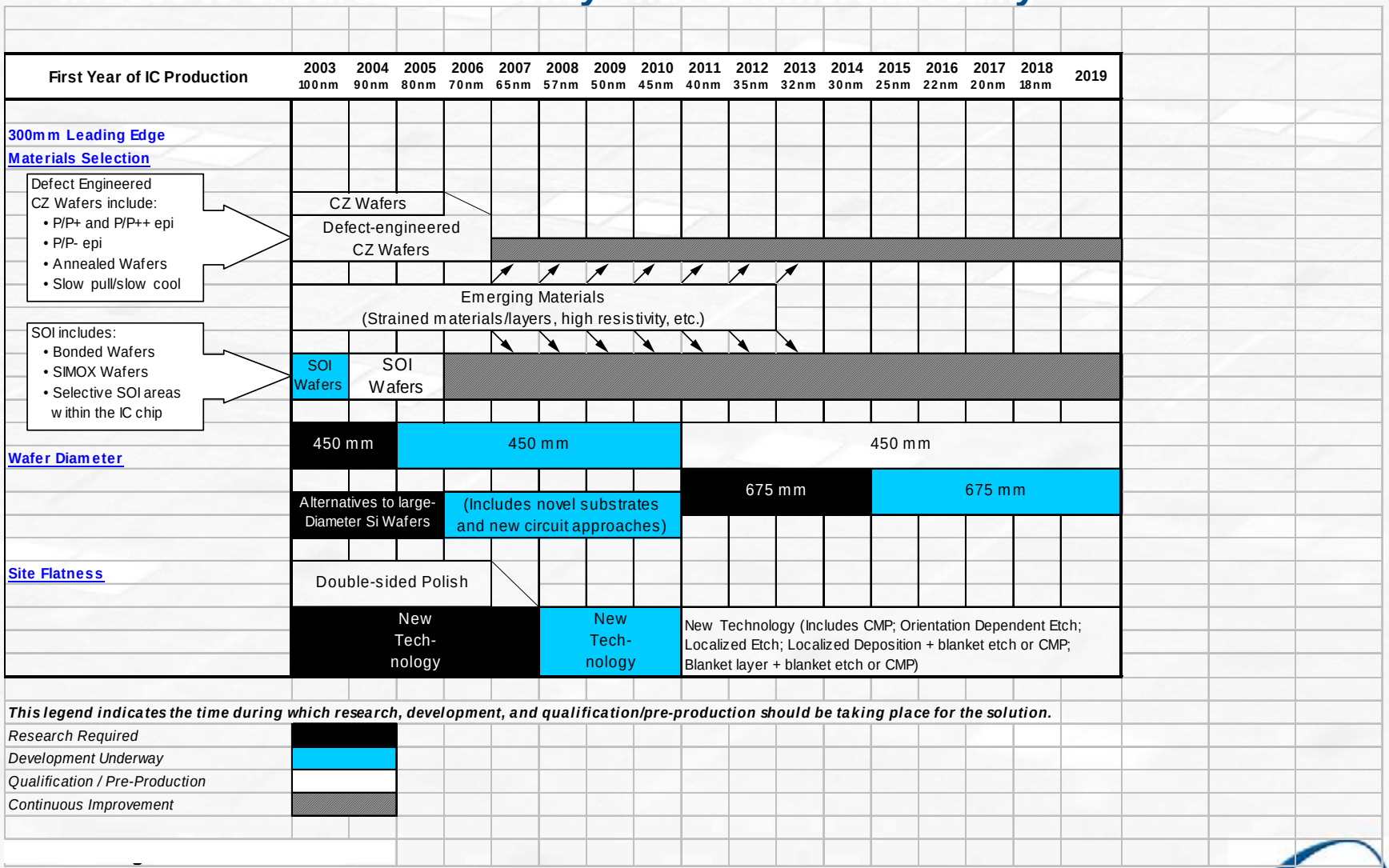




Courtesy of Robert Chau et al., ISSDM, 2002

Potential Solutions: 2004 Update

Changed SOI to clear colorization in 2004 and cross-hatched shading in 2006 to ensure consistency with commercial reality



SOI

- SOI implementation will at some point become necessary to solve leakage issues that are limiting further reductions in feature size
- There will be a point at which it will not be possible to maintain shrink progression that enables Moore's Law, without SOI
- Becomes a "timing" issue because there is question as to exactly when that point will come—as a matter of physics, economics, and technological readiness

SOI

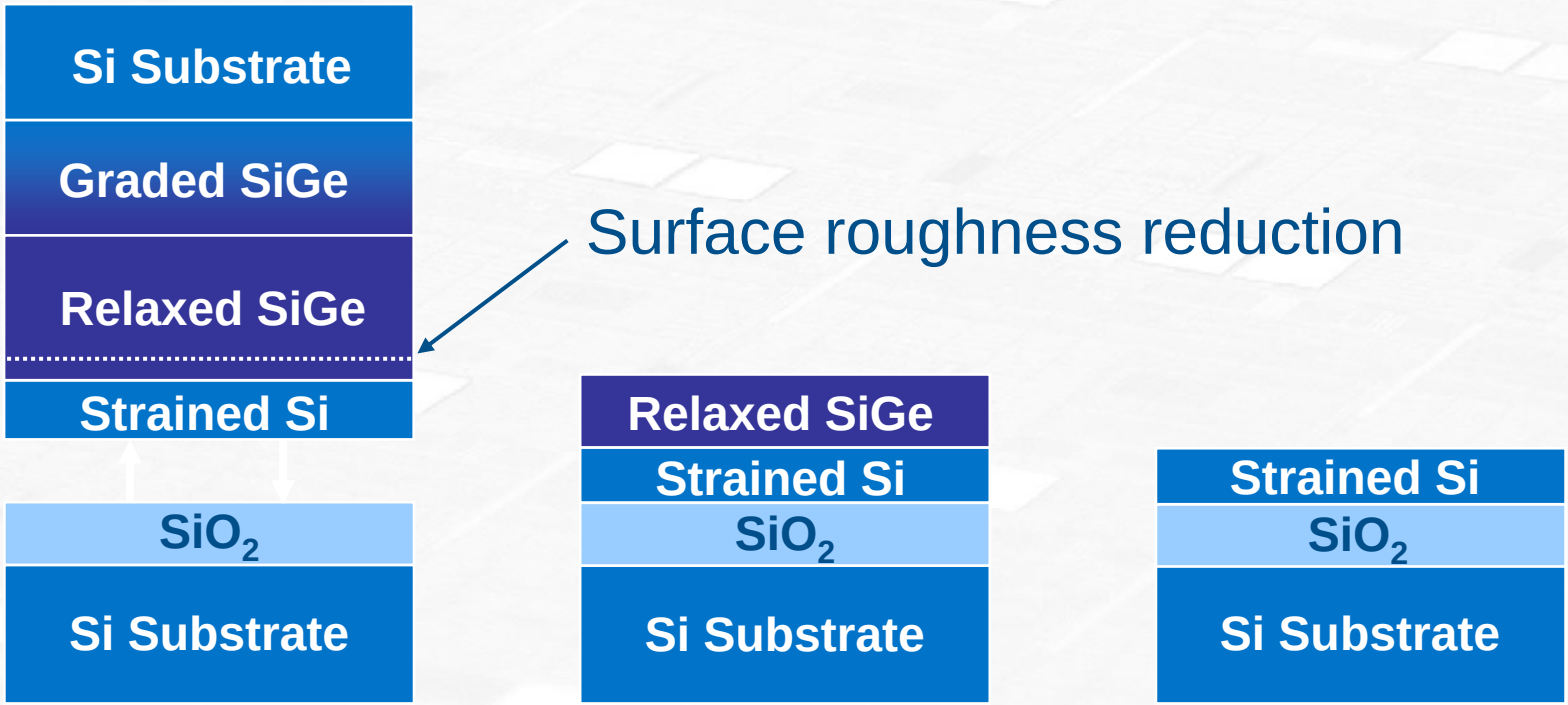
- Economic issues are price of SOI wafers and timing that each IC company uses for SOI implementation
  - Ideally should be implemented somewhat before becomes physically impossible to otherwise progress, because there [is] a learning curve involved in maximizing its yield
- Technological readiness issues have to do with capabilities of SOI wafers, for example metrology limitations / film thickness uniformity concerns
- Resolution of some issues depend on device structures (i.e., FinFET) required when SOI becomes imperative
- Therefore, very important for industry to have an accurate forecast of which technology node will absolutely require SOI, from a physics standpoint

Methods of Forming Strained Si / SGOI

- **Bonding and Layer Transfer**
- **Thermal Mixing of SiGe with SOI**
- **Integrated SIMOX-SGOI**

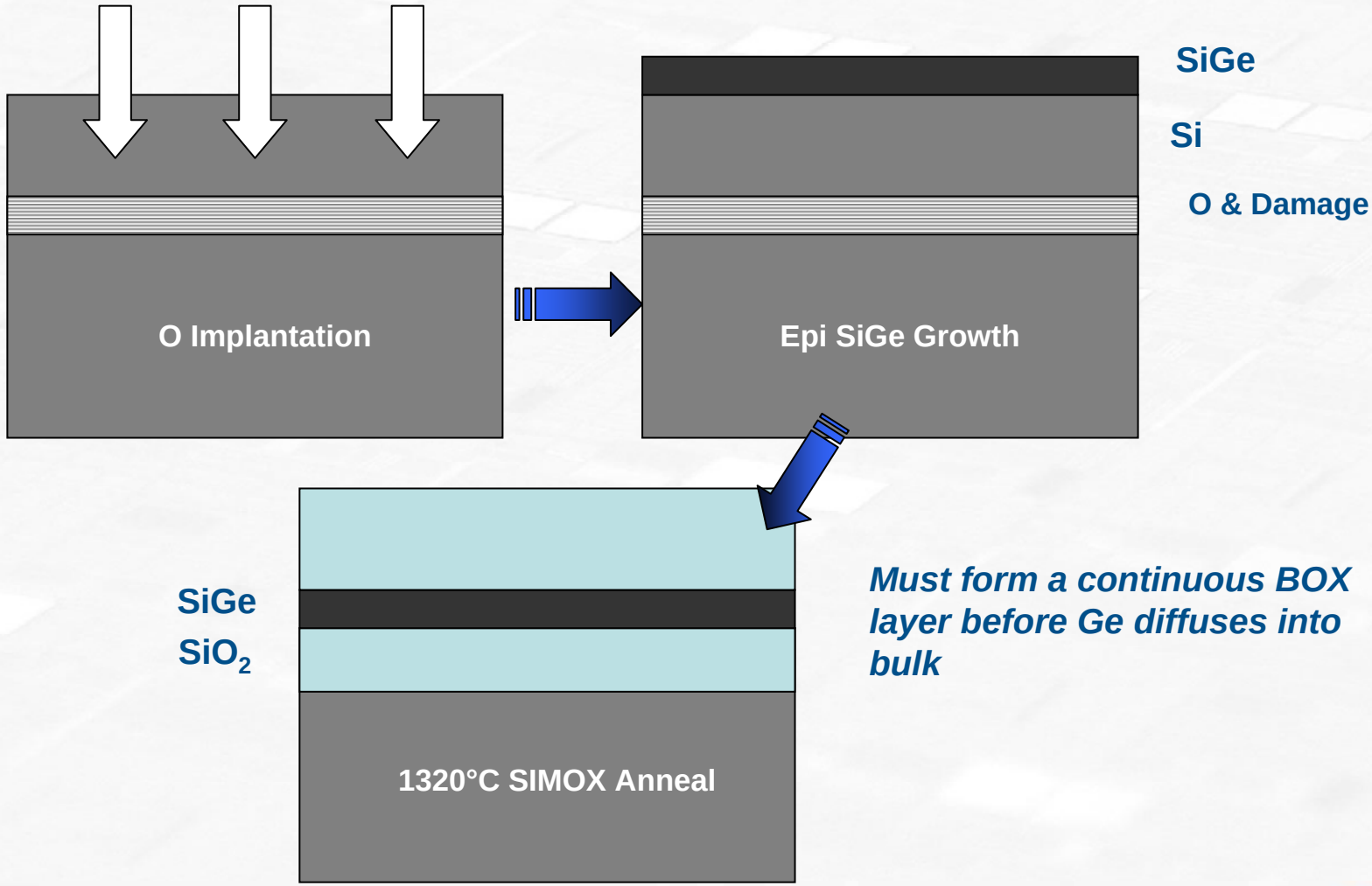
Sadana / Current, SOI Technology Symposium,
Oct. 18, 2004

SSOI Substrate Fabrication Process



Starting material quality critical to process

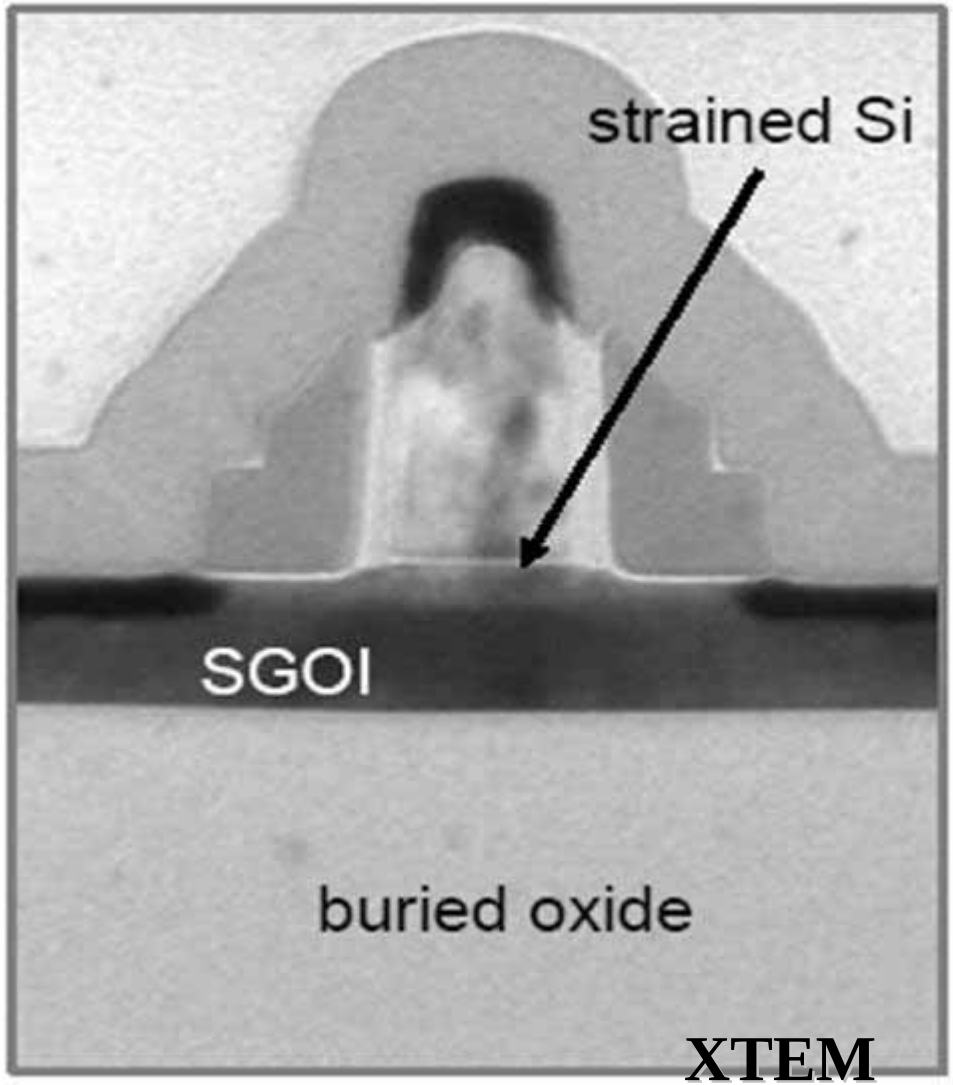
Integrated SIMOX and SGOI Process



Must form a continuous BOX layer before Ge diffuses into bulk

Sadana / Current, SOI Technology Symposium, Oct. 18, 2004

300 mm SGOI/Strain-Si FET



Sadana / Current, SOI Technology Symposium, Oct. 18, 2004

Strained Silicon Motivation: Mobility

$$\mu = |e|\ \tau / m^*$$

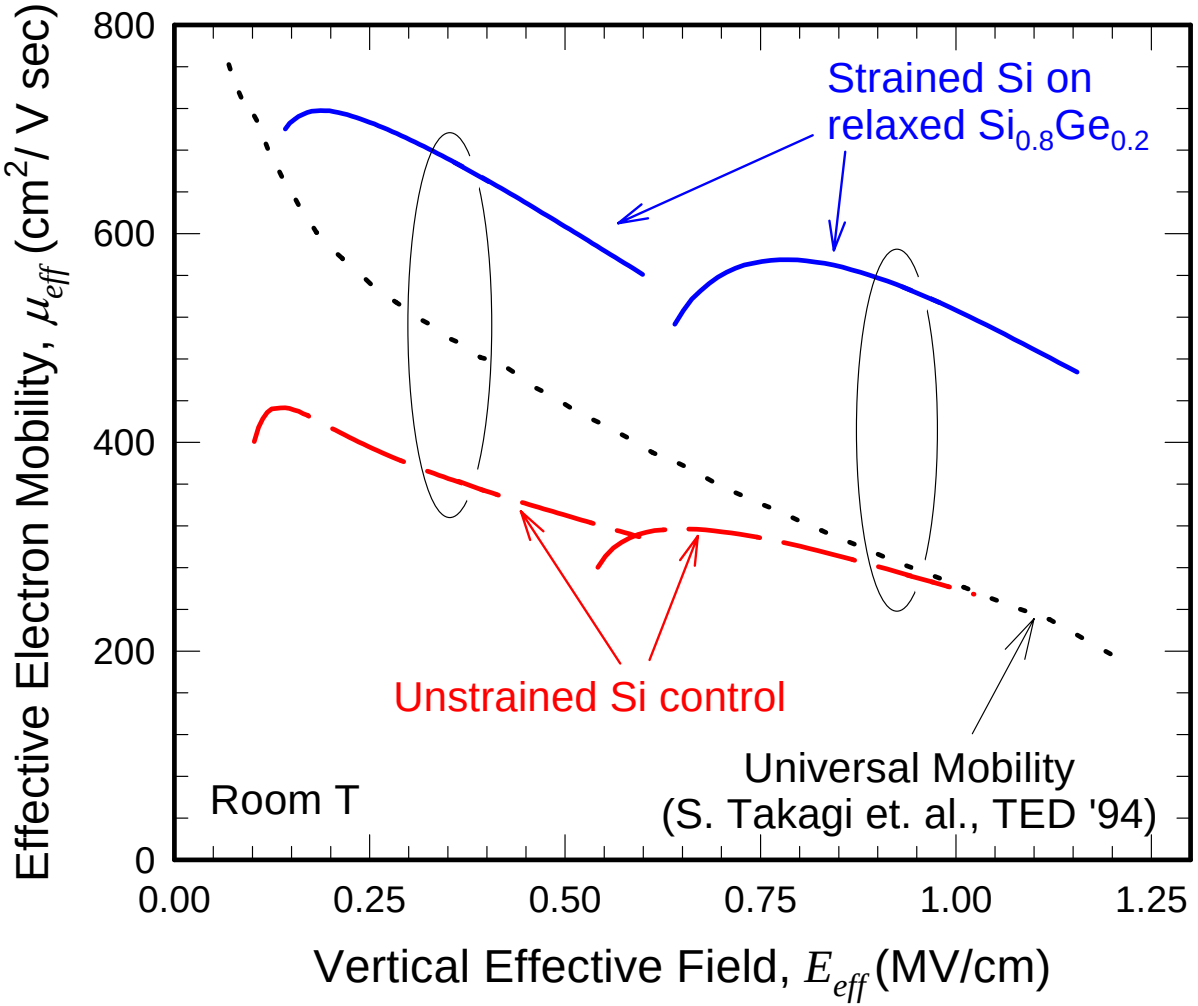
$|e|$ = absolute value of electronic charge

- τ = scattering rate
- m^* = effective mass

$$\mu = \delta v / \varepsilon$$

δv = incremental speed gained per applied electric field ε

Electron Mobility Enhancement in Strained Si MOSFETs (Rim.et al.. IEDM 1998)



- Electron mobility enhancement of ~ 1.8X persists up to high E_{eff} (~ 1MV/cm)
- Strained-Si allows "moving off" universal mobility curve

Strain Effect on Carrier Mobility

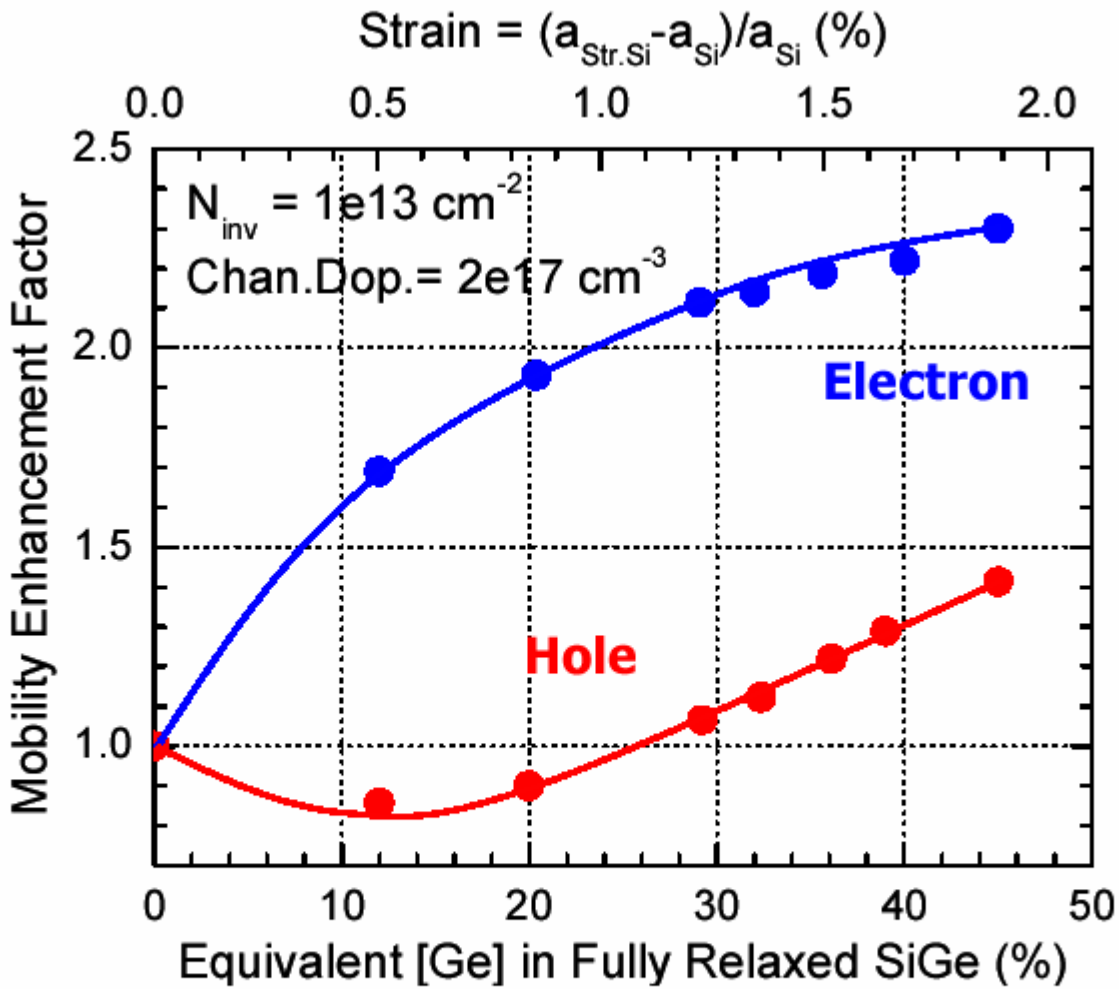
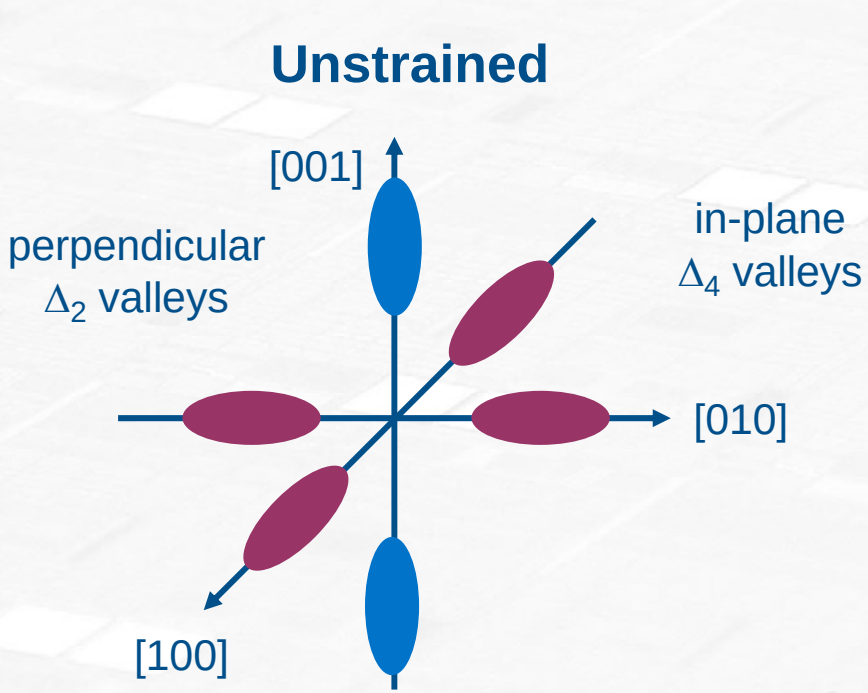
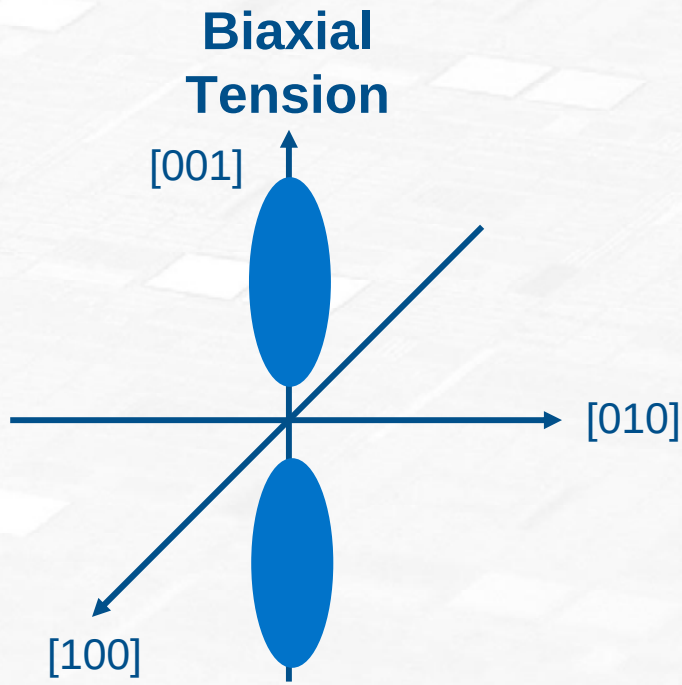


Fig. 4. Mobility enhancement vs. strain and [Ge] in strained Si/relaxed SiGe MOSFETs at 1e13 cm^{-2} carrier concentration. Hole mobility enhancement requires large amount of strain.

IBM, Rim et al, IEDM, Tech Dig, p. 49 (2003)

Electron Transport in εMOS™



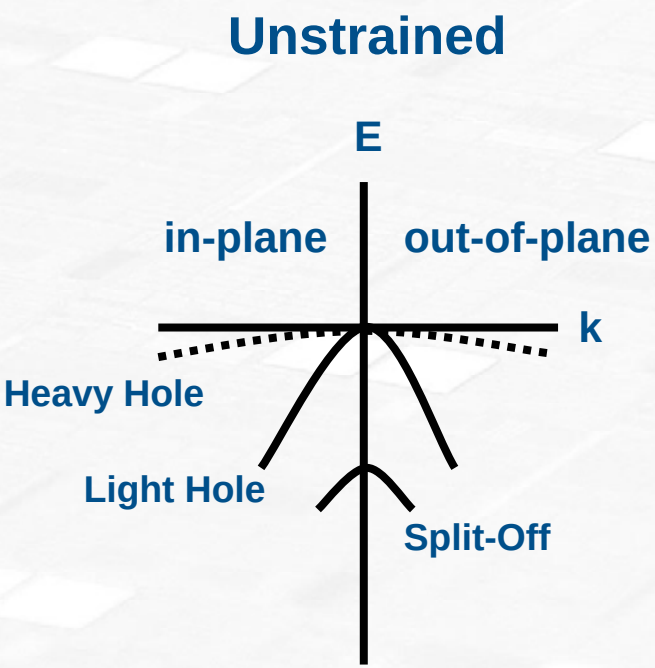


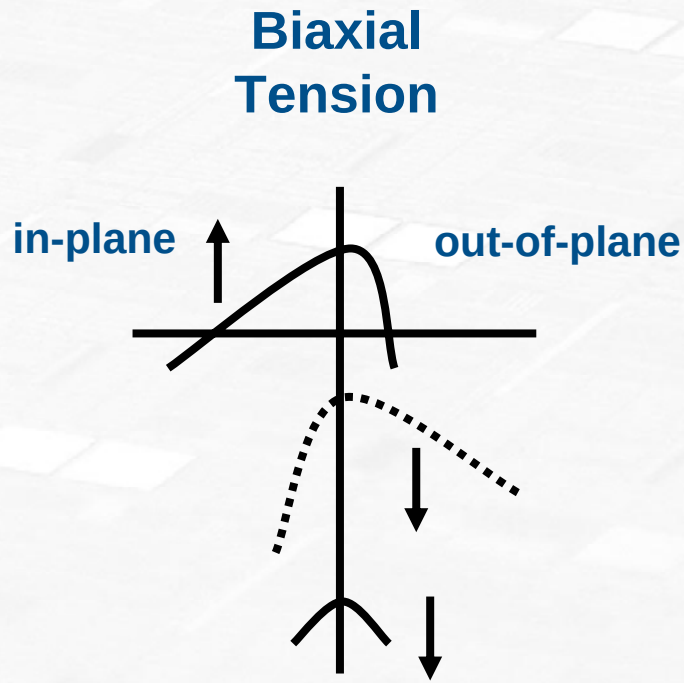
Tensile strain splits conduction band degeneracy

- **Reduced intervalley scattering**
- **Light in-plane effective mass**

Courtesy of Matt Currie
AmberWave Systems Corp.

Hole Transport in εMOS™





Tensile strain splits valence band degeneracy

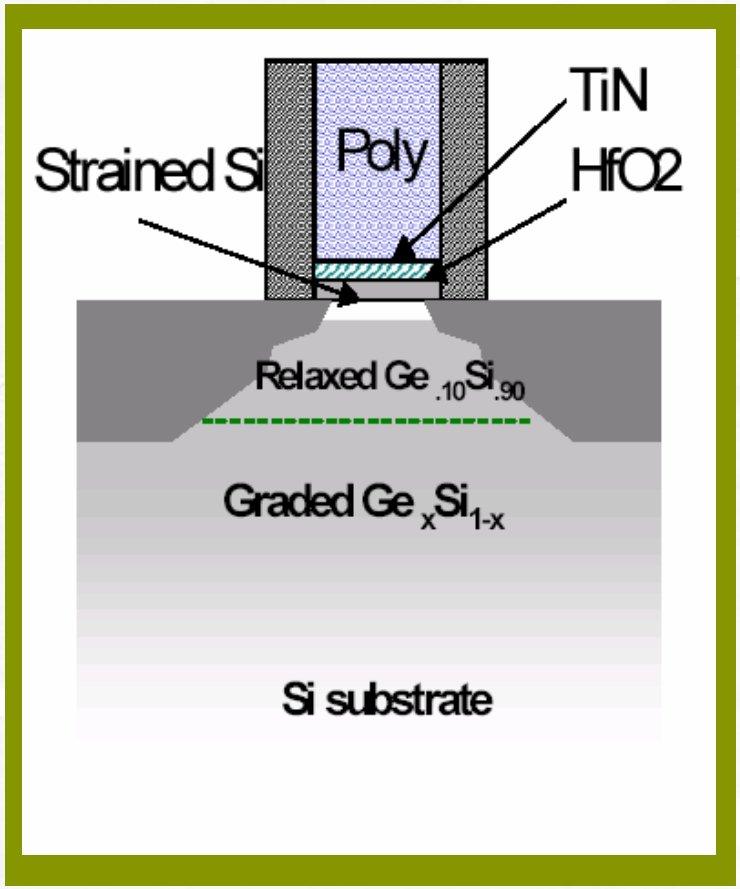
- **Reduced intervalley scattering**
- **Light in-plane effective mass**

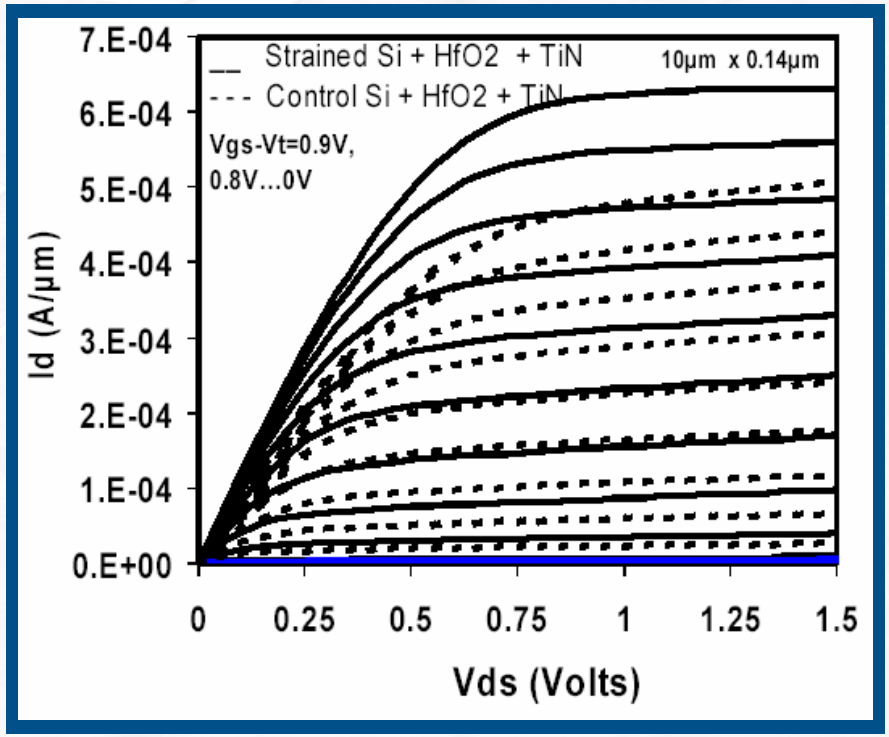
Courtesy of Matt Currie
AmberWave Systems Corp.

Key Strained Si Performance Results

- **Many manufacturers have reported performance enhancements with strained Si**
  - IBM, AMD, UMC, TSMC, Texas Instruments, Toshiba, Intel
- **Strained silicon provides higher speed, lower power transistors than bulk silicon**
  - Compatibility with 45 nm - 130 nm DRs (depending on structure and device)
  - Integrated with high K and metal gate
  - Benefits for RF application
  - 20% $I_{d,sat}$ enhancement demonstrated for L_g = 25nm
  - > 30% ring oscillator performance enhancement reported

Integration with High K and Metal Gate



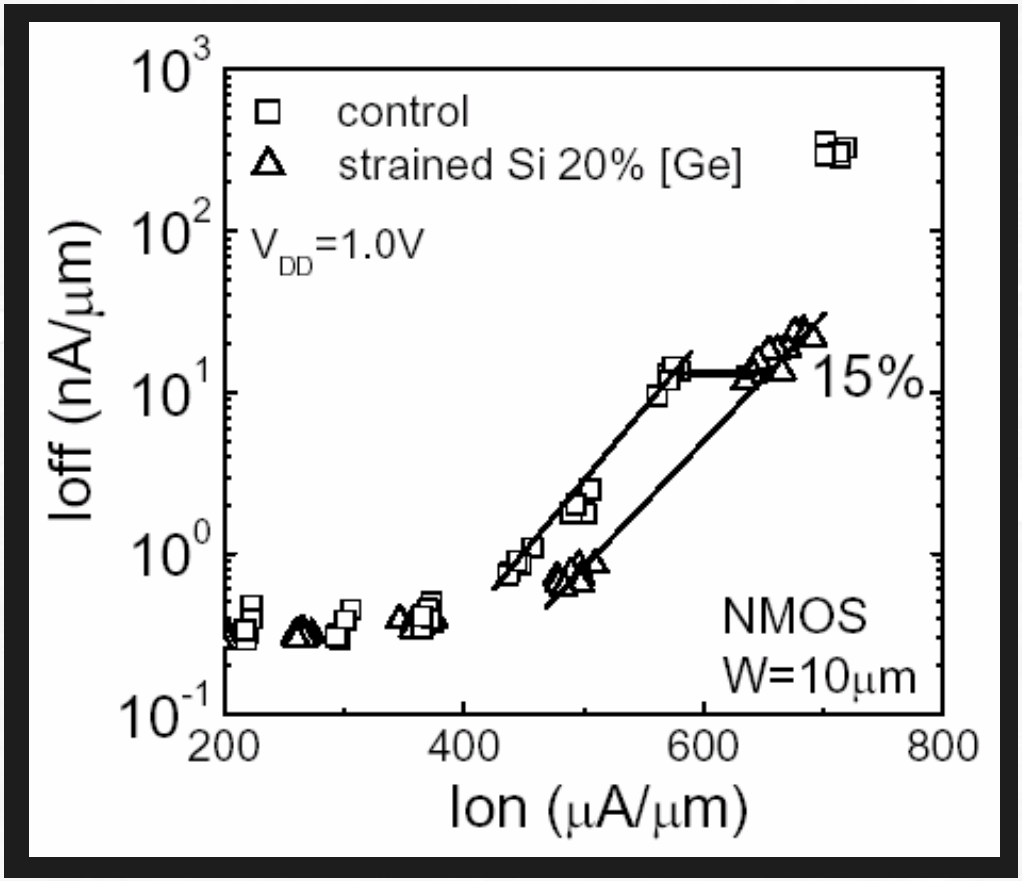


24% DC $I_{d,sat}$ enhancement

with good matching of V_t and subthreshold

INTEL, Datta, *et al*, IEDM, Tech. Dig., p. 653 (2003)

NMOS I_{on}-I_{off} Benefit



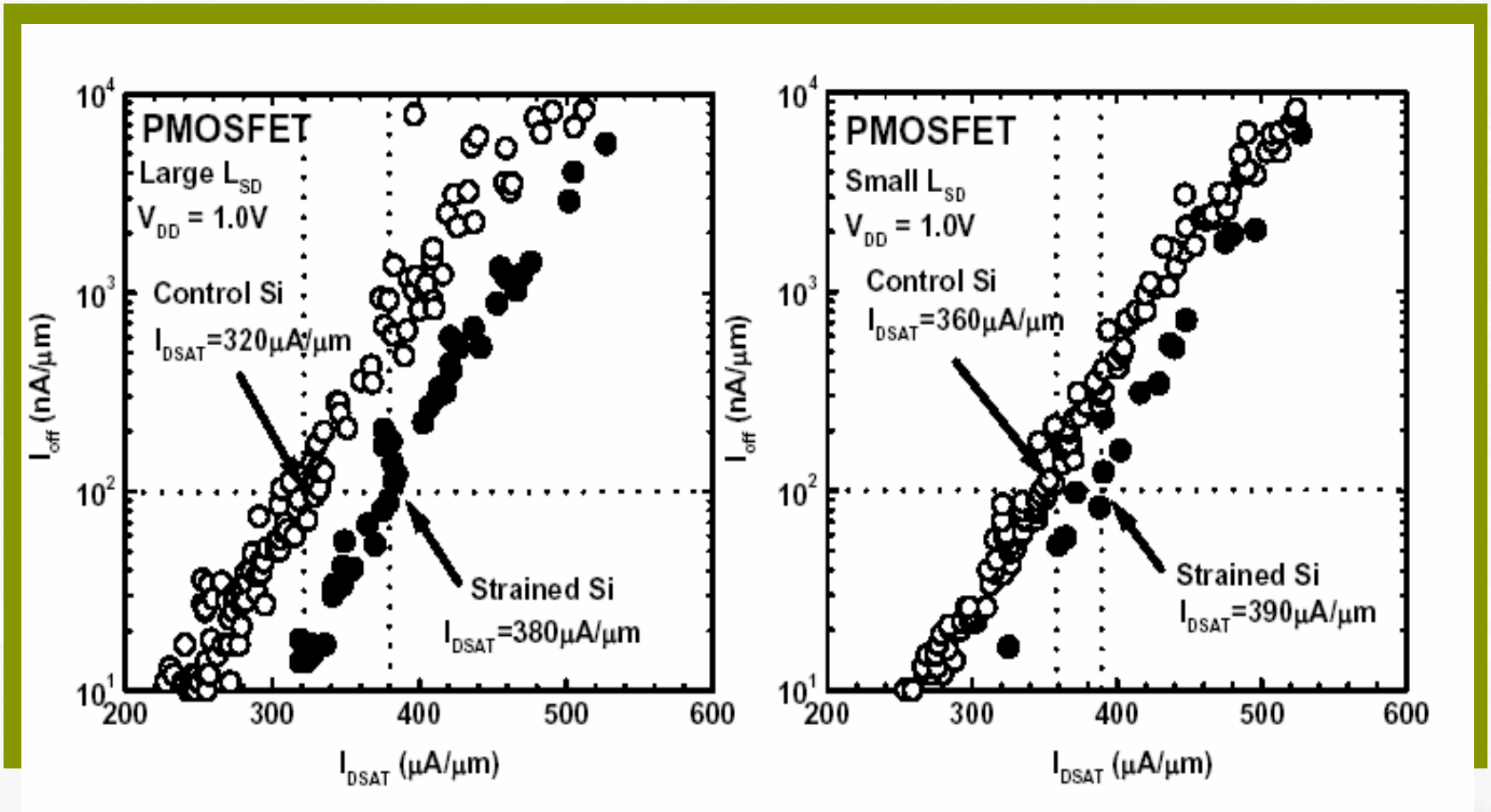
L_{gate} down to 60nm
1.7 nm EOT

15% DC enhancement
largest ever reported

Correction for self heating adds approximately **10% more enhancement**

TSMC, Wang et al, IEDM, Tech. Dig., p. 61 (2003)

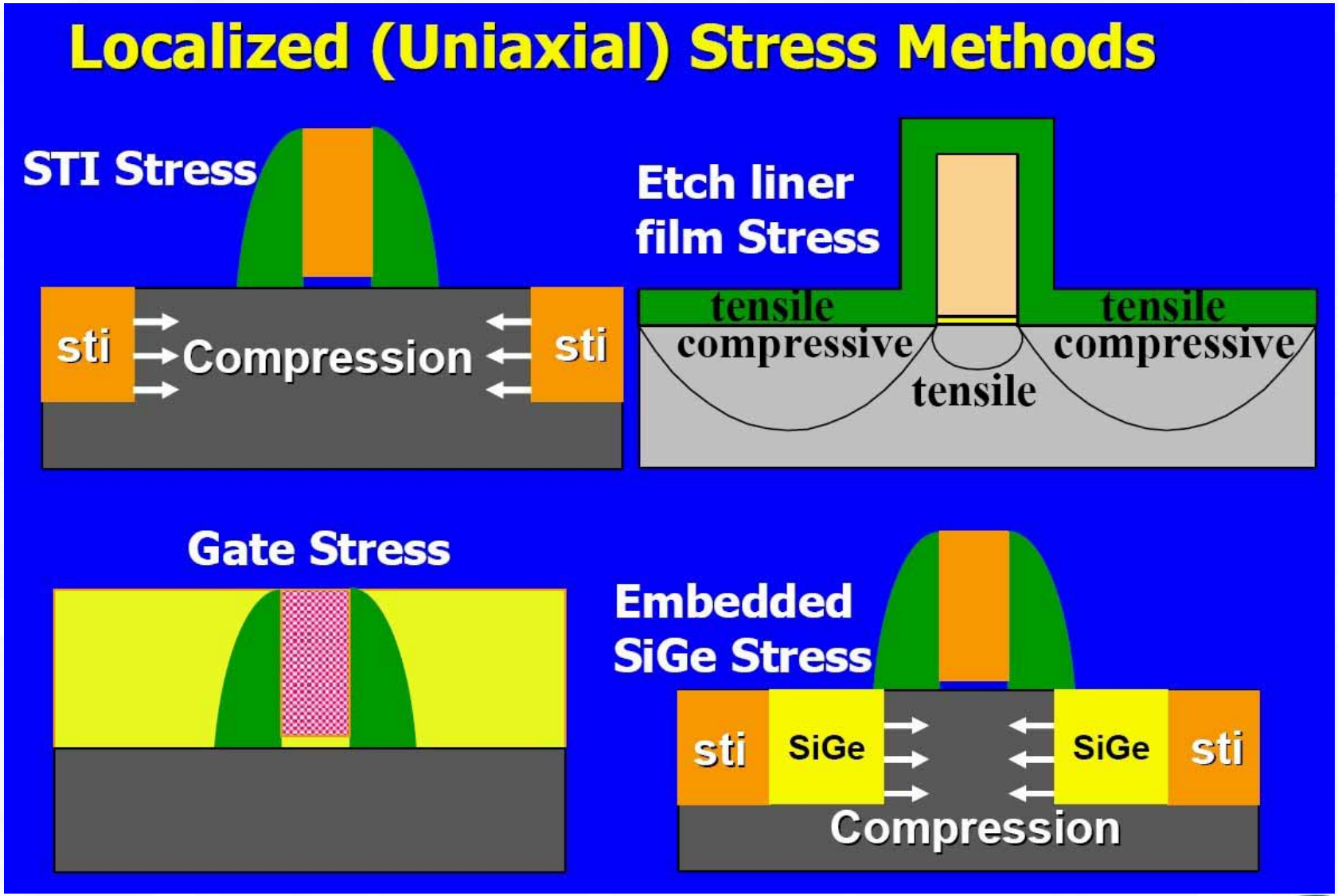
PMOS I_{on}-I_{off} Benefit



11-19% enhancement due to strained Si

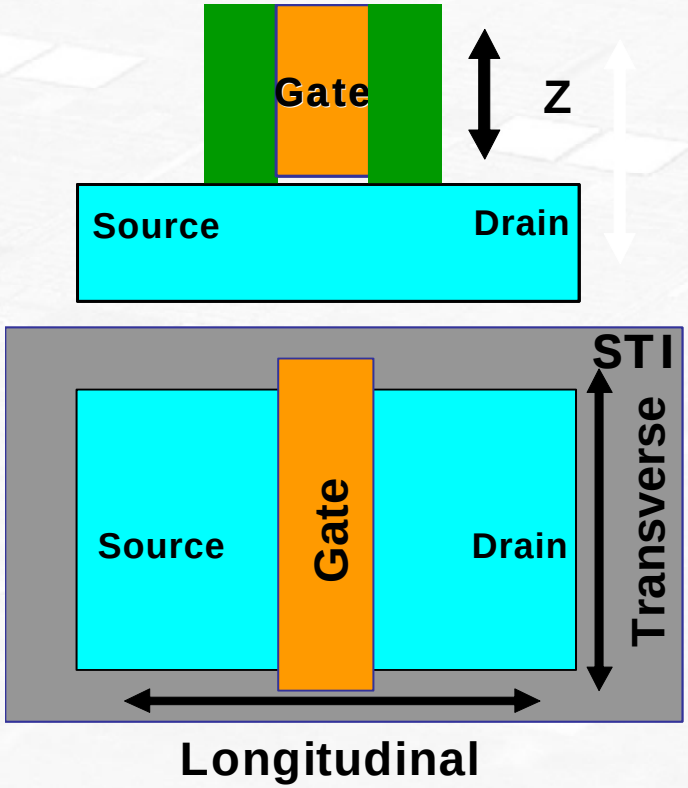
Toshiba, Sanuki et al, IEDM, Tech. Dig., p. 65 (2003)

Localized (Uniaxial) Stress Methods



Reproduced with the permission of M. Ieong et al., (IBM)

Tensile / Compressive Stress Relations



Desired Stress:

	Tran.	Long.	Z
pFET	T	C	T
nFET	T	T	C

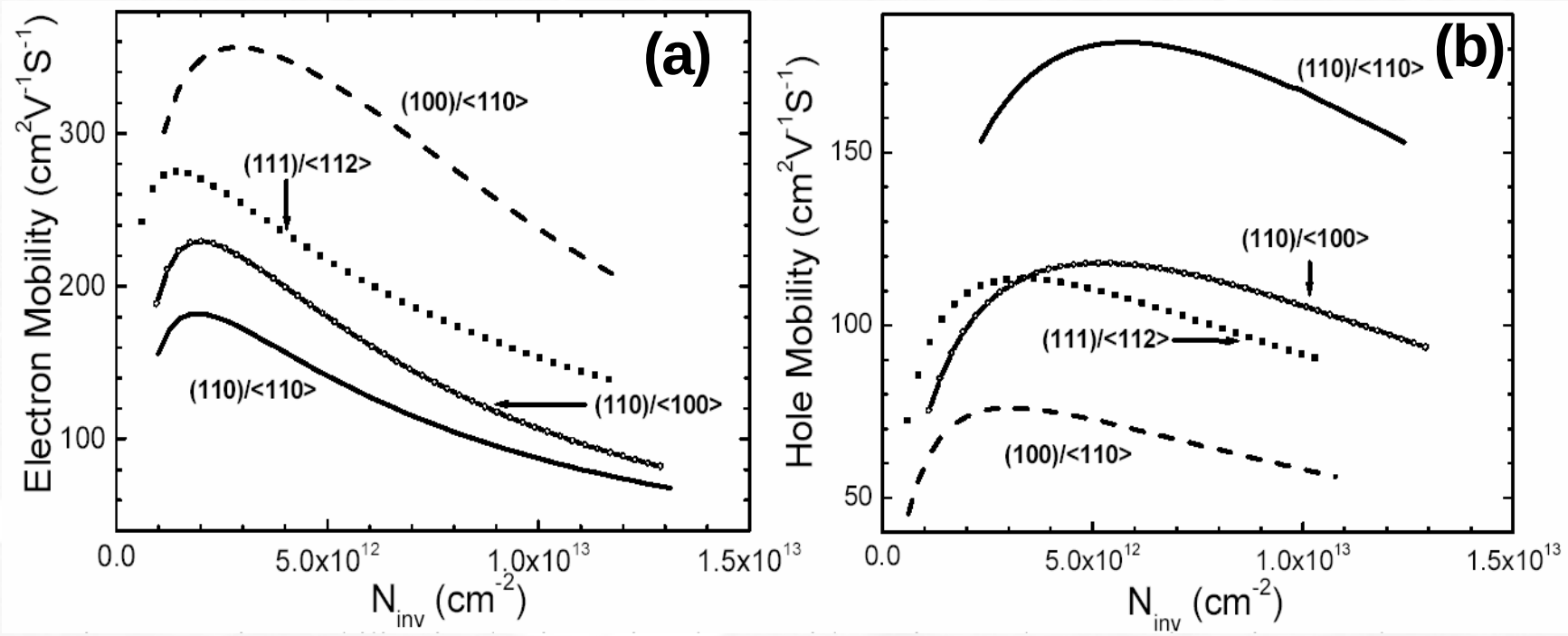
T: Tensile stress
C: Compressive stress

Dependence of device performance on the types and directions of uni-axial stresses. Reproduced with the permission of M. Ieong et al., (IBM) and The Electrochemical Society, Inc.

Agenda

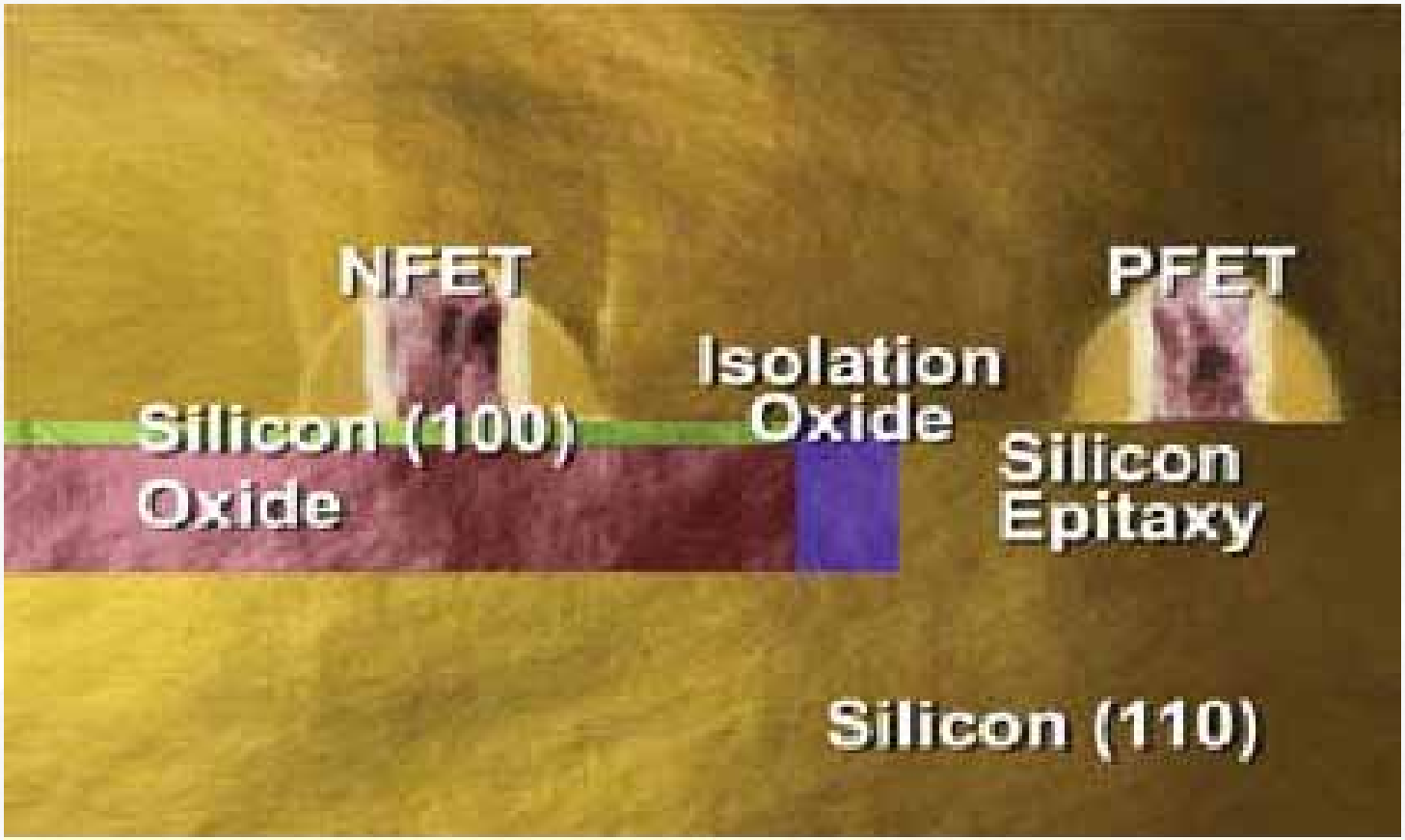
- Introduction
- Challenges
  - Site Flatness and Nanotopography
  - Particle Size
  - Wafer Edge Exclusion / Roll-Off
  - 450 mm Diameter Wafers
- Opportunities
  - SOI
  - Strained Silicon (and Ge)
  - Hybrid Structures
- Actions

Orientation Effect on Effective Electron and Hole Mobility



Orientation effect on the (a) effective electron mobility, (b) effective hole mobility as a function of inversion carrier density. Electron mobility is the highest on the (100) surface while the hole mobility on the (110) surface is more than 2.5 times higher than that on the (100) surface. Reproduced with the permission of M. Ieong et al., (IBM) and The Electrochemical Society, Inc.

Hybrid OrientationTechnology



Hybrid Orientation Technology (HOT). PFET on (110) surface and nFET on (100) surface. Planar structure, fully compatible with standard CMOS processes. Reproduced with permission of Min Yang et al., (IBM) and the IEEE (© 2003 IEEE).

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Actions

- Assess updated survey responses from IDMs for 2005 ITRS
  - 1:1 dialogue with silicon suppliers to ensure integrity of silicon and SOI suppliers cell colorization and manufacturing capability
- Significant loss of silicon mtl's expertise in IDMs due to evolving industrial focus on IC scaling
- Silicon suppliers expected to fill required research
- Silicon suppliers are resource and extremely financial limited
- 'Silicon still substrate for building these [non-classical CMOS] devices'* although many components inside CMOS-like transistors will be very different, including many manufacturing processes

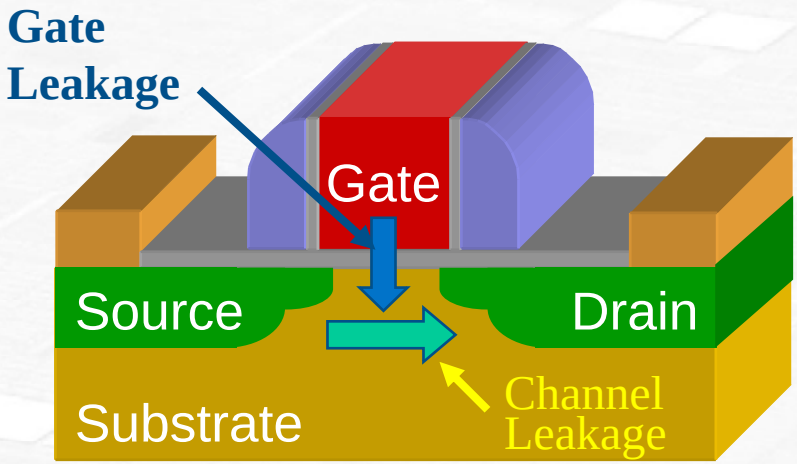
* Ken David (Intel)

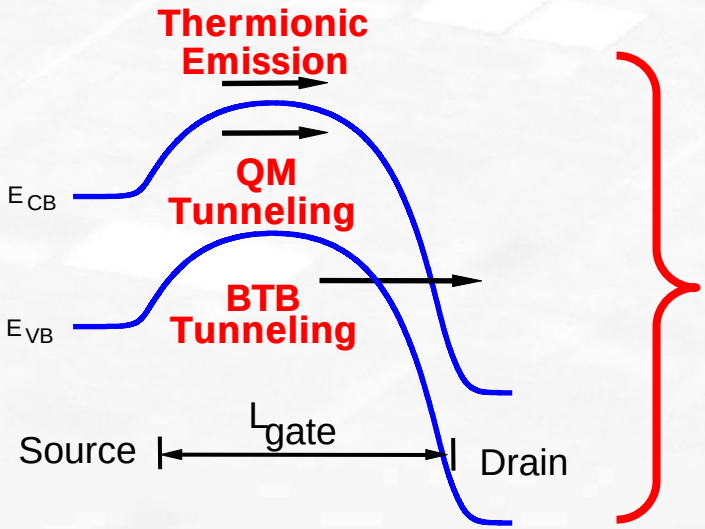
Acknowledgements

- Surface Preparation, Thermal / Thin Films, PIDS, Yield Enhancement and Factory Integration ITRS TWGs
- ISMI personnel at SEMATECH

Supplemental Material

Electrostatic Scaling of Classical CMOS Channel Leakage (I_{off})



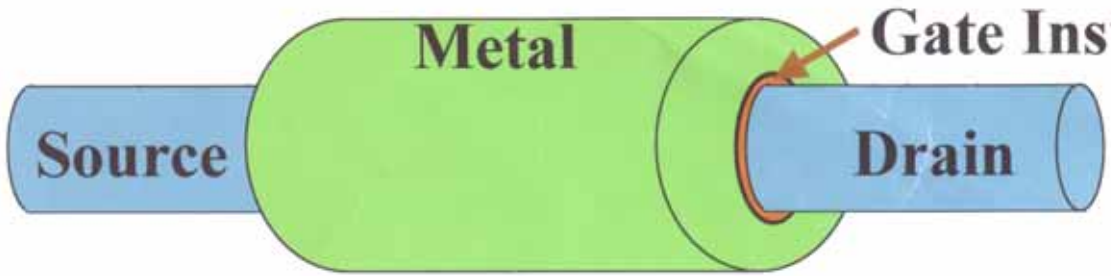


Sum = I_{off}

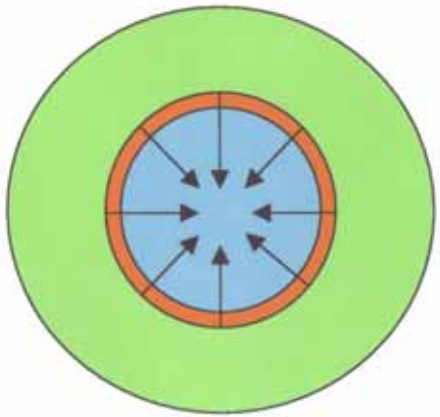
Channel Leakage

Jim Hutchby

The Ideal MOS Transistor



Fully Surrounding Metal Electrode



Fully Enclosed, Depleted Semiconductor

High-K Gate Insulator

Low Resistance Source/Drain

Band Engineered Semiconductor

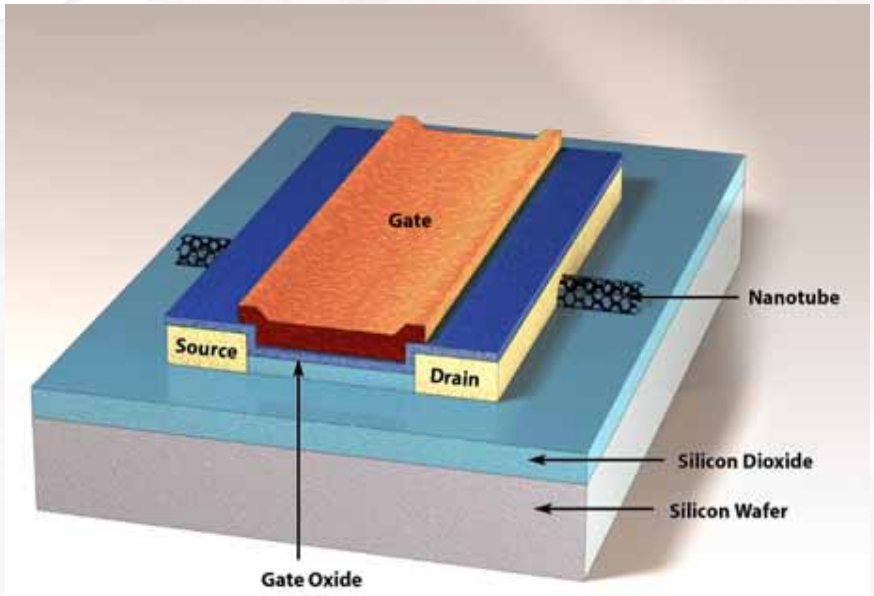
ITRS

M2 S2

P.Gargini

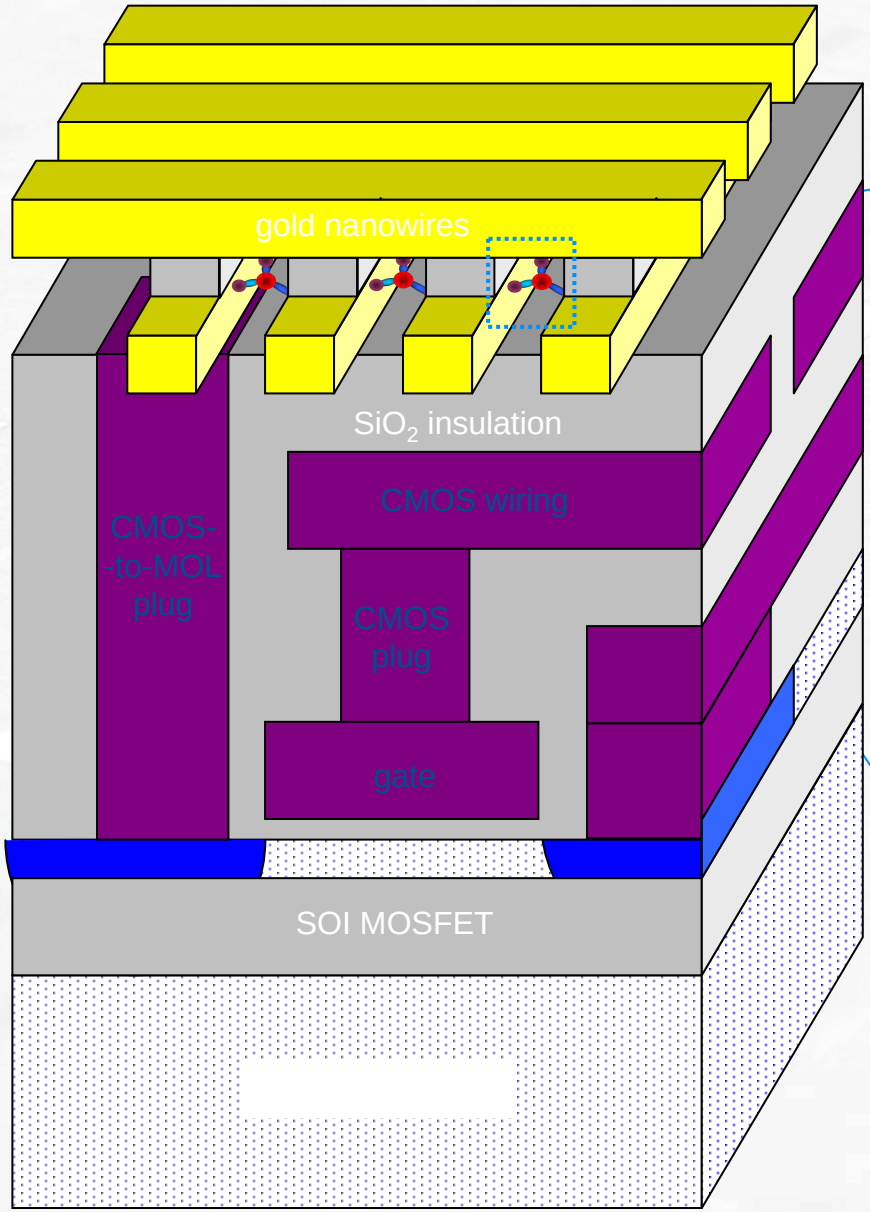
Non-classical CMOS does not include:

- **Classical CMOS : planar bulk CMOS / partially depleted SOI**
  - Materials, processes and device structures used since 1980's with extensive scaling (per Moore's Law)
- **Beyond-CMOS devices: fabricated with unique, non-Si material or utilizing non-MOSFET operation**
  - Single-electron transistor, quantum cellular array, neuromorphic, molecular, fullerenes, carbon nanotubes, or optical materials, etc.
  - Expected beyond time period of current ITRS.

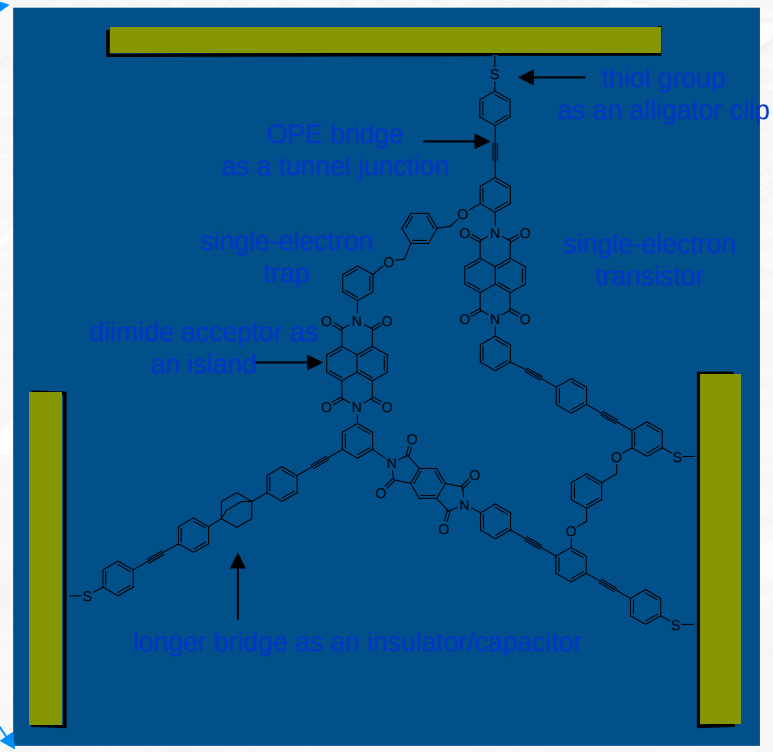


Nanotube FET [IBM]

CMOL CONCEPT



molecular single-electron latching switch



Possible density: 3×10^{12} functions per cm^2

K. Likharev and A. Mayr, 2002

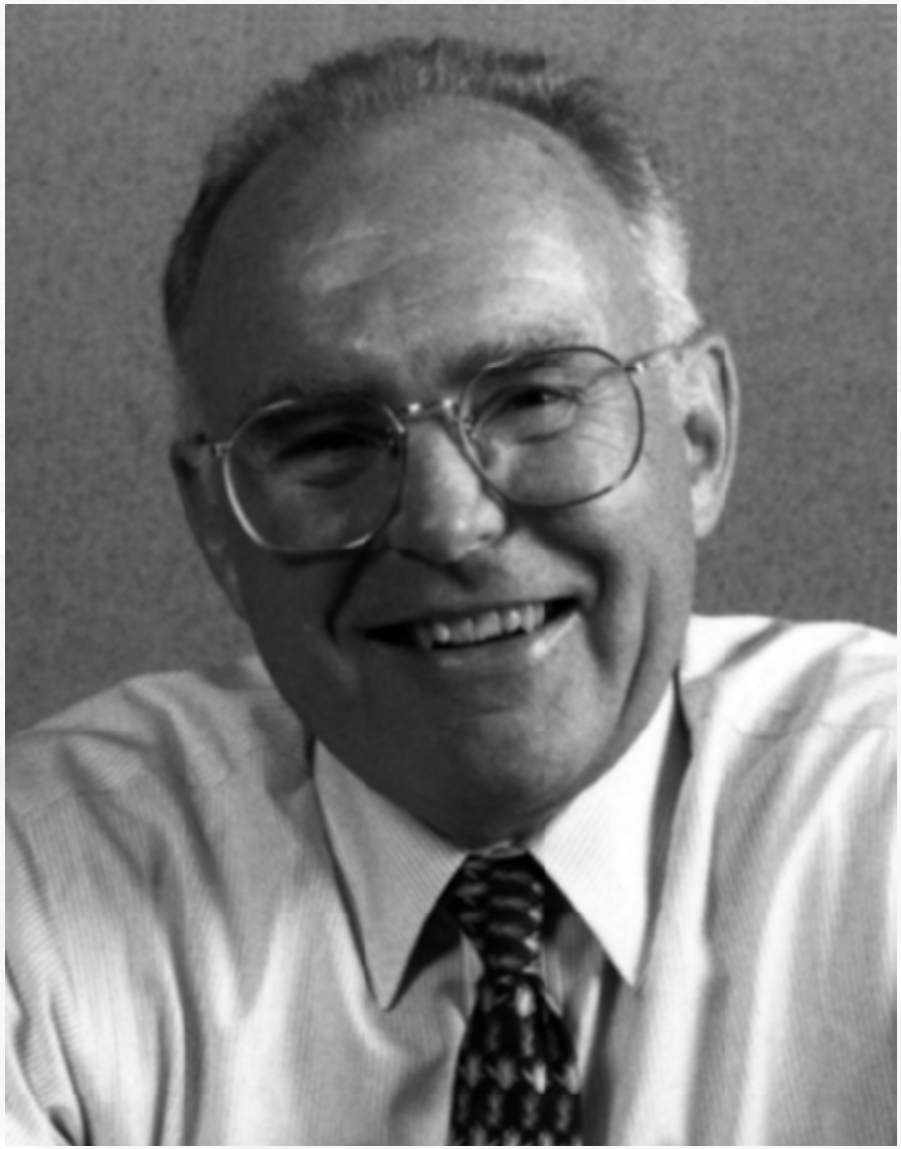
(see http://rsfq1.physics.sunysb.edu/~likharev/nano/GigaNano010603.pdf)

Microelectronics Revolution

- **Gordon Moore (a)**
  - "But then you see the numbers or hear your company's name on the evening news … and you are once again reminded that this is no longer just an industry, but an economic and cultural phenomenon, a crucial force at the heart of the modern world."
- **Gordon Moore (b)**
  - "No exponential is forever: but "forever" can be delayed!"

(a) Beyond Imagination:Commemorating 25 Years, SIA (2002) [Introduction by Gordon Moore]
(b) ISSCC 2003 / Session 1/ Plenary 1.1 (2003)

Gordon Moore



H.R.Huff,J. Electrochem. Soc., **149**, S35-S58 (2002) (© The Electrochemical Society,Inc., reproduced with permission)

John Bardeen

Courtesy of Lillian Hoddeson

Bob Dennard