March 18, 2005

Metrology for Emerging Devices and Materials

Eric M. Vogel Leader, CMOS and Novel Devices Group and Director, NIST AML Nanofab

NIST

Semiconductor Electronics Division
Gaithersburg, MD 20899

Outline

- Acknowledgments
- Trends in Electronics
- The End of CMOS?
- Beyond CMOS – Emerging Devices and Materials

- **Characterization Needs for Emerging Devices and Materials (using examples)**
  - Analytical characterization of chemical, structural, electrical, and atomic bonding at the nano-/atomic- scale.
  - Electrical test structures for timely characterization of electronic properties of nanoscale components (e.g. molecules, nanotubes, nanowires).

Acknowledgments
People

John Bonevich (TEM)
Christina Hacker (FTIR)
Joseph Kopanski (Scanning Capacitance Microscopy)
Sang-mo Koo (Nanowires)
Michael Gaitan (Single Molecule Measurement and Manipulation)
Qiliang Li (Nanowires)
Eric Lin et al. (Organic Electronics)
Seoung-Eun Park (Scanning Kelvin Probe)
Curt Richter (Molecular Electronics)
John-Henry Scott (Analytical Characterization)

Acknowledgments

CMOS and Novel Devices Group

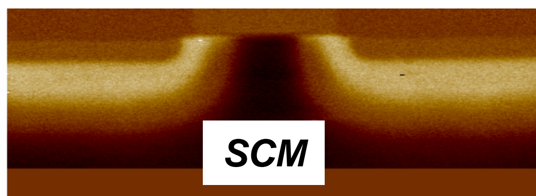
Performs research and development for the metrology, test structures, and reference materials required for CMOS and Beyond devices and their constituent materials.

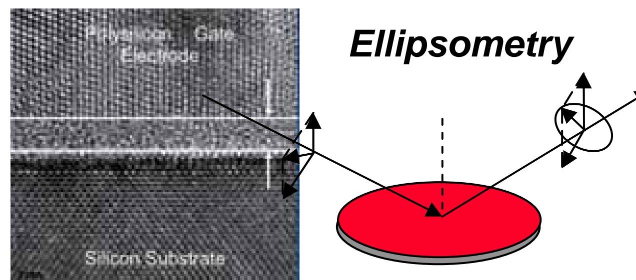
Summary of Core Competencies

1. Electrical characterization of CMOS and Beyond devices
2. Broad understanding of electronic materials characterization and surface science including specific expertise in SCM and Ellipsometry
3. Micro-/Nano- fabrication

1.

2.





3.

NIST

Acknowledgments
Intl. Tech. Roadmap for Semiconductors

Emerging Research Devices

Emerging Materials

Emerging Logic and Memory Devices

Emerging Architectures

Added to ERD in 2004

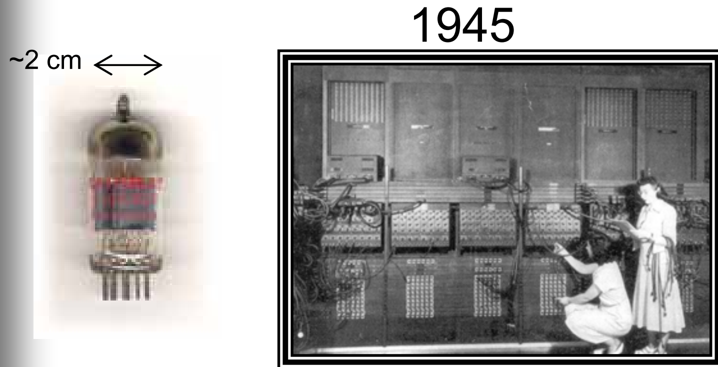
<u>Emerging Materials Scope</u>

- Materials to support ERD
- Synthesis
- **Characterization**
- Modeling

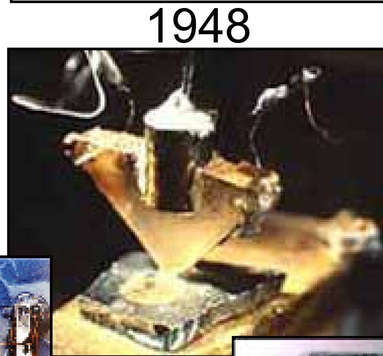
Trends in Electronics
Moore's Law

~2 cm

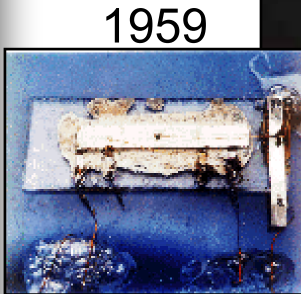
1945

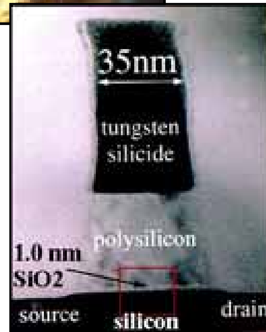


1948

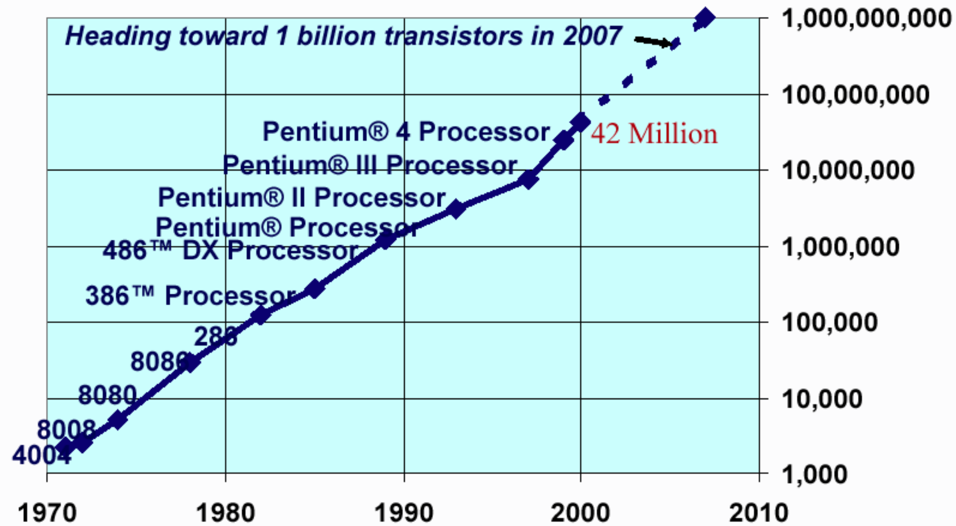


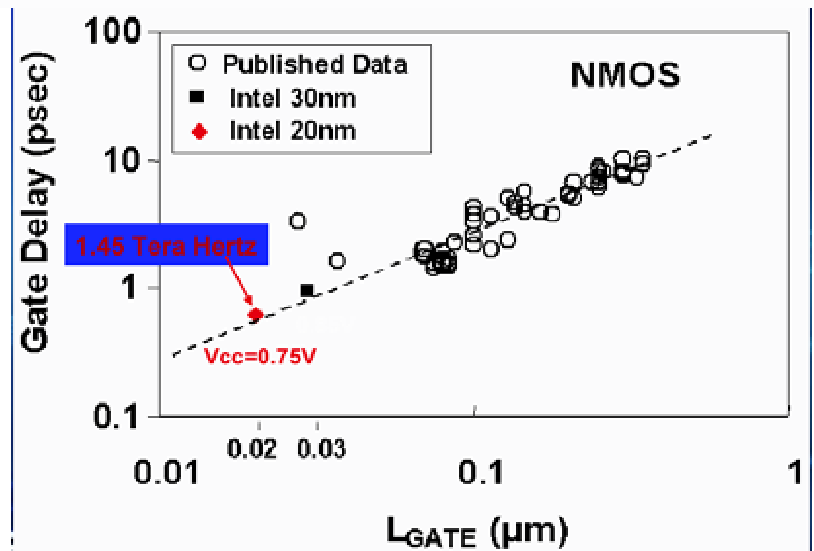
1959





2014





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Trends in Electronics

More than Moore's Law

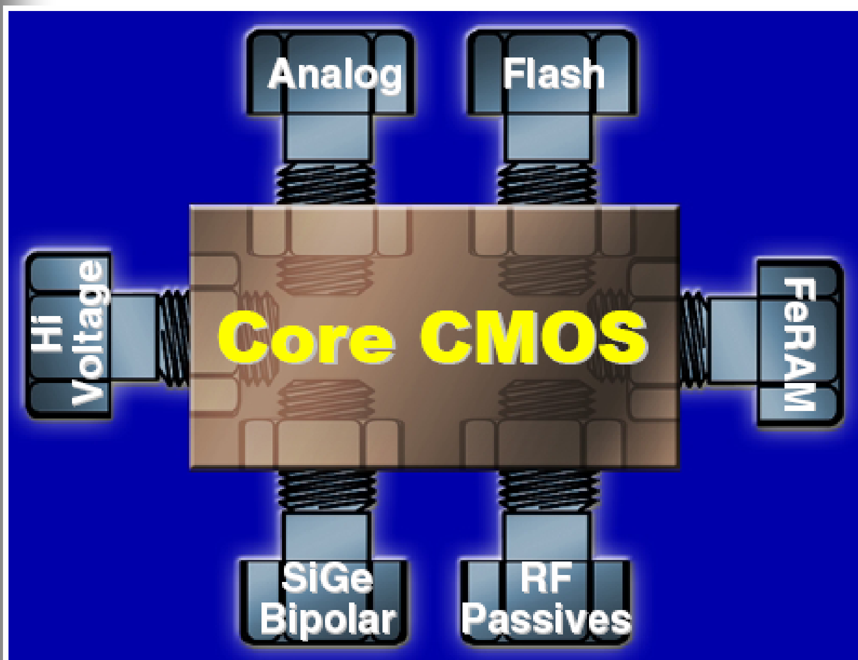
Moore's Law: Smaller, faster and cheaper logic and memory (CMOS and Beyond)

Functional Electronics: On-chip optical components, RF, power, sensors, bio tools, MEMS

Ubiquitous Electronics: Putting cheap electronics everywhere

Trends in Electronics
Functional Electronics

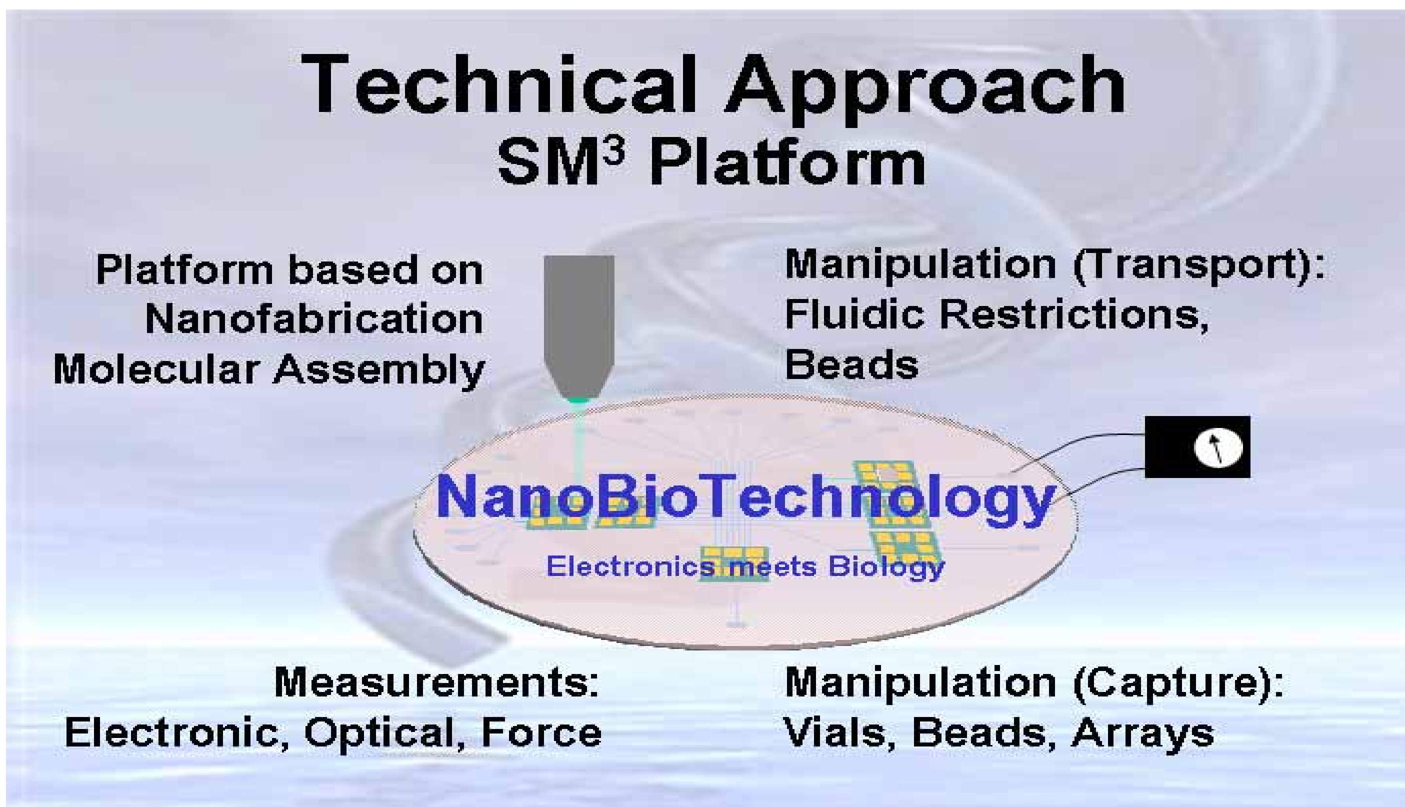
On-chip power, optical, memory, RF, sensors



Extracted from **Dennis Buss**' Centennial Lecture Series Talk at NIST,
"Jack Kilby's Invention and the Ensuing 40 Years of IC Technology Innovation,"
March 30, 2001

Trends in Electronics
Functional Electronics

On-chip molecular/biological manipulation and characterization using MEMS



M. Gaitan et al. (NIST)

NIST

Trends in Electronics

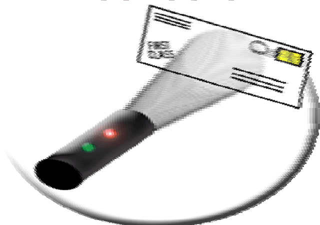
Ubiquitous Electronics

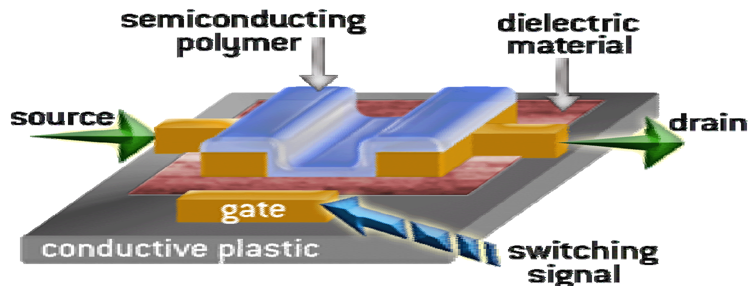
Organic Electronics

cheap dynamic signs

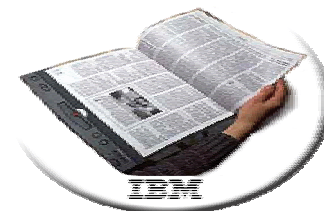
wearable electronics

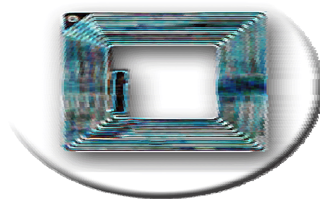
sensors



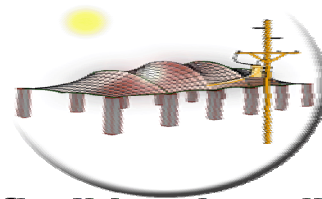


electronic paper





RFID tags

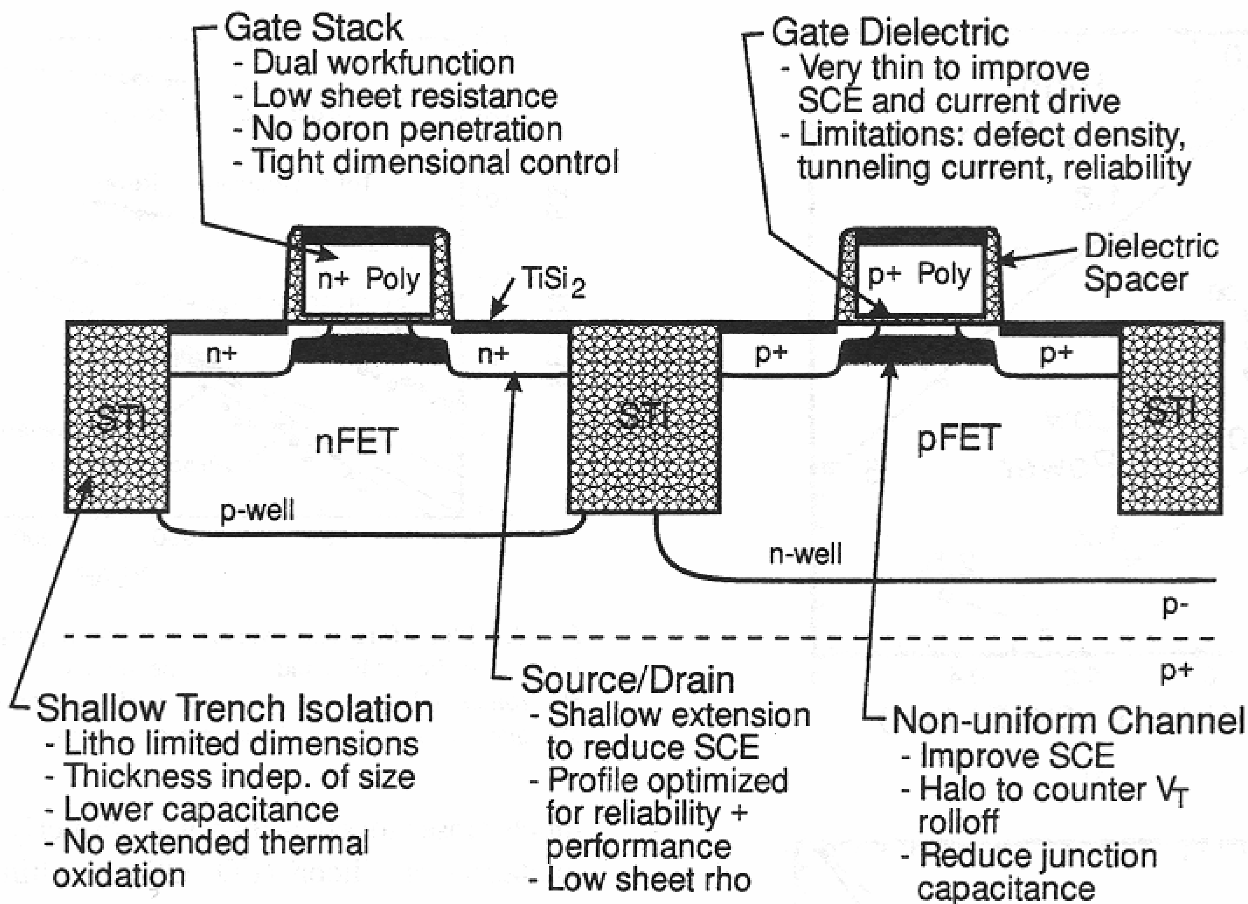


flexible solar cells

The NIST Organic Electronics Competence Team (E. Lin, C. Richter et al.), Marc Gurau and C. K. Chiang

The Basis of Moore's Law
CMOS

CMOS = Complementary Metal Oxide Semiconductor
FET = Field Effect Transistor



NIST

The End of CMOS?

Many "Red Brick Walls"

Possible "Red Brick Walls"

- Equivalent gate dielectric thickness <1nm
- Random dopant fluctuation
- Depletion of the polysilicon gate electrode
- Resistance of contact to devices too high

....

Table 71a Thermal and Thin Film, Doping and Etching Technology Requirements—Near-term

Year of Production	2003	2004	2005	2006	2007	2008	2009	*Driver*
Technology Node		hp90			hp65			
DRAM ½ Pitch (nm)	100	90	80	70	65	57	50	DRAM
MPU/ASIC ½ Pitch (nm)	107	90	80	70	65	57	50	MPU
MPU Printed Gate Length (nm)	65	53	45	40	35	32	28	MPU
MPU Physical Gate Length (nm)	45	37	32	28	25	22	20	MPU
Equivalent physical oxide thickness for MPU/ASIC T_{ox} (nm) [A, A1]	1.3	1.2	1.1	1.0	0.9	0.8	0.8	MPU
Gate dielectric leakage at 100°C (nA/µm) High-performance [B, B1, B2]	100	170	170	170	230	230	230	MPU

Table 71b Thermal and Thin Film, Doping and Etching Technology Requirements—Long-term

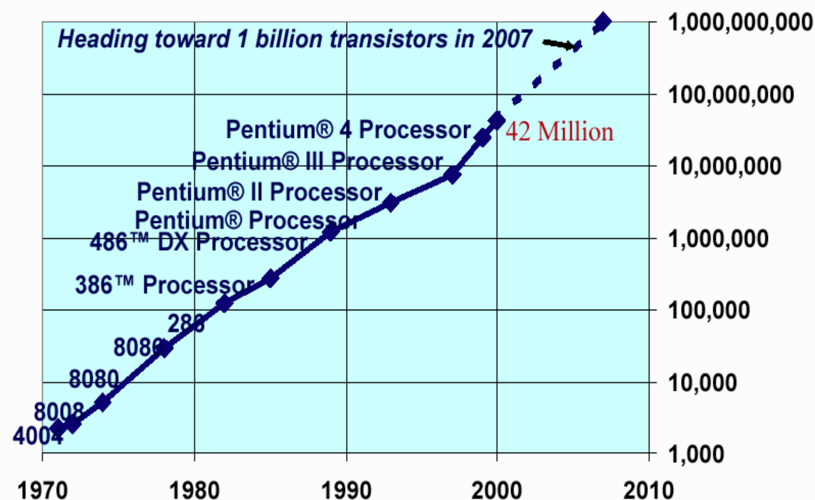
Year of Production	2010	2012	2013	2015	2016	2018	*Driver*
Technology Node	hp45		hp32		hp22		
DRAM ½ Pitch (nm)	45	35	32	25	22	18	DRAM
MPU/ASIC ½ Pitch (nm)	45	35	32	25	22	18	MPU
MPU Printed Gate Length (nm)	25	20	18	14	13	10	MPU
MPU Physical Gate Length (nm)	18	14	13	10	9	7	MPU
Equivalent physical oxide thickness for MPU/ASIC T_{ox} (nm) [A, A1]	0.7	0.7	0.6	0.6	0.5	0.5	MPU/ASIC
Gate dielectric leakage at 100°C (µA/µm) high-performance [B, B1, B2]	0.33	0.33	1	1.00	1.67	1.67	MPU/ASIC

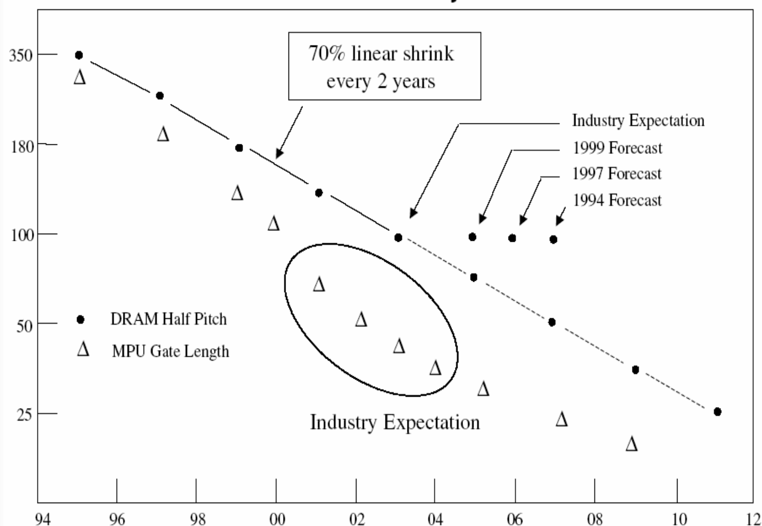
NIST

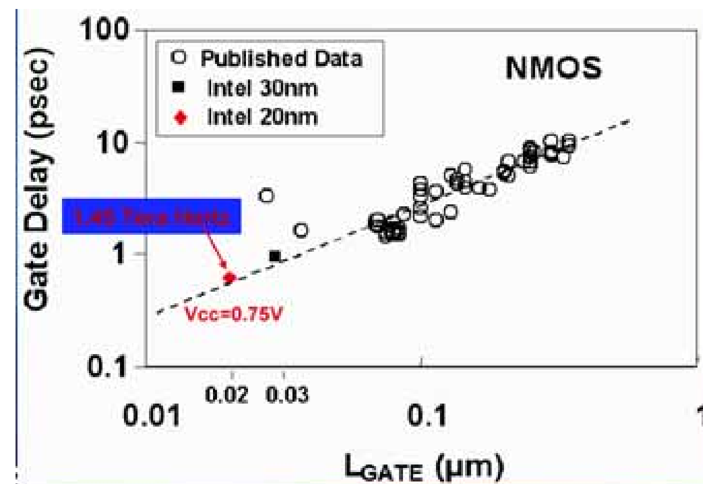
The End of CMOS?

It's Going to be Tough to Replace

- >> 10^9 devices
- << 10 nm feature size
- << 1 psec gate delay
- ~ 10 year reliability
- << 100 Watts*
- << $4B to fab*







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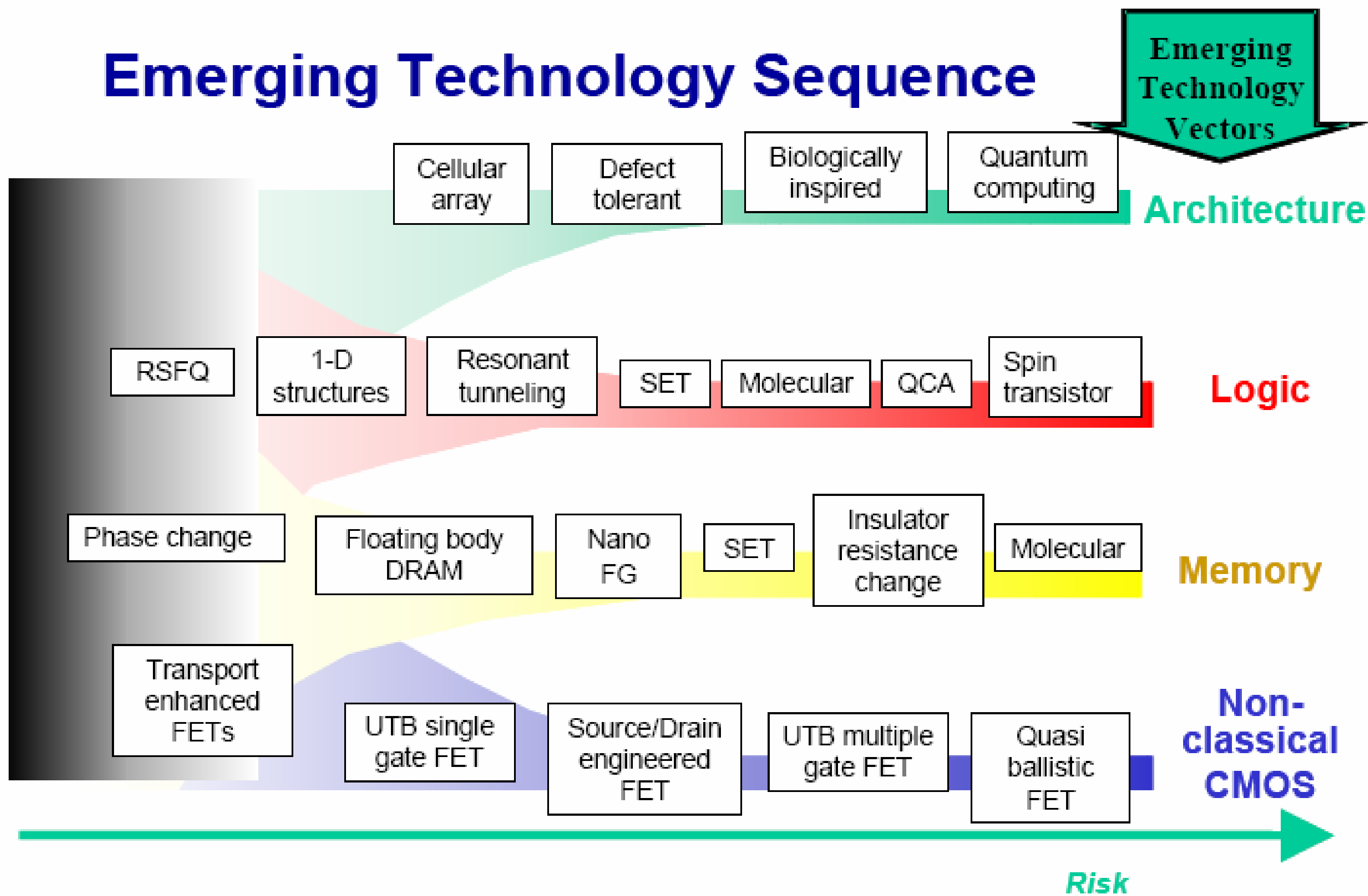
Beyond CMOS
Numerous Possibilities



Beyond CMOS

Emerging Logic Devices

Availability Sequence	1	2	2–3	2–3	4	5	6
Device	*FET*	*RSFQ*[A,B,C]	*1D structures*	*Resonant Tunneling Devices*	*SET*	*Molecular*	*QCA*[D]	*Spin transistor*
Types	▪ Si CMOS	▪ JJ	▪ CNT FET ▪ NW FET ▪ NW hetero-structures ▪ Crossbar nanostructure	▪ RTD-FET ▪ RTT	▪ SET	▪ 2-terminal ▪ 3-terminal FET ▪ 3-terminal bipolar transistor ▪ NEMS ▪ Molecular QCA	▪ E: QCA** ▪ M: QCA**	▪ Spin FET (SFET) ▪ Spin-valve transistor (SVT)
Supported Architectures	▪ Conventional	▪ Pulse	▪ Conventional ▪ Cross-bar	▪ Conventional ▪ CNN	▪ CNN	▪ Memory-based ▪ QCA	▪ QCA	▪ Quantum ▪ Programmable logic
Cell Size (spatial pitch)	100 nm*	0.3 µm	100 nm*	100 nm*	40 nm	Not known	60 nm	100 nm*
Density (device/cm^2)	3E9	1E6	3E9	3E9	6E10	1E12	3E10	3E9
Switch Speed	700 GHz	1.2 THz	Not known	1 THz	1 GHz	Not known	30 MHz	700 GHz
Circuit Speed	30 GHz	250–800 GHz	30 GHz	30 GHz	1 GHz	<1 MHz (NEMS)	1 MHz	30 GHz
*Switching Energy, J****	2×10^{-18}	2×10^{-19}(Nb) $[>1.4\times10^{-17}]$	2×10^{-18}	$>2\times10^{-18}$	1×10^{-18} $[>1.5\times10^{-17}]$[C]	1.3×10^{-16} (NEMS)	$[E: >1\times10^{-18}]$[E] M: $>4\times10^{-17}$	2×10^{-18}
Binary Throughput, GBit/ns/cm^2	86	0.4	86	86	10	N/A	0.06	86
Gain	Must be >>1 for all devices. See Table 63b for experimental values							
Operational Temperature	RT	▪ 4 K (Nb) ▪ 77 K (HTS) ▪ 20 K(MgB_2)	RT	RT	20 K	RT	E:QCA Cryogenic M:QCA RT	▪ Cryogenic (SFET) ▪ RT (SVT)
CD Tolerance	Critical	Not critical	Not critical	Very critical	Very critical	Not critical	Very critical <2% (M: QCA)	Critical
Materials System	Si	Nb HTS	CNT Si III-V	III-V Si-Ge	III-V Si	C-60	Al/Al_2O_3 (E: QCA)	▪ III-V (SFET) ▪ Si/FM (SVT)
Most Complex Circuit Demonstrated	See Table 63b							

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Emerging Memory Devices

Table 62a Emerging Research Memory Devices—Projected Parameters

	Present Day Baseline Technologies		*Phase Change Memory**	*Floating Body DRAM*	*Nano-floating Gate Memory***	*Single/Few Electron Memories***	*Insulator Resistance Change Memory***	*Molecular Memories***
Storage Mechanism								
Device Types	DRAM	NOR Flash	OUM	1TDRAM	Engineered tunnel barrier or nanocrystal	SET	MIM	Bi-stable switch
Availability	2004	2004	~2006	~2006	>2006	>2007	~2010	>2010
Cell Elements	1T1C	1T	1T1R	1T	1T	1T	1T1R	1T1R
Initial F	90 nm	90 nm	100 nm	70 nm	80 nm	65 nm	65 nm	45 nm
Cell Size	$8F^2$ 0.065 μm^2	$12.5F^2$ 0.101 μm^2	$\sim 6F^2$ 0.06 μm^2	$\sim 4F^2$ [A] 0.0049 μm^2	$\sim 6F^2$ 0.038 μm^2	$\sim 6F^2$ 0.025 μm^2	$\sim 6F^2$ 0.025 μm^2	Not known
Access Time	<15 ns	~80 ns	<100 ns	<10 ns [A,B]	<10 ns	<10 ns	Slow	~10 ns
Store Time	<15 ns	~1 ms	<100 ns	<10 ns [A,B]	<10 ns	<100 ns	<100 ns	~10 ns
Retention Time	64 ms	10–20 yrs	>10 yrs	<10 ms [A]	>10 yrs	~100 sec	~1 year	~1 month
E/W Cycles	Infinite	1E5	>1E13	>1E15 [A]	>1E6	>1E9	>1E3	>1E15
General Advantages	▪ Density ▪ Economy	▪ Non-volatile ▪ Multi-bit cells	▪ Non-volatile ▪ Low power ▪ Rad hard ▪ Multi-bit cells	▪ Density ▪ Economy	▪ Non-volatile ▪ Fast read and write ▪ Multi-bit cells	▪ Density ▪ Low power	▪ Low voltage ▪ Multi-bit cells	▪ Density ▪ Low power ▪ 3D potential ▪ Defect tolerant
Challenges	▪ Scaling	▪ Scaling	▪ Large E/W current ▪ New materials and integration	▪ Need SOI ▪ Retention versus scaling ▪ Dopant fluctuation ▪ Endurance	▪ Material quality	▪ Dimension control for RT operation ▪ Background charge disturb	▪ New materials and integration ▪ Slow access ▪ Speed versus R trade-off	▪ Volatile ▪ Thermal stability
Maturity	Production	Production	Development	Demonstrated	Research	Research	Research	Research
*Research Activity*****			3***	3	61	40	3	43

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Characterization Needs for Emerging Devices and Materials

Analytical <u>characterization</u> of chemical, structural, and electrical, properties at the nano-/atomic- scale.

- Unlikely to find one "holy grail"
- Need 2D/3D
- Need Å spatial resolution
- Need atomic sensitivity
- Need subsurface characterization (specifically organic/inorganic).
- Need to profile local properties

Electrical test structures for timely characterization of electronic properties of nanoscale components (e.g. molecules, nanotubes, nanowires).

- Results must be independent of contacts
- Need independent confirmation of results

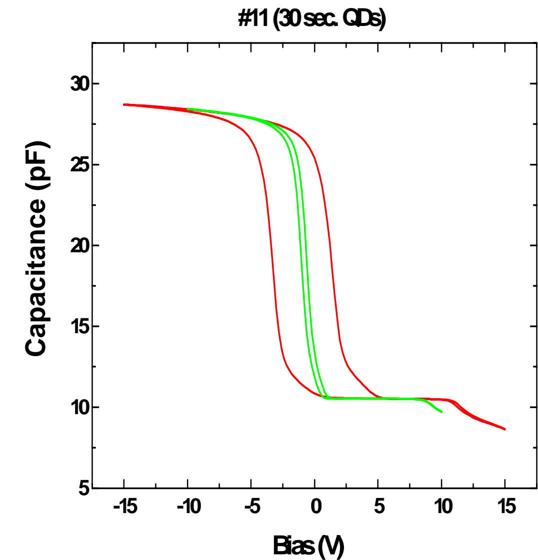
Analytical Characterization

Unlikely to Find One "Holy Grail"

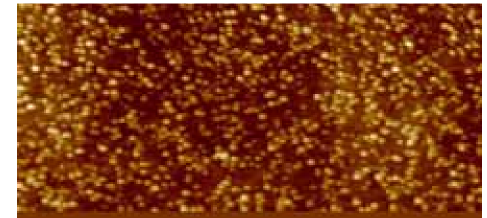
• Quantum dot memories generally show hysterisis and retention time that is strongly dependent on the size and distribution of the dots.

• The measured size of the quantum dots determined using AFM is larger than that determined using TEM.

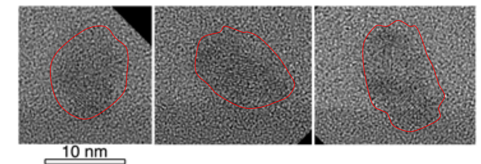
C-V



AFM



TEM



†J. Park, C. A. Richter, J. Y. Kim, N. V. Nguyen, J. E. Bonevich, and E. M. Vogel, 'Characterization of ultrathin amorphous silicon and correlation with crystalline evolution after thermal annealing,' 2003 MRS Spring Meeting.

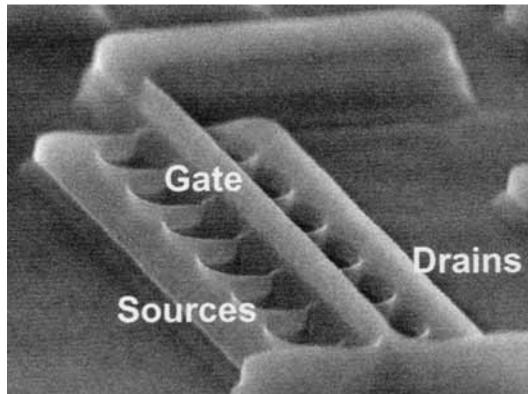
Analytical Characterization

Need 3D

FIN/Tri-gate FETs are based upon Si-nanowires

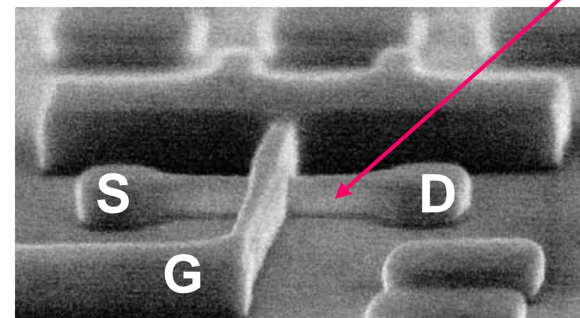
Need to monitor:

- 3D properties…
  - Accurate size of wire
  - Film thicknesses (ie, gate dielectric) on a 3D structure
- 3D Processing parameters:
  Pattern/orientation dependent oxidation?



Multiple Si-nanowire FET

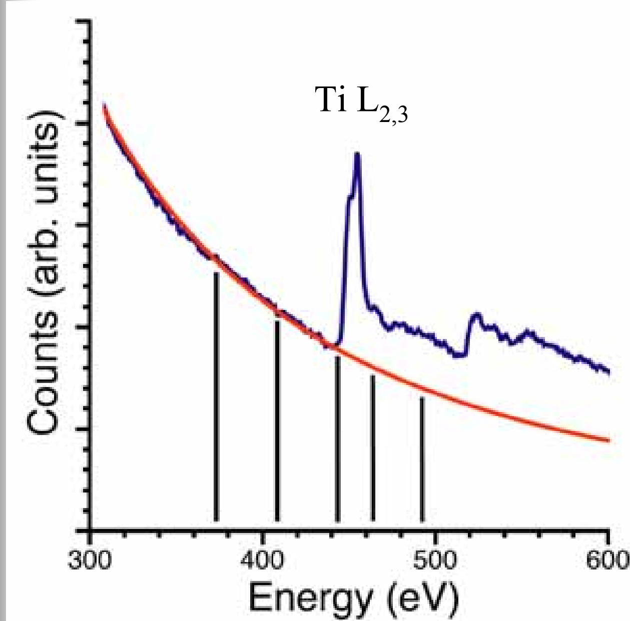
Silicon nanowire



Intel

Analytical Characterization

2D Compositional Mapping



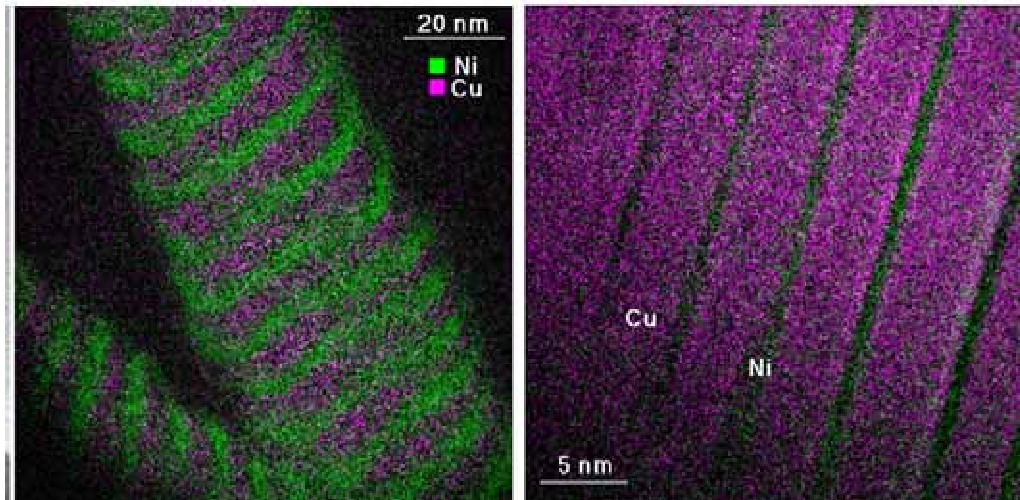
Energy Filtered Imaging

Spatial Resolution, $d = C_c\ ß\ \Delta E/E_0$

C_c = 1.4 mm, ß = 10 mrad,
ΔE = 20 eV, E_0 = 300 keV

∴ d ≈ 1 nm

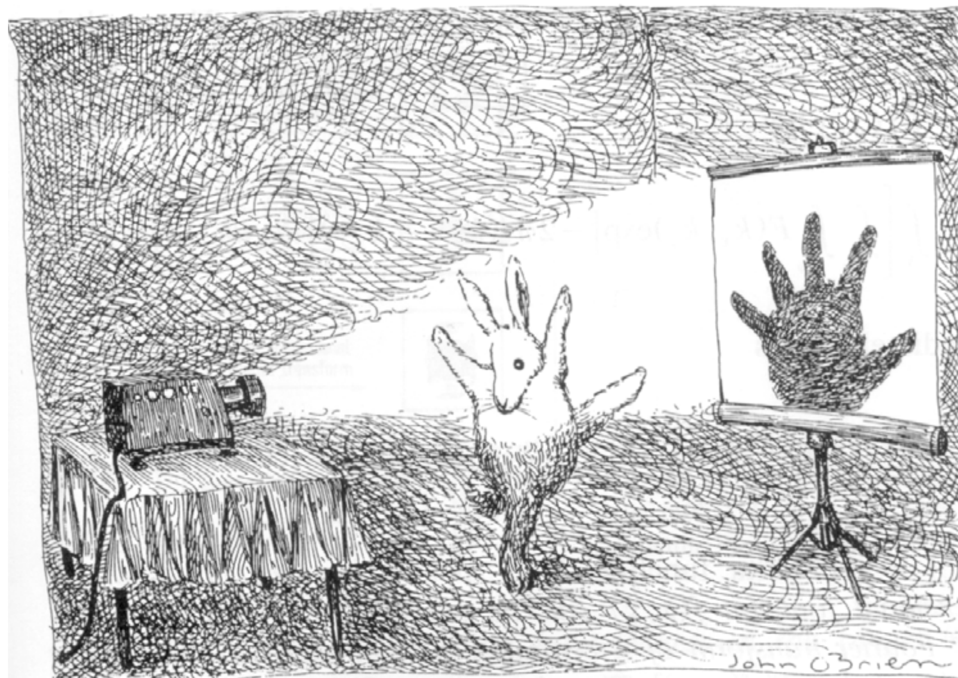
"Tuning the Magnetic Properties of Multilayer Nanowires,"
M. Chen, L. Sun,
J.E. Bonevich, D.H. Reich,
C.L. Chien, and P.C. Searson,
Appl. Phys. Lett., **82** (2003) 3310.



Analytical Characterization
Need 3D

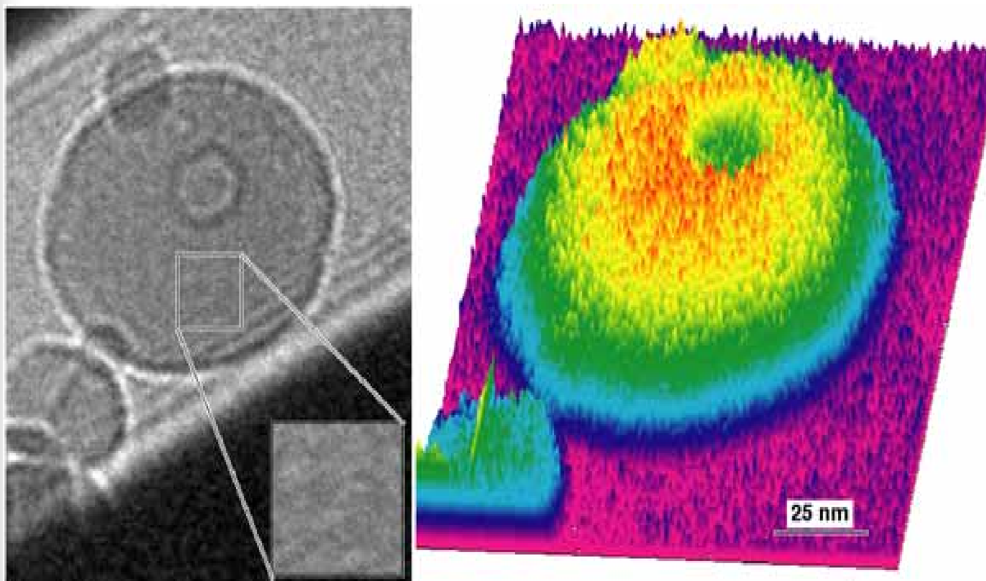
J.-H. Scott (NIST)

- Currently, most used approach is 2D projection or surface morphologic imaging with limited chemical mapping
- This approach can easily lead to misinterpretation
- Chemical 3D information is required.



Drawing by John O'Brien, The New Yorker Magazine (1991)

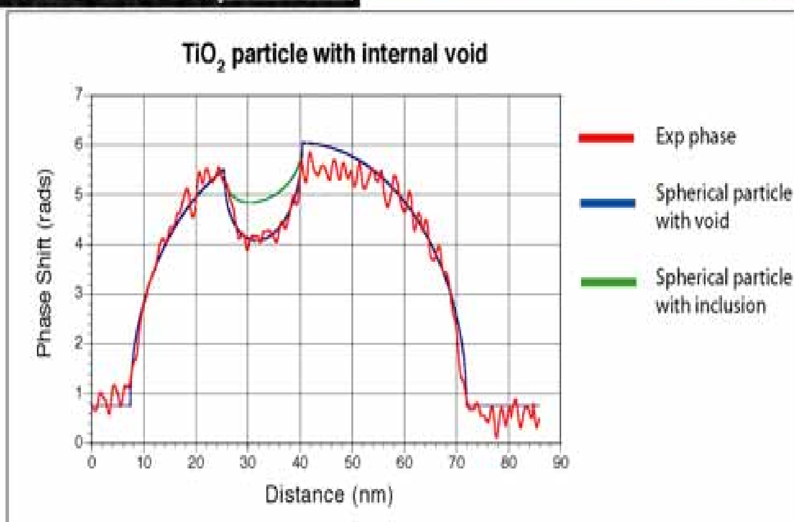
Analytical Characterization
3D Holography using TEM

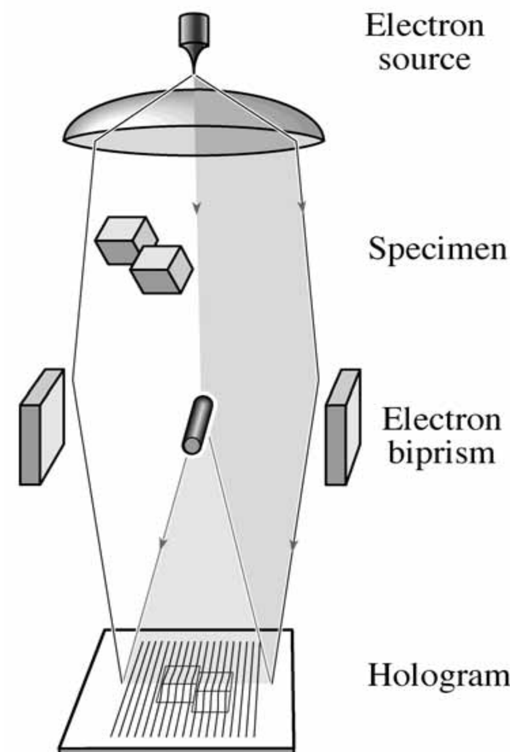


Electron phase shifts are sensitive to variations in:

Mean inner potential (thickness)

Electro-magnetic fields (fluxons, pn junctions)





Analytical Characterization

Need Å Resolution and Atomic Sensitivity

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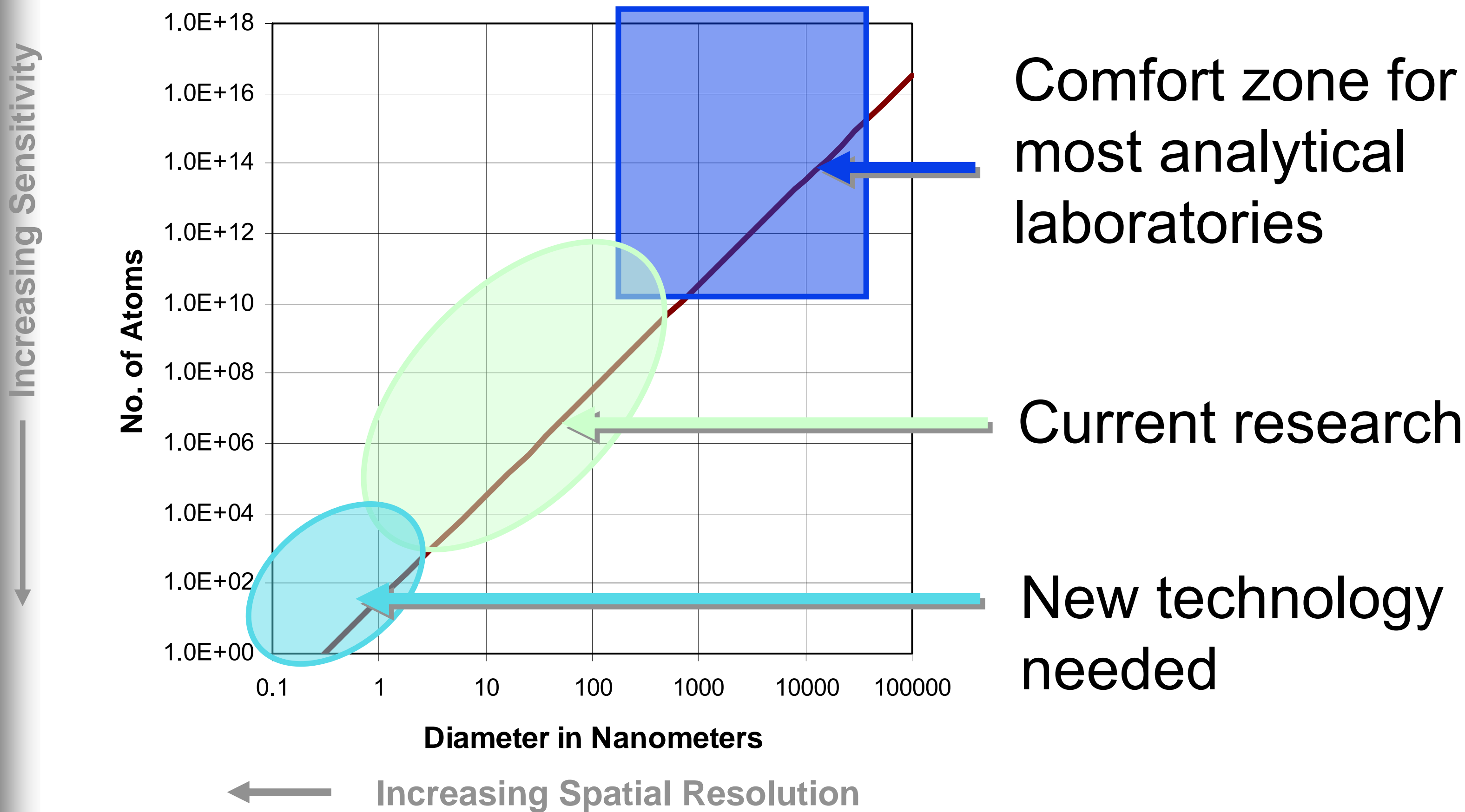
J.-H. Scott (NIST)



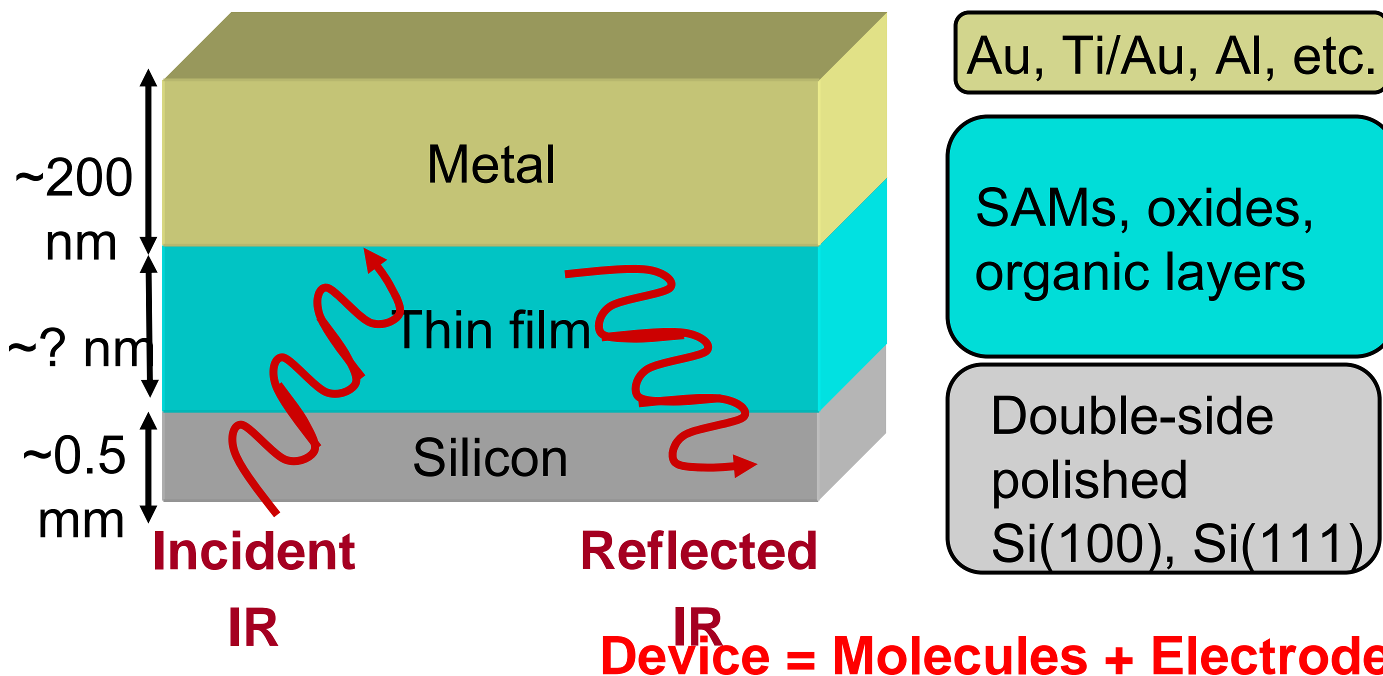
Analytical Characterization

Need Subsurface Characterization

Backside FTIR

C. Hacker (NIST)

Spectroscopic characterization of the buried metal-SAM interface can be studied by using infrared radiation through IR-transparent substrates and thin films.



Device = Molecules + Electrodes

*Characterizing the structure of organics is a problem.

Analytical Characterization

Need Subsurface Characterization

Au (and Al): minimal perturbation

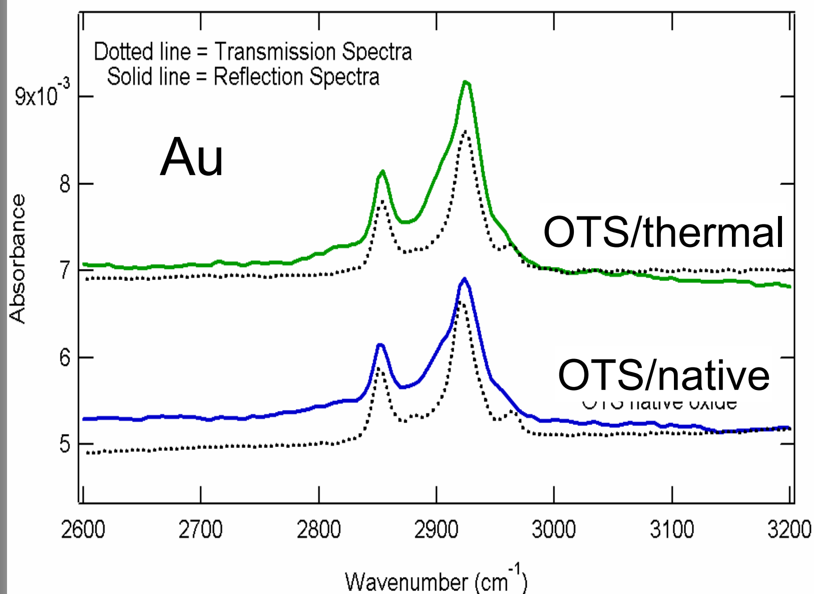
Ti: strong perturbation (but not complete destruction)

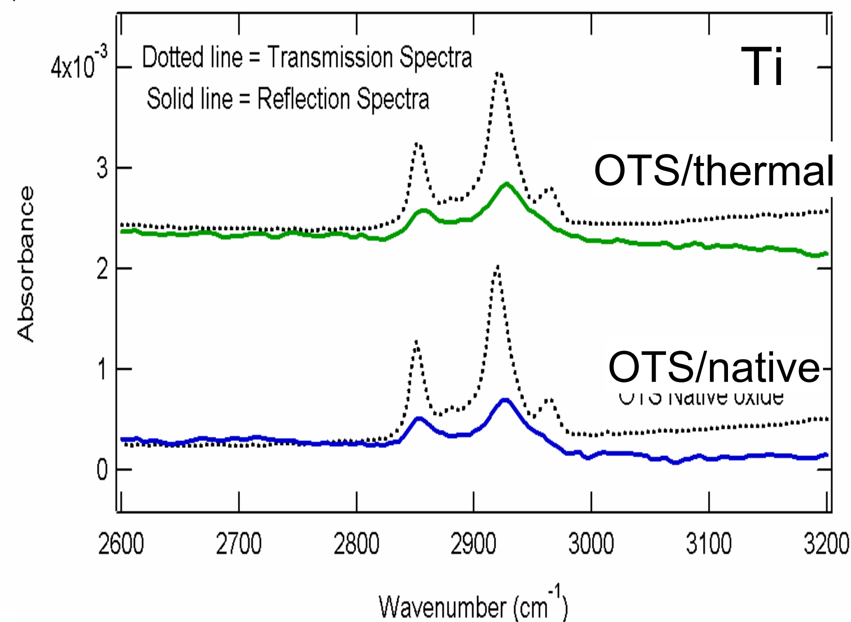
Pb-RAIRS Spectra

Transmission Spectra

Backside FTIR

C. Hacker (NIST)





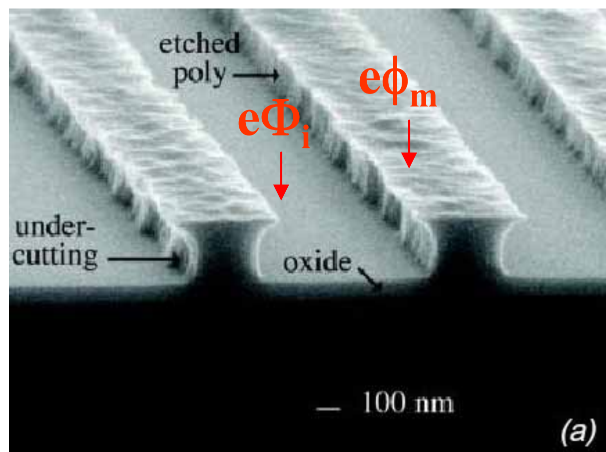
Analytical Characterization

Need to Profile Local Electronic Properties

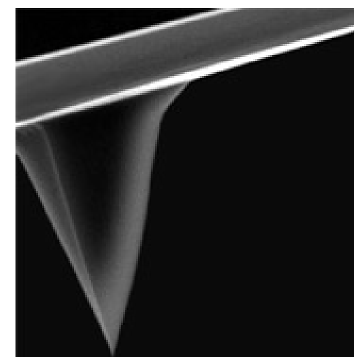
Scanning Kelvin to profile the surface potential

- Non-contact/destructive measurements of variations in surface potential
- Available for mapping local charge distributions
- Able to monitor processes
- Capable of determining the relative work functions of a conducting surface with a precision of 2~3 meV and a spatial resolution of about 10 nm

S.-E. Park (NIST)



(A conventional MOS structure)



(SKPM tip radius ≈ 10 nm)

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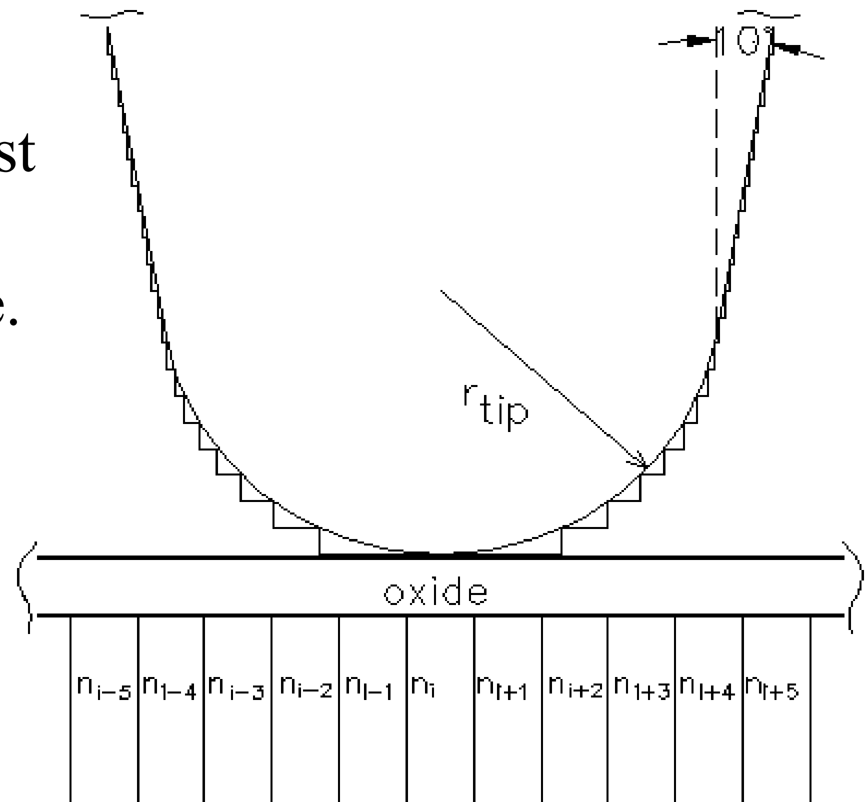
Analytical Characterization

Need to Profile Properties

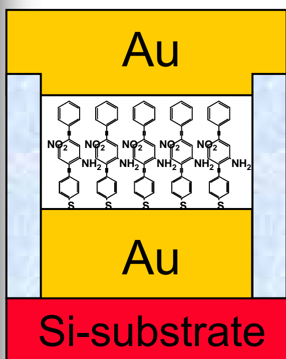
• The true tip geometry must be deconvolved from the measurement of the sample.

J. Kopanski (NIST)



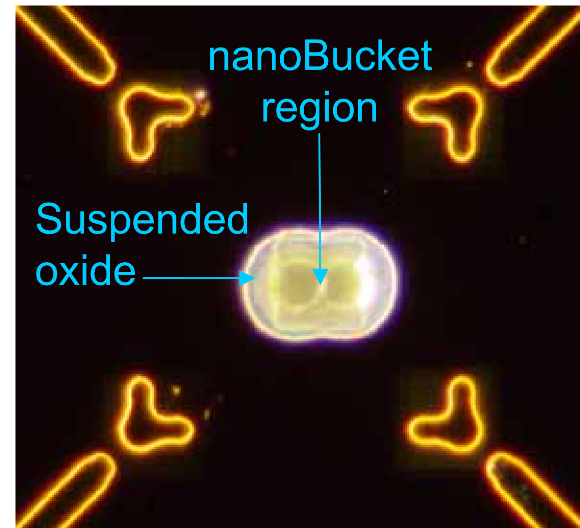
Electrical Test Structures
Molecular Electronics

A Device prototype that enables robust electrical measurements of molecules



Schematic of planar nanoBucket

Criteria:
- Characterizes Molecules
- Tunable to fit Molecules
- Prototypical Device Structure
- "Makeable" (i.e., transferable)



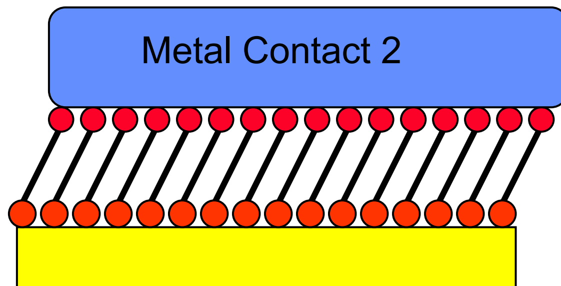
C. Richter (NIST)

NanoBuckets allow control:
- Variety (contacts & molecules)
- Depth (molecular length)
- Area (no. of molecules)

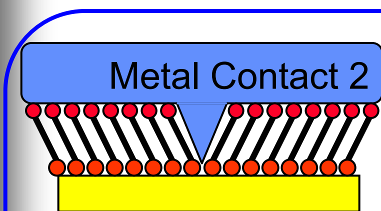
Electrical Test Structures

Contacts

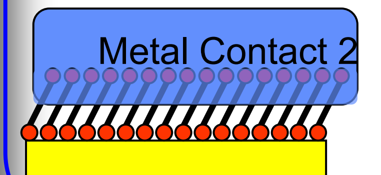
"Ideal structure"



1. Non-invasive top-metal
2. Well-ordered monolayer
3. Smooth bottom contact



- Most common failure mode during fabrication is physical shorting of top- to bottom-metal through molecular monolayer



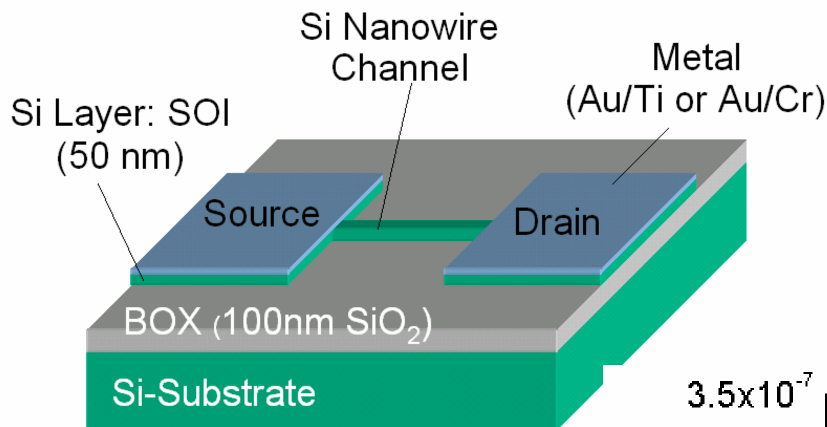
- Observed electrical behavior in moletronic devices is often not intrinsic to molecules, but attributed to metal interfaces/behavior.

C. Richter (NIST)

We must learn how to successfully put metals on monolayers for molecular electronics to succeed.

Electrical Test Structures

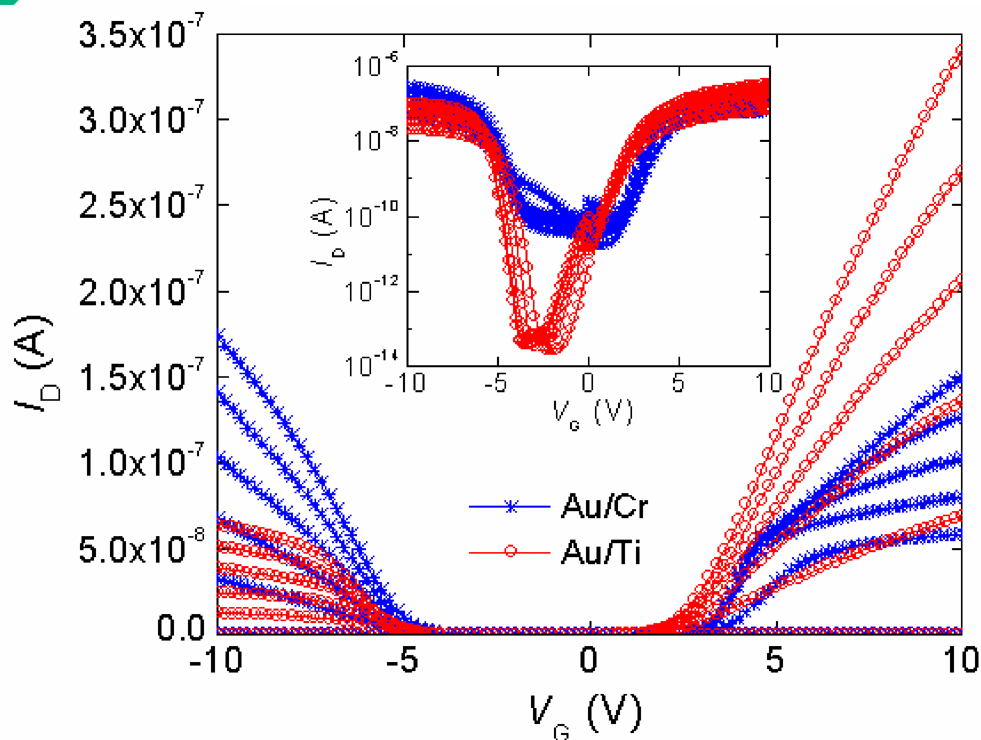
Contacts



SiNW - Length: 28 μm
Width: ~60 nm
Thickness: ~50nm

Nanowires transistors with different metal contacts (Cr, Ti) were fabricated.

The metal contacts to the nanowire strongly influence the conduction characteristics.



S. M. Koo (NIST)

NIST

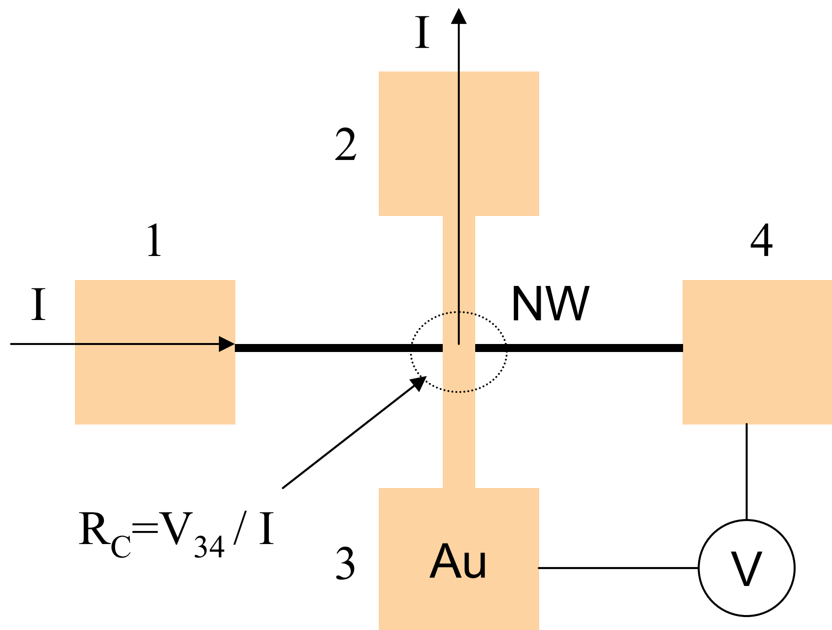
"Metrology for Emerging Devices and Materials"
Eric M. Vogel

2005 Intl. Conf. on Char. and Metrology for ULSI Technology

Electrical Test Structures
Contacts

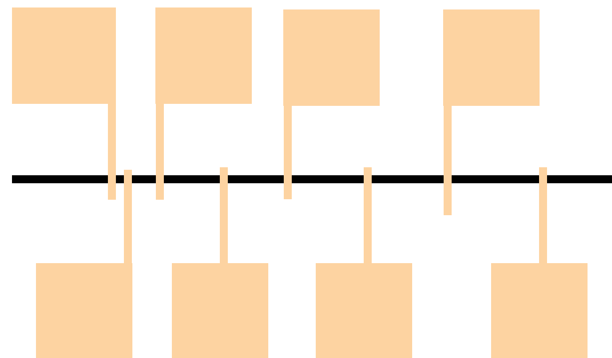
Methods to characterize the contact resistance to nanowires

4-point Kelvin test structure



Q. Li (NIST)

Transfer length method structure

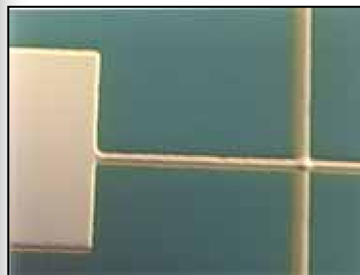


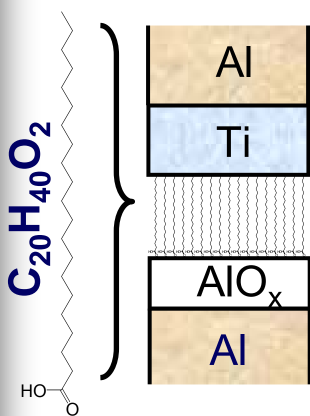
$R_{total} = (\rho_{nw}/S_{nw})d + 2R_C$

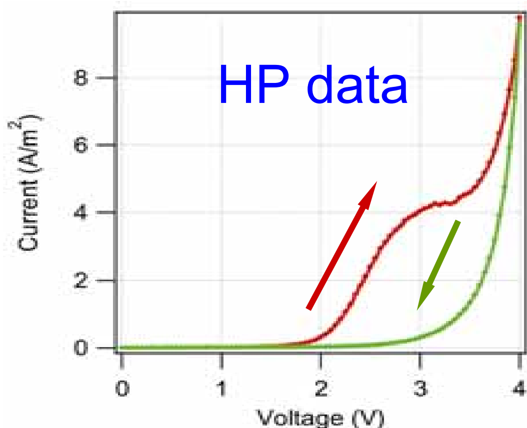
Use linear-fit of $R_{total} \sim d$

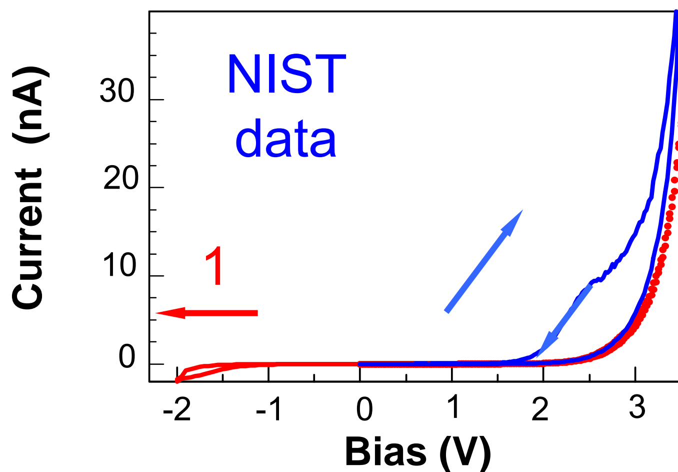
R-intercept is $2R_C$

Electrical Test Structures
Reproducible Data









- **First independent confirmation of molecular device behavior. (Switching observed at both NIST and HP.)**

C. Richter (NIST)

CA Richter (NIST) & DR Stewart (HP)

Device = Molecules + Electrodes

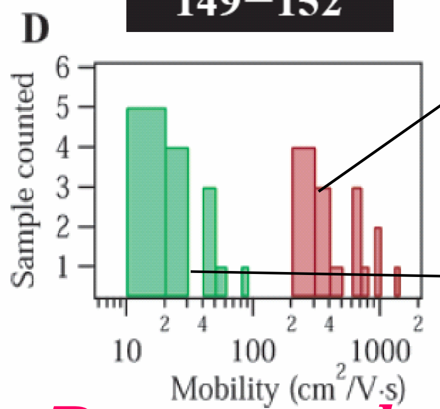
“Metrology for Emerging Devices and Materials”
Eric M. Vogel

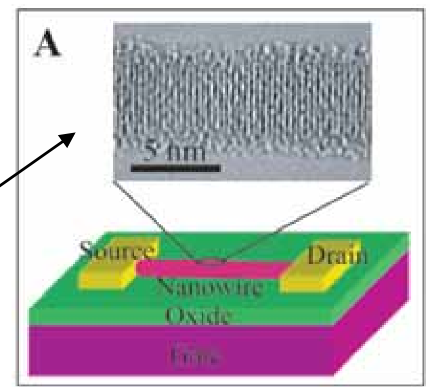
2005 Intl. Conf. on Char. and Metrology for ULSI Technology

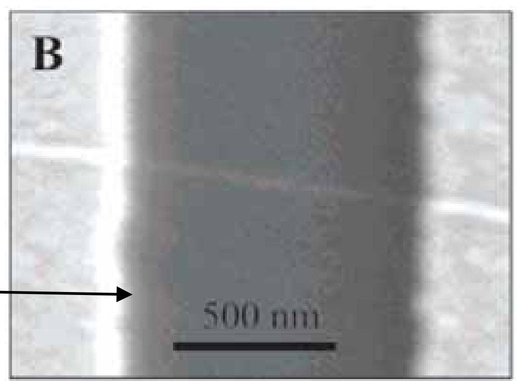
Electrical Test Structures
Reproducible Data

SiNW FETs – Lieber et al.

NANO LETTERS
2003
Vol. 3, No. 2
149–152





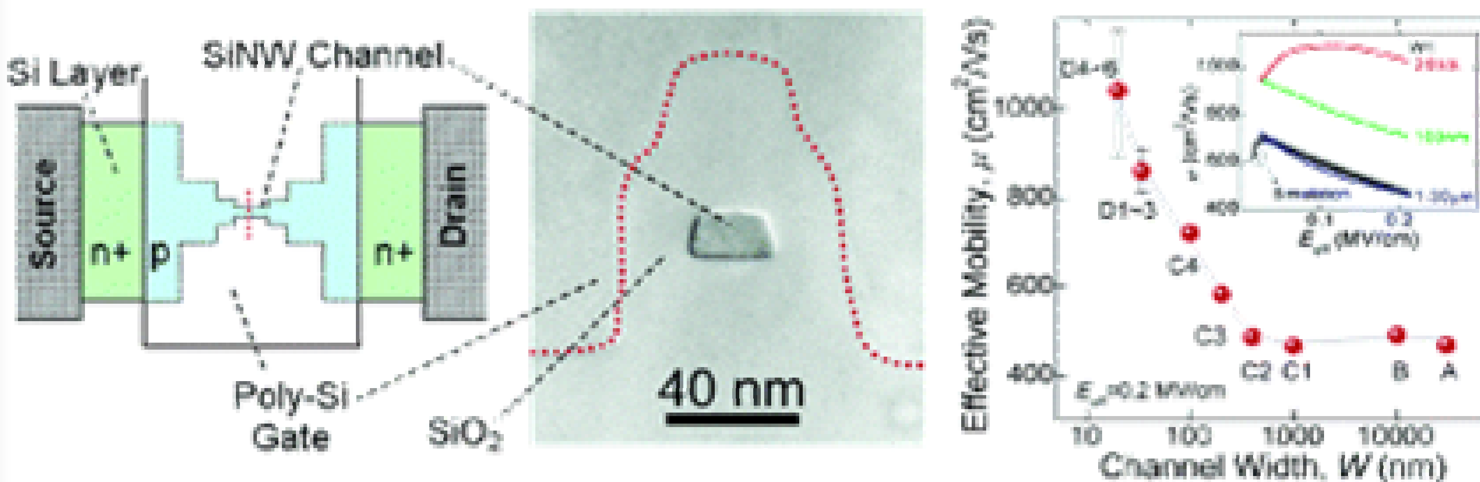


Recent results by Lieber et al. suggest that silicon nanowires may have hole mobility much greater than that of bulk silicon => this result was in question.

Electrical Test Structures
Reproducible Data

High Inversion Current in Silicon Nanowire Field Effect Transistors
Sang-Mo Koo, Akira Fujiwara, Jin-Ping Han, Eric M. Vogel,
Curt A. Richter, and John E. Bonevich

Web Release Date: 30-Sep-2004; *NanoLetters*



Using geometrically controlled test structures, the dependence of mobility on nanowire width was determined.

Summary

- The future of electronics involves many thrusts: Moore's Law (faster, smaller, cheaper CMOS and Beyond), Functional Electronics (On-chip optical components, RF, power, sensors, bio tools, MEMS), and Ubiquitous Electronics (Cheap electronics everywhere).
- There are many "red brick walls" for CMOS technology, but it will likely continue for the foreseeable future.
- There are numerous emerging architectures, logic & memory devices, and materials that are being researched for Beyond CMOS.

Characterization Needs for Emerging Devices and Materials

Analytical characterization of chemical, structural, electrical, and atomic bonding at the nano-/atomic- scale.

- Unlikely to find one "holy grail"
- Need 2D/3D
- Need Å spatial resolution
- Need atomic sensitivity
- Need subsurface characterization (specifically organic/inorganic).
- Need to profile local properties

Electrical test structures for timely characterization of electronic properties of nanoscale components (e.g. molecules, nanotubes, nanowires).

- Results must be independent of contacts
- Need independent confirmation of results