CHIPS for AMERICA

The Vision for the National Advanced Packaging Manufacturing Program

CHIPS Research and Development Office

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CHIPS for AMERICA

NIST NATIONAL INSTITUTE OF STANDARDS AND TECHNOLOGY
U.S. DEPARTMENT OF COMMERCE

CHIPS for America includes the CHIPS Program Office, responsible for semiconductor incentives, and the CHIPS Research and Development Office, responsible for R&D programs. Both sit within the National Institute of Standards and Technology (NIST) at the Department of Commerce.

NIST promotes U.S. innovation and industrial competitiveness by advancing measurement science, standards, and technology in ways that enhance economic security and improve our quality of life. NIST is uniquely positioned to successfully administer the CHIPS for America program because of the bureau's strong relationships with U.S. industries, its deep understanding of the semiconductor ecosystem, and its reputation as fair and trusted.

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BACKGROUND

President Biden's CHIPS and Science Act appropriated $50 billion to the Department of Commerce's CHIPS for America program to support both research and development (R&D) and return manufacturing to the United States. This includes $39 billion for the Department of Commerce (the Department) to onshore semiconductor manufacturing through an incentives program and $11 billion to advance U.S. leadership in semiconductor research and development. The research and development advances will be realized through four programs: the National Semiconductor Technology Center (NSTC), the National Advanced Packaging Manufacturing Program (NAPMP), the CHIPS Metrology Program, and Manufacturing USA institute(s).[1] These investments, across both R&D and incentives, further President Biden's Investing in America agenda to strengthen U.S. competitiveness, support domestic manufacturing and innovation, and create good jobs across the country.

The Department administers the CHIPS for America program through two offices, the CHIPS Program Office, which manages the $39 billion incentives program, and the CHIPS Research and Development Office, which manages the $11 billion research and development program. These programs are complementary and strengthen American manufacturing, supply chains, and national security. They invest in research and development, science and technology, and the workforce of the future to keep the United States leading the industries of tomorrow. Since passage of the CHIPS Act, the Department has and will continue to communicate the vision and strategy for the various programs of both the CHIPS Research and Development and CHIPS Program Offices.[2]

CHIPS for AMERICA

PACKAGING

VISION

The CHIPS Research and Development Office's vision for success of the National Advanced Packaging Manufacturing Program is to establish U.S. leadership in advanced packaging and provide the technology needed for packaging manufacturing in the U.S.

Furthermore, within a decade, NAPMP-funded activities, coupled with CHIPS manufacturing incentives, will establish a vibrant, self-sustaining, profitable, high-volume, onshore packaging industry where advanced node chips manufactured in the United States are packaged in the United States.

PURPOSE

This paper serves two purposes:

1. To provide more details on the NAPMP vision to the packaging community in advance of future funding opportunities, and
2. To outline the planned NAPMP investment areas in innovations that will help realize the ambitious goals for U.S. technology leadership in advanced packaging for the American semiconductor industry.

OPPORTUNITIES IN ADVANCED PACKAGING

Investments in semiconductors will not succeed without investments in advanced packaging. The CHIPS and Science Act offers a once-in-a-generation opportunity to establish a domestic competitive advanced packaging capability in semiconductor manufacturing.

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The rate of miniaturization expressed by Moore's Law alone can no longer improve performance of microelectronic technologies. Improving all aspects of packaging system performance to support the breadth of semiconductor applications, each with different performance metrics (e.g., speed, power, and thermal properties) requires advanced packaging to further push the application boundaries. Advanced packaging innovations are central to achieving these requisite continued performance improvements.

Semiconductor packaging serves two general purposes. The first is to protect the chip mechanically, thermally, and environmentally. The second is to facilitate reliable inter-chip communication, deliver power, and provide a stable test and system integration platform.

Advanced packaging and capabilities, such as heterogeneous integration, encompass the need to integrate multi-component-assemblies with large numbers of interconnects to achieve a degree of integration that blurs the line between chip and package. The ability to "scale-down and scale-out" will be critical, where the term "scale-down" commonly refers to shrinking the size of features on the package, and the term "scale-out" refers to increasing the number of chips assembled on the substrate. This scaling is highly interdisciplinary with many interdependencies.

Advanced packaging allows manufacturers to make improvements in performance and function and to shorten time to market. Additional benefits include a reduced physical footprint, lower power, increased chip reuse, and potentially decreased costs, allowing for more diverse and customizable manufacturing lots.

In addition, the vast majority of advanced packaging manufacturing capacity currently resides in Asia.[3] As the CHIPS for America program invests in leading-edge semiconductor design and fabrication, there is a need to develop a domestic advanced packaging manufacturing capability that is cost effective and efficient to enable semiconductors that are made in the United States to be packaged in the United States. This end state is necessary to sustain U.S. global competitiveness and to maintain supply chain security and resilience.

The NAPMP offers an opportunity to make approximately $3 billion[4] in strategic R&D investments to expand the limited packaging capability and capacity within the United States to support existing and increased domestic semiconductor manufacturing. These efforts will be particularly important to support the CHIPS Program Office's incentive investments to enable domestic manufacturing of leading-edge semiconductors. The NAPMP will make research and development investments that leverage existing areas of strength for the United States including:

- **Design and simulation tools** — U.S.-based firms lead the development of chip design tools. Innovations in advanced packaging

strongly depend on combining multiple design and engineering stages. The strong interdependency between chip design and packaging presents an opportunity for U.S. companies to augment existing design and simulation products to serve advanced packaging.

- **Manufacturing equipment** — U.S. leadership in microelectronics equipment will be leveraged to implement many wafer-based fab processes necessary for advanced packaging.
- **Research and development strengths** — The nation has strong research and development capabilities in areas relevant to advanced packaging, such as novel materials, wide-bandgap and ultra-wide-bandgap semiconductors, novel memory, and photonics. This expertise can be leveraged along with heterogeneous integration to build advanced, highly functional systems.

MISSION AND OUTCOMES

To enable the CHIPS Research and Development Office's vision for success, the National Advanced Packaging Manufacturing Program will make approximately $3 billion in investments to develop critical and relevant innovations for advanced packaging technologies and accelerate their scaled transition to U.S. manufacturing entities. These investments will include research programs for core technologies that can be scaled to high-volume manufacturing, an advanced packaging piloting facility to support this scaling, resources to support the expansion of advanced packaging solutions, and workforce development. As a result, within a decade, NAPMP-funded activities, coupled with CHIPS manufacturing incentives, will establish a vibrant, self-sustaining, high-volume, domestic, advanced packaging industry where advanced-node chips manufactured in the United States are packaged in the United States. The technology developed will be leveraged in new applications and market sectors and at scale.

As a result of these investments, the NAPMP will:

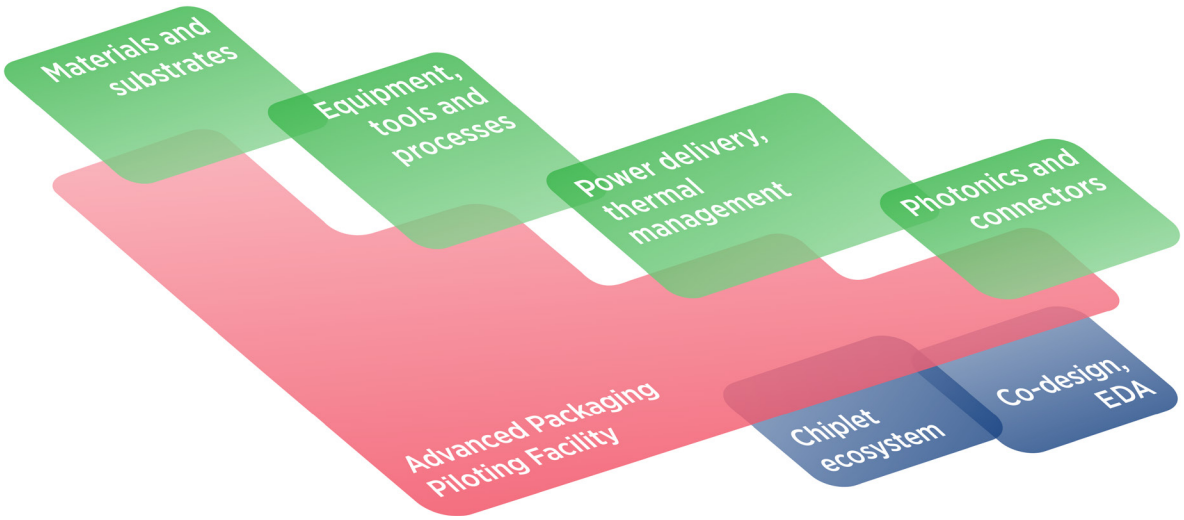
- Enable successful advanced packaging development efforts to be validated and transitioned at scale to U.S. manufacturing.
- Develop packaging platforms capable of both high-volume and customized manufacturing.
- Create an advanced packaging ecosystem based on heterogenous chiplet technology to promote widespread and easy use of the technologies developed.
- Bolster advanced packaging workforce development efforts to sustain the domestic ecosystem.

INVESTMENT AREAS

The CHIPS Research and Development Office has designed the NAPMP to include an **Advanced Packaging Piloting Facility** (APPF) where successful development efforts will be transitioned and validated for scaled transition to U.S. manufacturing. This is a key facility for technology transfer to high-volume manufacturing.

Investments will be made in six additional areas critical to attaining the NAPMP goals and to accelerate advanced packaging where, if successful, the results of these investments will be piloted in the APPF to accelerate commercial deployment.

The six top priority research investment areas and their interdependencies are shown in the figure below and are:



Technology investments are in green. Ecosystem investments are in blue. The piloting facility, in red, will provide opportunities to validate new technologies for transition to U.S. manufacturing.

- **Materials and substrates** are the platform on which advanced packaging is built. The key requirements of new substrates include multiple levels of fine wiring and via pitches, low warpage, large area, and the ability to integrate active and passive components. These substrates may be based on silicon, glass, or organic materials and can include fan-out wafer-level processes.
- Advances in **equipment, tools, and processes** are required, where substrates are patterned and chiplets are reliably assembled on these substrates. CMOS[5] equipment and processes will be adapted to handle dies and wafers compatibly with different types of substrates.
- **Power delivery and thermal management** for advanced packaging assemblies. Advanced packaging is demanding in terms of power density and heat dissipation. Advances in power delivery and efficient thermal management must be solved for advanced packaging to succeed. They require innovative materials and solutions that are compatible with the substrate and assembly processes used. These activities will require new thermal materials as well as novel circuit topologies that employ advanced substrates and heterogeneous integration.
- **Photonics and connectors** that communicate with the outside world. Low error rate photonics and high-density, high-speed, and low-loss active connectors will be needed to manage long haul communications and will require novel and compact solutions. The focus will be on reliable and manufacturable integrated connectors that include computational capability, data pre-

Packaging is complex and interdisciplinary and requires interaction of the areas shown schematically. The intersections among these areas highlights the interdependencies; their seamless interactions are strategically and operationally crucial to success. The NAPMP will proactively drive advances in these areas and in operational interactions.

processing, security, and ease of installation to the packaged assembly.

- Developing a **chiplet ecosystem**. Chiplets refer to small, partially functional, semiconductor chips that, when assembled at tight pitch and close to one another, result in a highly functional subsystem. Chiplet discovery methodologies will be developed to ensure a high level of reusability, design, and warehousing of these chiplets.
- **Co-design** of these multi-chiplet subsystems with automated tools. These will be adapted for advanced packaging with consideration for built-in test and repair, security, interoperability, and reliability, with a detailed understanding of the substrate and processes used for assembly, including the thermal and power management solutions.

These NAPMP investments will develop the robust domestic advanced packaging capabilities necessary to accelerate R&D in packaging, equipment, and process development. They will support the transfer of innovations into full-scale manufacturing, while bolstering advanced packaging workforce development efforts. They will focus on drivers of advanced packaging to develop and transition leap-ahead technologies. They represent key innovation areas in advanced packaging that will underpin future technology directions, and they will support existing and emerging application areas including artificial intelligence, the automotive sector, biomedical devices, the internet of things, and next generation 5G/6G communications.

ADVANCED PACKAGING WORKFORCE

The NAPMP intends to integrate workforce education and training into all NAPMP efforts leveraging internships, co-ops, work-study programs, seminars, hands-on experiential learning, and other educational advancement activities within each investment area and in the APPF. The NAPMP intends to fund projects that incorporate strong workforce development plans that emphasize educational advancement and professional development.

COORDINATION WITH OTHER PROGRAMS

The NAPMP works closely with all of the CHIPS R&D programs to meet the CHIPS R&D Office's collective program goals of accelerating the development and commercial deployment of foundational semiconductor technologies by establishing, connecting, and providing access to domestic tools, resources, workers, and facilities. For example, it is possible that the NSTC will manage physical integration of activities in the APPF. Collaborations with the Metrology Program may develop tools and manufacturing test vehicles to validate the performance of packaged products, and standards development for these new approaches to packaging will be needed to realize their broad adoption.

The NAPMP is working closely with other government agencies on the common goal of increasing U.S. capabilities and capacity in advanced assembly, packaging, and testing with a specific focus on transformational heterogeneous integration technologies that can transfer into the NSTC and NAPMP facilities.

NEXT STEPS

The NAPMP expects to release its first funding opportunity in early 2024. The topic of this first funding opportunity will be materials and substrates. The NAPMP will engage with the stakeholder community to provide more details about the vision and strategy outlined in this paper. This will include public webinars, meetings, and additional materials.

ENDNOTES

[1] The William M. (Mac) Thornberry National Defense Authorization Act for Fiscal Year 2021 authorized funding, while the CHIPS and Science Act of 2022 appropriated funding. Pub. L. 116-283, §§ 9901–9908, 134 Stat. 3388, 4843–4860 (2021) (codified at 15 U.S.C. §§ 4651–4657), as amended by the CHIPS Act of 2022, Pub. L. 117-167, §§ 101–107, 136 Stat. 1366, 1372–1390 (2022) (codified as amended at 15 U.S.C. §§ 4651–4843).

[2] Two recent releases include: Metrology Gaps in the Semiconductor Ecosystem: First Steps Toward Establishing the CHIPS R&D Metrology Program, https://www.nist.gov/document/chips-rd-metrology-gaps-semiconductor-ecosystem, and A Vision and Strategy for the National Semiconductor Technology Center, https://www.nist.gov/document/vision-and-strategy-national-semiconductor-technology-center

[3] North American Advanced Packaging Ecosystem Gap Assessment — Critical Systems, Capability, Capacity Analysis and Recommendations IPC Industry Research Report — November 2021

[4] Pursuant to the requirements of the CHIPS and Science Act of 2022, the Department has allocated $2.9 billion of the amounts made available for FY22 and FY23. An additional approximately $95 million allocation was included in the FY24 NIST Budget Submission to Congress.

[5] Complementary metal oxide semiconductor, or CMOS, is technology used in most integrated circuits.

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